ACE Deliverable 2.1-D3

Report on facilities assessment

Project Number: FP6-IST 508009

Project Title: Antenna Centre of Excellence

Document Type: Deliverable

Document Number: FP6-IST 508009/ 2.1-D3

Contractual Date of Delivery: 31 December 2004

Actual Date of Delivery: 14 January 2005 (with cover-page + reviews). Update 6 January 2005

Workpackage: Mainly WP 2.1-3, but also related to WP 2.1-1 & 2.1-2

Estimated Person Months: 24

Security (PU,PP,RE,CO): PU

Nature: R (Deliverable Report)

Version: rev 0 for the main document

Total Number of Pages: 400

File name: ACE_2.1D3_total.pdf

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Abstract

This report aims at assessing the technologies available for integrated antennas, and the associated facilities. The documentation is divided in four distinct chapters which focusses on the following families of technologies : Semi Conductor and Packaging, Material machining, Structuring technologies, Micro Systems.

Each chapter includes a Survey of existing technologies (Material and Process), and Possible antenna applications.

Keyword List

Active antenna subsystems, phased arrays, beam-forming, beam-steering, control devices, integrated antennas, Micromachining, MMIC, MEMS, packaging

European Commission - 6th Framework Programme	***ACE (Antenna Centre of Excellence)***	Information Society Technologies

Report on technologies and facilities assessment

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Document Evolution		
Revision	Date	Reason of change
0	14.01.05	

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CHAPTER 1

INTRODUCTION

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1. INTRODUCTION

This report aims at assessing the technologies available for integrated antennas, and the associated facilities.

Many technologies are involved in the manufacturing of integrated antennas, which are very different from those used in conventional antennas :

- Active integrated antennas, an issue is the accommodation of active devices within the radiating element, in order to improve its compactness or to add new functionalities. All technologies related to semiconductor and packaging are therefore concerned ;
- For millimetre wave and sub millimetre wave integrated antennas, high accuracy is required for the antenna parameters. Micromachining technologies are therefore of special interests ;
- Structural materials such as substrates, multilayer circuits, dielectrics are also used for the radiating element, with special specifications according to the applications ;
- Micromachined electro-mechanical systems (MEMS) also offer huge opportunities for novel high performance antennas ;

The documentation is divided in four distinct chapters which focusses on the following families of technologies : Semi Conductor and Packaging, Material machining, Structuring technologies, Micro Systems.

Each chapter includes :

- **Survey of existing technologies** (Material and Process), in which the technology is described, the interest is presented, the main characteristics are given (accuracy, RF characteristics, limitations,…), the supplier and manufacturer are listed.
- **Possible antenna applications :** The objective of this section is to illustrate existing or novel applications of the technologies, and to identify the advantages and limitations of each one. Some trade-off analyses between applicable technologies will be presented.

CHAPTER 2

SEMICONDUCTOR AND PACKAGING

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FIGURE 2.2-12: MICROMACHINED LOOP SLOT ANTENNA ON SIGE MMIC, [15] 118

2.1 SURVEY OF SEMICONDUCTOR FOUNDRIES AND TECHNOLOGIES

Semiconductor material is crystalline and can mainly be characterized by its lattice constant, the bandgap between valence and conduction band and charge carrier mobility among other physical properties. The conductivity can be changed by the introduction of impurities (dopant), which can be either n-type (increase of electron number) or p-type (increase of hole number). This enables the formation of pn-junctions for diode or transistor devices, which allow a number of applications.

The most popular semiconductor material is crystalline silicon, the respective technology is mature and well-established and with SiGe a compound material system is available for the realization of heterostructure devices (i.e. devices with a junction between different materials). The most common technologies are bipolar transistors with a homo-junction (i.e. the junction is formed between the same material with different doping concentration), heterostructure bipolar transistors (i.e. with junction at a Si/SiGe interface) and MESFET (metal semiconductor field effect transistor) or MOSFET (metal oxide semiconductor transistor) available in different technologies (e.g. CMOS=Complementary MOS, BICMOS=Bipolar CMOS ...). These devices are exemplary used for digital circuits (e.g. memory, microcontroller) or for power applications (e.g. in mobile applications). The basic disadvantage in view of high-frequency applications is the missing semi-insulating Si-substrate material. This leads to substrate transfer technologies like SOS (silicon on saphire) or more commonly SOI (silicon on insulator) where the thin active layer is transfered to an insulating substrate with better high-frequency properties then silicon substrate and therefore more adequate for RF-application.

Beyond, there is a variety of compound semiconductors available, which consist of two or more basic materials (e.g. the well-known III/V compound semiconductor GaAs). Depending on the position of those elements in the periodic table, compound semiconductor material is classified with respect to the group number as III/V- (e.g. GaAs, InP, GaN) or II/VI-compounds (e.g. ZnO). Even ternary compounds consisting of three different materials can be found, e.g. InGaAs, AlGaAs, InGaP. In comparison to Si, compound semiconductors usually offer higher carrier mobility and provide semi-insulating substrate material. Therefore, they are suitable for high-frequency applications (e.g. oscillator, mixer, amplifier).

The basic advantage of compound semiconductors is variation of bandgap and lattice constant by modifying the concentration of different elements. This enables lattice matched growth of different materials (heterostructure = interface between different materials) with different bandgap but similar lattice constant, the so-called bandgap-engineering. This allows the realization of HEMT (high electron mobility transistor), HBT (heterostructure bipolar transistor) and devices like laser diodes or HBV (hetero barrier varactor).

2.1.1 Semiconductors and their material parameters

For the most interesting semiconductors the key parameters are given to estimate compatibility to existing technologies for the realisation of active antennas for high frequencies.

GaAs:

Basic Parameters at 300 K:	
Crystal structure	Zinc Blende
Group of symmetry	Td2-F43m
Number of atoms in 1 cm3	$4.42 \cdot 10^{22}$
de Broglie electron wavelength	240 A
Debye temperature	360 K
Density	5.32 g cm^{-3}
Dielectric constant (static)	12.9
Dielectric constant (high frequency)	10.89
Effective electron mass m_e	$0.063 \cdot m_o$
Effective hole masses m_h	$0.51 \cdot m_o$
Effective hole masses m_{lp}	$0.082 \cdot m_o$
Electron affinity	4.07 eV
Lattice constant	5.65325 A
Optical phonon energy	0.035 eV

Thermal properties:	
Bulk modulus	$7.53 \cdot 10^{11}$ dyn cm^{-2}
Melting point	1240 °C
Specific heat	0.33 J g^{-1}°C $^{-1}$
Thermal conductivity	0.55 W cm^{-1} °C $^{-1}$
Thermal diffusivity	0.31 $cm^2 s^{-1}$
Thermal expansion, linear	$5.73 \cdot 10^{-6}$ °C $^{-1}$
Melting point	T_m=1513 K
For 0 < P < 45 kbar	T_m= 1513 - 3.5 P (P in kbar)
Saturated vapor pressure (in Pascals)	
T=1173 K	1
T=1323 K	100

Mechanical parameters:

Bulk modulus	$7.53 \cdot 10^{11}$ dyn cm^{-2}
Density	5.317 g cm^{-3}
Hardness on the Mohs scale	between 4 and 5
Surface microhardness (Knoop's pyramid test)	750 kg mm^{-2}
Cleavage plane	{110}
Piezoelectric constant	e_{14}=-0.16 C m^{-2}
Elastic constants 300 K.	$C_{11}=11.90 \cdot 10^{11}$ dyn/cm^2
	$C_{12}=5.34 \cdot 10^{11}$ dyn/cm^2
	$C_{44}=5.96 \cdot 10^{11}$ dyn/cm^2
For T = 300 K	
Bulk modulus (compressibility^{-1})	$B_s= 7.53 \cdot 10^{11}$dyn/cm^2
Shear modulus	C'= $3.285 \cdot 10^{11}$dyn/cm^2
[100] Young's modulus	$Y_o= 8.59 \cdot 1011$dyn/cm^2
[100] Poisson ratio	$\sigma_o = 0.3$

$Si_{1-x}Ge_x$:
Basic parameters:

Crystal structure	Diamond
Group of symmetry	O_h^7-Fd3m
Number of atoms in 1 cm3	$5 \cdot 10^{22}$ (Si), $4.4 \cdot 10^{22}$ (Ge)
Density	2.329 g cm^{-3} (Si), 5.3234 g cm^{-3} (Ge)
Dielectric constant (static)	11.7 (Si), 16.2 (Ge)
Lattice constant a(x)	$(5.431 + 0.20x + 0.027x^2)$ A
Bulk modulus	(97.9 - 22.8x) GPa
Si (x=0)	98 GPa
Ge(x=1)	75 GPa

Linear thermal expansion coefficient :

$Si_{1-x}Ge_x$	$(2.6 + 2.55x) \times 10^{-6}$ K^{-1} x <0.85
	$(-0.89 + 7.53x) \times 10^{-6}$ K^{-1} x >0.85
Si (x=0)	2.6×10^{-6} K^{-1}
Ge(x=1)	5.9×10^{-6} K^{-1}

Debye temperature:

Si (x=0)	640 K
Ge(x=1)	374 K

Melting point:

$Si_{1-x}Ge_x$ (solidus)	$T_s \approx (1412 - 738x + 263x^2)$ °C
$Si_{1-x}Ge_x$ (liquidus)	$T_l \approx (1412 - 80x - 395x^2)$ °C
Si (x=0)	1412 K
Ge(x=1)	937 K

Specific heat:

$Si_{1-x}Ge_x$	$(19.6 + 2.9x)$ J mol^{-1} K^{-1}
Si (x=0)	19.6 J mol^{-1} K^{-1} = 0.7 J g^{-1} K^{-1}
Ge(x=1)	22.5 J mol^{-1} K^{-1} = 0.31 J g^{-1} K^{-1}

Thermal conductivity :

$Si_{1-x}Ge_x$	$(0.046 + 0.084x)$ W cm^{-1} K^{-}	$0.2 < x < 0.85$
Si (x=0)	1.3 W cm^{-1} K^{-1}	
Ge(x=1)	0.58 W cm^{-1} K^{-1}	

Thermal diffusivity

Si (x=0)	0.8 cm^2 s^{-1}
Ge(x=1)	0.36 cm^2 s^{-1}

Thermal expansion coefficient

$Si_{1-x}Ge_x$	$\gamma = (2.6 + 2.55x) \times 10^{-6}$ K^{-1} $x < 0.85$	300 K
$Si_{1-x}Ge_x$	$\gamma = (7.53 - 0.89x) \times 10^{-6}$ K^{-1} $x > 0.85$	300 K

Loss tangents are strongly dependend on manufacturer and can reach typical values as high as 10 k?cm for Si and GaAs.

2.1.2 Technologies

The basic advantage of compound semiconductors compared to silicon is the ability to form a wide variety of interfaces between material systems with similar lattice constants but different energy gaps (bandgap engineering). This additional degree of freedom resulted in heterostructure devices, e.g. high electron mobility transistor (HEMT), hetero-barrier varactor (HBV), or hetero bipolar transistor (HBT). A further advantage is the high electron mobility (and therefore short electron transit time), which leads to higher maximum operation frequencies. Some of those compound semiconductors are suitable for operation at higher temperatures in high-voltage applications due to the higher bandgap and high-current applications because of higher thermal hardness.

From the technological point of view, parasitic effects are reduced and integration with other elements is facilitated using semi-insulating substrate materials. The disadvantage is the lack of a high-quality native oxide on the surface of the III/V-system, which necessitates an additional process step, the passivation of a surface e.g. with silicon oxide. Furthermore, the silicon technology is more simple and mature than the III/V-technology making silicon the first choice for digital circuits.

Technologies	Lateral Current Flow	Vertical Current Flow
Homostructures	Field Effect Transistor MOSFET ft up to 15 GHz P typ 5 mW	Bipolar Junction Transistor ft up to 30 GHz P typ 500 mW
Heterostructures	High Electron Mobility Transistor ft typ. 50 GHz P typ 300 mW	Hetero Bipolar Transistor ft typ. 50 GHz P typ 1000 mW

Nevertheless, compound semiconductors are still the only option for real analog high frequency applications. In contrary to digital circuitry, the integration density for RF-circuits is mainly determined by their peripheral passive circuitry (e.g for matching) and does not follow Moore's law. The electric properties of III/V devices result either from metal-semiconductor interfaces (Schottky-diode, MESFET) and their lateral dimensions or from semiconductor-semiconductor interfaces (HBT).

2.1.3 Active devices and foundries

2.1.3.1 Introduction

As academic research institutes and small companies can not afford own semiconductor fabrication facilities they require external service which allows to bring in their knowledge.

To enable research and development in the area of solid-state electronics a number of companies give access to state-of-the-art semiconductor fabrication facilities to circuit designers with limited or no own process capabilities.

This report gives a survey on semiconductor fabrication facilities which offer their service to external customers. This service includes the fabrication of chips with individual design which are based on the respective technologies. While the basic process technologies are fixed, device usage can be defined by customer needs. Beyond this, model libraries and support for circuit design is offered and a review process with rule-checking for verification of the final product can be applied.

Detailed information about process technologies is given where available. This allows for a effective pre-check of the feasibility for the targeted applications.

The listed companies are chosen with respect to the capabilities of industrial standard processes. The given companies offer devices and circuits based on different material systems and process technologies which include Si based MOS technology, SiGe based HBT and GaAs HEMT. The application ranges from digital signal processing over mixed signal chips to pure high frequency circuits up to 100 GHz.

The companies offer products ranging from single devices over mixed circuits to ASIC's (Application Specific Integrated Circuit). ASIC's are custom chips which implement a high number of logical functions for specialized tasks. They are specially designed and optimized for a certain application and requirement (e.g. power saving in mobile phones). VLSI (Very Large Scale Integration) capabilities are also offered for higher integration densities (logical units complexity is typ. 1000-20000).

Furthermore, possibilities for combining multiple single chips into a large module are given yielding in a MCM (Multi Chip module). A multichip module could be defined in a number of ways. Some define it as a structure consisting of two or more integrated circuits electrically connected to a common circuit base and interconnected by conductors in that base. A second approach to defining MCMs is based on the silicon efficiency achieved by the technology. Using this approach, an MCM is defined as a structure in which a packaging efficiency of greater than 30% is achieved. This definition implies a particular technology that allows chips to be packed closely together. The completed chips can be packaged in different ways.

Typical packaging options are listed in the following:

- DIL/DIP: Dual in-line package. DIL is a rectangular package for electronic devices, which offers two connection pin rows on opposite sites of the housing. In the beginning, this was the standard housing form for integrated circuits and usually offers 8-48 pins.
- PGA: Pin Grid Array
- CPGA: Ceramic Pin Grid Array
- OPGA: Organic Pin Grid Array
- CLCC: Ceramic Leadless Chip Carrier
- JLCC: J-Leaded Chip Carrier

CQFP: Ceramic Quad Flat-pack
SOIC: Small Outline Integrated Circuit

Additionally some material parameters are given for the useable semiconductors which allow estimating possible integration of antennas and their performance.

Most of the listed foundries can be accessed through EUROPRACTICE, which are their partners for processing. This allows flexibility and cost reduction for new developments and their realisation.

2.1.3.2 Europractice (http://www.europractice.com/)

EUROPRACTICE was launched by the European Commission (DGIII) in October 1995 to help companies improve their competitive position in world markets by adopting ASIC, Multi-Chip Module (MCM) or Microsystems solutions in the products they manufacture

The program helps to reduce the perceived risks and costs associated with these technologies by offering potential users a range of services, including initial advice and ongoing support, reduced entry costs and a clear route to chip manufacture and product supply. EUROPRACTICE can also provide users with the training and CAD software required to design and develop their ASIC, MCM or Microsystems solution.

The EUROPRACTICE IC Service is offered by a consortium of following partners :

- IMEC (Belgium)
  - Coordinator
  - Academic Support
  - MPW & Small Volume
- RAL (United Kingdom)
  - CAD Support
  - Academic Support
- FhG-IIS **(Germany)**
  - MPW & Small Volume

The IC service has been started in October 1995 by **IMEC** (Belgium) to setup a low cost and easy access to ASIC design, prototype and small volume fabrication. These activities are part of the global EUROPRACTICE project in order to stimulate industry to use ASIC solutions in their new product developments and to stimulate academics to introduce new design methodologies in their curricula.

During the past years, the IC service of EUROPRACTICE has been developed to one of the most successful ASIC prototype and small volume service in Europe.

The European Commission funded the EUROPRACTICE initiative in 2000, 2001 and 2002 in order to strenghten the offered services, to increase the quality, and to setup close cooperation with design houses in order to offer a complete solution including design and fabrication to their customers. This will further strenghten the possibility of new successful ASIC developments.

Multi Project Wafer Runs:
EUROPRACTICE reduces the cost for ASIC prototyping by combining several designs from different customers onto one wafer. This approach, known as **Multi-Project Wafer (MPW)**, allows the costs to be shared among a number of customers.

Fabrication of prototypes can thus be as low as 5% to 10% of the cost of a full wafer run. A limited number of tested or untested ASIC prototypes, typically 10-20, are delivered to the customer for evaluation, either as naked dies or as encapsulated devices. Only prototypes from fully qualified wafers are taken to ensure that the chips delivered will function first time right.
In order to achieve this, extensive Design Rule and Electrical Rule Checkings are performed on all designs submitted to the Prototyping Service.

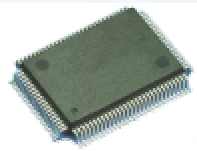
EUROPRACTICE is organising about 130 MPW runs per year in various technologies. Most of the participating customers use these runs to get cheap samples for validation of their self-made designs.

Design Kits:
Designers need the necessary information (design rules, electrical parameters, cell library, etc.) of the chosen technology before they can start the design phase. All this information is put together by the foundry in the so-called 'design kit'. EUROPRACTICE has bundled all the design kits for the different technologies and CAD tools together on a CD-ROM. Customers can have a copy of the CD-ROM and the design kits by signing a non-disclosure agreement (NDA) with EUROPRACTICE.

Prototype testing:

In most of the cases the customers test their ASIC samples themselves. But for those who do not have this possibility prototype testing is offerd by EUROPRACTICE. In order to set up a test solution, the testvectors are needed from the customer. The testvectors are software generated (simulation) or manually made by the designer.

Prototype encapsulation:



EUROPRACTICE ASIC service offers encapsulated prototypes. It is required to supply the prototypes in a package which is as close as possible to the final ASICs delivered in production. The packaging is done by industrial assembly houses and the range of prototype packages includes DIL, SOIC, CLCC, JLCC, PGA, CQFP, etc.

During the past two years the Europractice IC Service has extended its MPW prototyping service to a one-stop solution for industrial low volume production. EUROPRACTICE bridges the gap between prototypes and the minimum production runs associated with most foundries. Agreement has been reached with a number of major European manufacturing facilities for wafer runs ranging from only two to several hundred, thus providing companies with fully functional ASICs in quantities as low as 100 through to 100,000. Design support, design services, silicon production, encapsulation and testing services have been combined to offer flexible interfaces from any level of ASIC development.

For small volume fabrication, a contract is signed between one of the EUROPRACTICE partners (IMEC or FhG-IIS) and the customer. The contracted EUROPRACTICE partner then coordinates the different activities by subcontracting :

- wafer fabrication to the selected foundry
- encapsulation to the selected assembly house
- testing to the selected test house

Small volume fabrication flow:
The verified GDSII data can be used for prototype fabrication on a MPW run or for a small wafer batch with dedicated mask set for prototype samples. When the volume is sufficiently low the complete volume can be produced and some samples are used for prototype verification and test solution debugging.

If prototypes have not been verified before the small volume production, some samples are encapsulated for test debug and full qualification. In order to avoid delays, lead frames and packages must be ordered already during silicon production. Delivery of package specification, bonding diagram and marking instructions at the time of layout submission guarantees the lead time necessary.When prototypes have been qualified during a separate prototyping phase, one can immediately proceed to volume testing.

Testing circuits on wafer avoids encapsulating non-functional circuits. Therefore, EUROPRACTICE compares the costs for wafer test solution (probecard, etc.) and wafer test against costs for encapsulating non-functional devices (depending on expected yield and package costs). Test program generation and probe card manufacturing require some lead time. To avoid delays, test pattern and test specification have to be delivered 6-8 weeks in advance.

Tested or untested wafers are shipped for encapsulation. As most of the plastic encapsulation is performed in Far East, 2 weeks delivery time is minimum, even when paying additional fees for hot lot encapsulation.The full range of available plastic packages including PDIP, SO, PLCC, QPFP, etc. is offered.

Final test is performed on encapsulated devices and functional parts are delivered to the customer. If prototype devices are available, debug of final test solution can be done during volume encapsulation, thus speeding up the production process. The final production test flow is, for industrially used components, performed according to the following :

- Full electrical test at 25 degrees C
- If applicable 100% test of all electrical parameters at extended temperatures (minimum and maximum)
- On sample basis a production batch is exposed to further electrical analysis in order to secure long term electrical stability

The electrical test must check the full specification which means that a normal test programme in the production phase will at least have the following sequence :

- Connectivity
- Power supply current
- Leakage input/output
- Input voltage check
- Output voltage/current check
- Functionality in all voltage corners

- Full dynamic parameter test
- Application specific test and other special analog parameters

Industrial qualification:
In order to cover the area of product responsibility and liability of the ASIC-components produced for the customer a qualification has to be performed. This is done in order to be able to give the warranty on the components produced. The activity at this level is dependent on the volume and complexity of the ASIC component. As a minimum the long term reliability of the components has to be checked for critical design/process failures with the following flow at sample basis:

- Full electrical test
- Temperature cycling
- Full electrical test
- Burn-in
- Full electrical test

The level of qualification is dependent on the warranty levels for the produced ASICs. Some customers are using the ASICs in specific applications ranging from space, military, automotive to medical applications. In order to be responsible for those ASICs an extended qualification and screening programme has to be performed.

2.1.3.3 AMI Semiconductor (http://www.amis.com/)

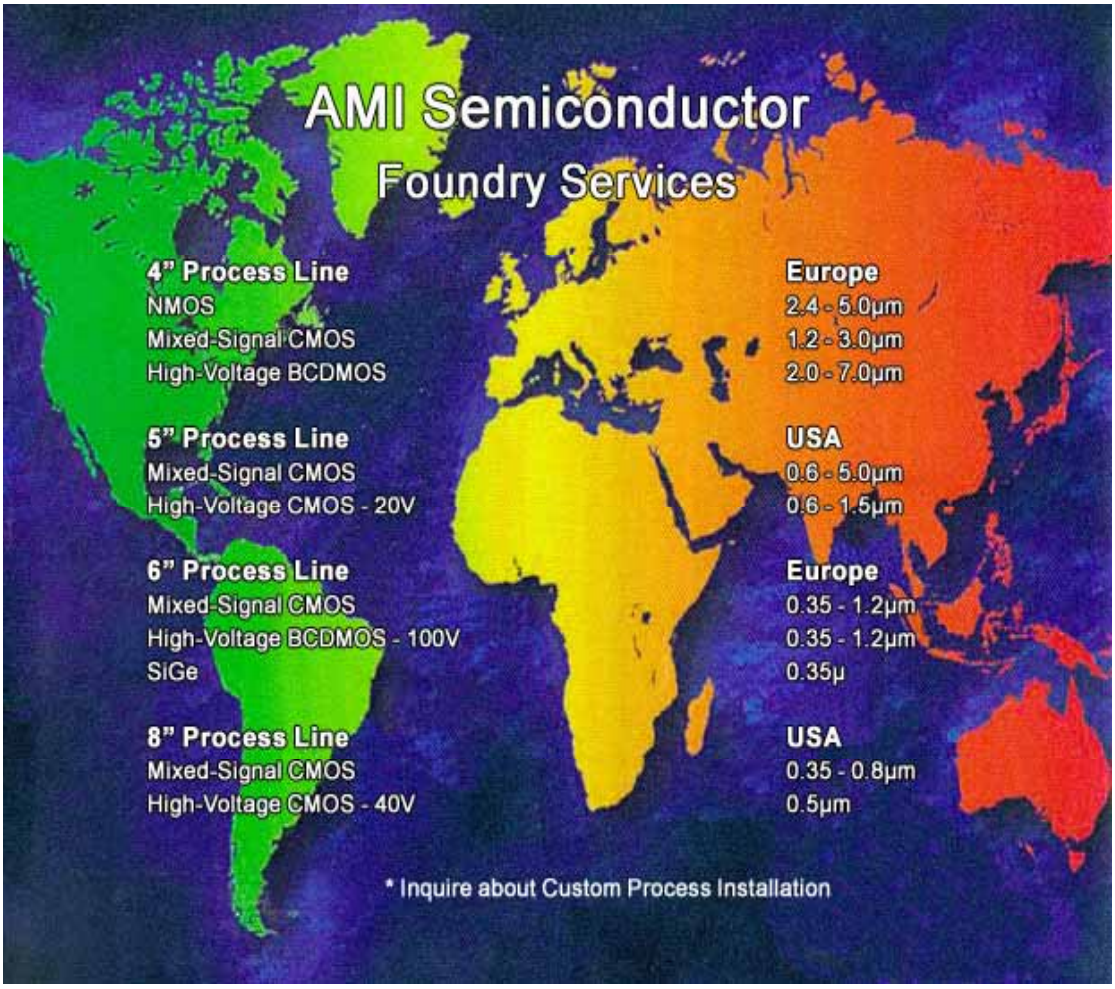
Mixed-Signal Foundry Services:
AMI Semiconductor has a long-standing experience as a mixed-signal foundry

- Over 34 years of experience
- #1 in customer service
- Shortest span from start of project to production
- Web based information system
- Process longevity
- Process lifetimes to match automotive, medical, and industrial requirements
- High-voltage
- Wide selection of mixed-signal processes with up to 100V capability
- Multi-continent fab operations
- Custom process installations - convenient and timely communications

Mixed-Signal Foundry:
Customer service and satisfaction are paramount for AMI Semiconductor. An experienced development customer service representative (CSR) pushes the design through the engineering and prototype stages to ensure the best prototype cycle time in the industry. If customers need an expedited turn time, the development CSR will develop a special program for them. Superior service continues in production. A knowledgeable factory-based product marketing manager and CSR are available to quickly respond to inquiries and service immediate needs.

The MyAMIS website enables AMIS customers to access available intellectual property (IP) libraries, review/request legal agreements, monitor product activity, and view associated trend charts. Global presence ensures accurate and responsive communications with factories in the USA (Pocatello, Idaho) and Europe (Oudenaarde, Belgium). If the product has a long-life cycle, AMIS is an excellent choice as foundry partner.

Multi-Project Support:



AMI Semiconductor is affiliated with two "multi-project houses" - MOSIS and Europractice. Both are low-cost prototyping and small-volume production services for VLSI circuit development. Mask generation, wafer fabrication and device packaging can be contracted through MOSIS and Europractice to AMIS.

MOSIS and Europractice keep the cost of fabricating prototype quantities low by aggregating multiple designs onto one mask set. This option provides yet another cost-effective tool for customers. MOSIS and Europractice have certified AMIS as a qualified foundry supplier. A variety of both foundry-specific and vendor-independent CAD tools, design kits and libraries may be used to prepare the design. Reticles with multi-chip designs are sent to AMIS, processed on a routine schedule and the device's function and performance results are provided to the customer.

Fab process performance is reviewed routinely by the multi-project houses. Special test chips are included on every reticle to monitor wafer fab performance.

This multi-project approach is a cost-effective and efficient technique for the new project developer and the low volume user. When project volumes increase, GDSII can be forwarded to the foundries for a cost effective production run.

High-Voltage Mixed-Signal Solutions:
AMI Semiconductor provides leading-edge solutions for applications that combine mixed-signal with high-voltage functionality - up to 100V, low-power technology, complex digital circuitry and signal processing capabilities, all on a single chip.

AMIS has developed an ambitious roadmap of new high-voltage 0.35µm CMOS-based technologies operating at up to 80V. AMIS developed this I3T technology in response to the increasing demand for more digital integration, combined with mixed analog and smart power high-voltage structures. This technology enables customers to develop complex, high-voltage smart power SoC solutions for applications in markets such as automotive and industrial.

Rounding out AMI Semiconductor's portfolio of high-voltage/smart power technologies is the I2T (Intelligent Interface Technology) family. This technology platform includes 30V, 60V and 100V optimized modules on 0.7µm mixed-mode CMOS, as well as embedded EEPROM and OTP.

For applications that are especially cost sensitive, AMIS offers its 0.5µm C5X mixed-signal process, which gives customers a medium-density, high-performance mixed-signal technology capable of integrating complex analog functions, digital content, 20V capability. The C5X process delivers the advantages of a dedicated mixed-signal 0.5µm process without the costs associated with the extra mask steps required for 30V, 60V or 100V capability.

Foundry Process Technology:

Process Name	Design Info	Min. Drawn Poly	Sub. Type	# Metal Layers	Wafer Size(in)	Max. Oper. Voltage	Metal1 Pitch	OTP	EE PROM	Poly-Poly Cap	Nchan DMOS	Pchan DMOS	Bi polars	Trans Char	Other Devices
CE	D	5.0	N	1	5	12.0	5.0			Y				Poly	resistors
CC	D	3.0	N/P	1,2	5	10.0	5.0			Y				Poly	resistors
N24	N	2.4	P	1,2	4	5.0								Poly	resistors
HBIMOSF	D	2.5	P	2	6	80.0		Y		Y	Y	Y	Y	Poly	resistors
CB	D	2.0	N/P		5	5.0	5.0							Poly	resistors
AB	B	1.5	N/P	2	5	5.0	3.5	Y		Y	Y	Y	Y	Poly	resistors
CA	B	1.25	P	2	5	5.0	4.0							Poly	resistors
CY	B	1.0	P	2,3	5	5.0	3.0	Y		Y				Poly	resistors
CW	B	0.8	P	2,3	5	5.0	2.0	Y		Y				Poly	resistors
C07E	F	0.7	P	2,3	6	5.0	1.8	Y	Y	Y	Y			Poly	misc.
I2T100	F	0.7	P	2,3	6	100.0	1.8	Y	Y	Y	Y	Y	Y	Poly	misc.
I2T30E	F	0.7	P	2,3	6	30.0	1.8	Y	Y	Y	Y	Y	Y	Poly	
C5	L	0.6	P	2,3	8	5.0	1.2		Y	Y	Y	Y		Poly	misc.
C4	N	0.6	P	3-5	8	5.0	1.0		Y	Y	Y	Y		Poly	misc.
C05	F	0.5	P	2-3	6	3.3	1.5							Salicide	misc.
L5	B	0.5	P	2,3	8	3.3	1.2							Poly	resistors
C035U	F	0.35	P	2-5	6,8	3.3	1.0			Y				Salicide	resistors
I3T80	F	0.35	P	2-5	6	62.0	1.0	Y	Y	Y	Y	Y	Y	Salicide	misc.
I3T50	F	0.35	P	2-5	6	40.0	1.0	Y		Y	Y	Y	Y	Salicide	
I3T25	F	0.35	P	2-5	8	17.0	1.0	Y		Y	Y	Y	Y	Salicide	
C3	L	0.35	P	3-5	8	3.3	1.0		Y	Y				Salicide	resistors

Note: 4- and 6-inch wafers are manufactured in Oudenaarde Belgium
5- and 8-inch wafer are manufactured in Pocatello, Idaho, USA

Project Kick-off:
Prior to starting the project AMIS needs:

1. Geometric Database (GDSII)
2. A Foundry Start Package is intended as an aid to both the foundry customer and AMIS in preparing AMIS for receipt of design and test data. The information provided by the foundry customer gives AMIS the basic instructions to begin the development task in foundry.
3. Purchase Order.

Once AMI Semiconductor receives these items, the project is assigned to a development customer service representative (CSR)/project manager who reviews the information and creates a work statement to begin the project. The information is then sent to AMI Semiconductor's data prep/reticle generation group for design rule checks and device layout. After confirming the design rules are correct, reticles will be ordered. Project kick-off typically requires 1-2 weeks.

Transferring the product to production:
Once the project evaluation is complete, the foundry development CSR will work with the customer to complete the prototype approval form and officially transfer the product from engineering to production.

Foundry:
With greater than three decades of experience, AMIS is a experienced mixed-signal foundry. An experienced group of professionals will quickly turn the geometric data into prototypes in the finished product form you require. AMIS provides process longevity with process lifetimes to match the product life requirements. Whether wafers, die, or tested package units, AMIS has the streamlined prototype flow needed to keep development projects on schedule.

2.1.3.4 ATMEL (http://www.atmel.com/)

Atmel's New High-speed SiGe Power Technology Available as Foundry Service:

Atmel announced the release of its new 0.5 micron Silicon Germanium (SiGe) HBT bipolar semiconductor technology SiGe2-Power. This technology offers designers additional performance at a reasonable cost for RF applications with even higher frequency and higher power requirements. The new SiGe2-Power technology is a shrink version of Atmel's SiGe1-Power bipolar 0.8 micron process which has been in high-volume production since 1999.

This technology supports simultaneous use of two available transistor types, with switching speeds of 35/45 GHz cut-off frequency, 90 GHz cut-off for power gain, and breakdown voltages of 6/4 V. The new 3-layer metal system introduced with SiGe2-Power has been optimized for high current densities. Stacked vias enable design engineers to improve the performance and layout of their power amplifier and front-end designs. The transistor performance improvement facilitates high gains, especially for RF applications above 2 GHz. This helps to eliminate the number of stages and enables simpler, cost-effective designs.

A preliminary version of the design kit for SiGe2-Power is available now, the complete design kit is available since December 2003. Atmel also offers Multi Project Wafer runs (MPW or "pizza masks") for low-cost prototyping as well as assembly and test services for all SiGe processes. The first SiGe2-Power MPW run will start in November 2003, MPWs will be continued quarterly.

Atmel operates 5 wafer manufacturing facilities using leading-edge technologies. Its extensive manufacturing is also made available to customers who want to access silicon foundry for their products. In addition to SiGe, Atmel's foundry service includes state-of-the-art production lines for CMOS NVM, BiCMOS, Bipolar and BCDMOS/ BCD-on-SOI technologies that benefit from Atmel's strong experience in statistical methods and manufacturing tools.

Multi-Project Wafers (MPW):
Multi-Project Wafers can offer a real benefit to customers. Multiple projects (die) are run together on a wafer-run in the fab. Sharing the same reticle and wafer-run allows a lower cost of entry for customers wanting to prototype in AT46000 SiGe BiCMOS.For manufacturing efficiencies and to accommodate various customer needs, die sites of 2.5 mm x 2.5 mm, 5.0 mm x 5.0 mm, or 10.0 mm x 10.0 mm are provided.

2.1.3.4.1 AT46000 SiGe BiCMOS Process

In 1998, Atmel acquired a 0.8-micron SiGe Bipolar technology. Atmel in Colorado Springs has integrated this bipolar technology with existing 0.35-micron BiCMOS capability allowing system-level IC design with mixed RF, analog, and digital. Atmel's AT46000 SiGe BiCMOS process is suitable for IC design applications in telecommunications and high-speed data up to 12 GHz. This process offers designers transistor speeds of 50 GHz, at 3.3 volt CMOS with a 5.0 volt I/O option, and a complete digital standard cell library. The AT46000 process is the first of several SiGe BiCMOS processes offered in Atmel's roadmap.

2.1.3.4.2 AT46700 SiGe BiCMOS Process

The second SiGe BiCMOS process in Atmel's development roadmap is the AT46700. This process was created by replacing the bipolar transistor in the AT46000 with a 0.4um NPN. AT46700 offers designers transistor speeds of 70 GHz at 3.3 volt CMOS with a 5.0 volt I/O option as well as a complete digital standard cell library. The AT46700 process is the second of several SiGe BiCMOS processes offered in Atmel's roadmap and is ideally suited for wireless data communications applications. (WLAN, cellular, satellite, etc.)

2.1.3.4.3 UHF6 Bipolar Foundry

Atmel's versatile full featured, double-poly, bipolar 0.5µm process has been in production since 1999. This industry-leading process is a high-performance, attractively priced 0.5 µm bipolar technology with FT of 33 GHz and a complementary NPN and VPNP, optimised for low power one-chip RF solutions due to its I2L capability with 6600 gates/mm2.

This technology is in high volume production for a broad range of products from DECT, WLAN, GPS, to CD/DVD laser drivers.

UHF6 Applications:
Cost efficiency and high-speed performance of Atmel's UHF6 process makes it deal for IC design applications in telecommunications, especially RF frontend SoC designs including RX, TX, VCO, PLL as well as high speed digital designs and high current driver IC's, e.g. DECT, GPS, WLAN, RKE, CD/DVD and almost any type of wireless and RF components.

UHF6 Performance:

Devices	UHF6	
Types of NPN	2	
Minimum pitch [µm]	3	
Minimum emitter width [µm]	0.5	
Current gain SIC (non-SIC)	80 (60)	
BVCB0[V]	12	15
BVCE0[V]	3.3	7.0
FT [GHz]	33	23
Fmax [GHz]	35	35
Low-ohmic resistor [Ohm/sq]	8	
Medium-ohmic polysilicon resistor [Ohm/sq]	90	
High-ohmic polysilicon resistor [Ohm/sq]	2000	
I2L, Collector 0.7 x 0.7 µm2	6600 gates / mm2	
Inductors (Qmax @ 2.4 GHz)	10	
Dielectric Capacitors (double-poly) [fF/µm^2]	1.4	
LPNP	fT=75MHz (VCE=2V) hFE=60, BVCEO=7V	
VPNP1 (low cost)	Emitter 1.4 x 1.4µm2, fT=2.5 GHz (VCE=2V), hFE=40, BVCEO=7V	
VPNP2 (cpmplementary)	Emitter 0.5 x 0.7µm2, fT=10 GHz (VCE=2V), hFE=40, BVCEO=7V	
Clamp Diode	Yes	
ESD-diode	Yes 2 Types	
Varactor-diode	Tuning range 3.5	
Metal layers	2	

Engineering Run (ER):
Engineering runs lots consisting of 15 wafers can be started on demand. Customers have the ability to put wafers on hold at different process steps to allow quick turnaround time product changes.

Multi Project Wafers (MPW) will be offered in 2004. MPW's offer an easy mechanism for UHF6 process evaluation for minimal commitment. Additionally, MPWs allow very cost effective design by offering design area on a shared wafer, starting at 6.25 mm^2. Furthermore, Atmel can offer additional services including: assembly, test, qualification, and, depending upon circumstances, design support.

2.1.3.4.4 SiGe HBT Process

Introduced early last year, Atmel offers another world-class process, called SiGe2, with FT of > 80 GHz. This 0.5 µm SiGe HBT bipolar process offers designers additional performance at reasonable cost for higher frequency RF and fiber optic applications.

SiGe Applications:
Cost efficiency and high-speed performance of Atmel's SiGe processes make them ideal for IC design applications in telecommunications and high-speed data, e.g. front-end design (DECT, CDMA, Bluetooth, ...), 5.8GHz WLAN, new power amplifier requirements (WCDMA, 802.11, Bluetooth range extension, etc.), optical networking to OC192 and above, and almost any type of wireless and RF components.

SiGe Performance:
Comparison table of SiGe Bipolar Technologies.

Devices	SiGe1-RF		SiGe1-Power	SiGe2-RF		SiGe2-Power	
Types of NPN-HBT	2		1	2		2	
Minimum pitch [µm]	5		5	3		3	
Minimum emitter width [µm]	0.8		0.8	0.5		0.5	
Base sheet resistance [Ohm]	1500		1500	2000		1400	
Current gain	180		180	250		180	
V_{CB0} [V]	15	12	20	11.0	9.5	16	15.5
V_{CE0} [V]	6	3	7.3	4.3	2.4	6.3	4.5
F_T [GHz]	30	50	25	50	80	33	42
F_{max} [GHz]	50	50	50	90	90	90	90
Low-ohmic resistor [Ohm/sq]	4.5		4.5	4		4	
Medium-ohmic resistor [Ohm/sq]	110		110	150		150	
High-ohmic resistor I [Ohm/sq]	360		360	430		430	
High-ohmic resistor II [Ohm/sq]	n.a.		n.a.	1500		1500	
Inductors (Q_{max} at 2 GHz)	20		20	20		20	

Devices	SiGe1-RF	SiGe1-Power	SiGe2-RF	SiGe2-Power
Typ1 Capacitors [fF/μm^2]	1.1	1.1	1.1	1.1
High Q (MIM) Capacitors [fF/μm^2]	n.a.	n.a.	0.93	0.93
LPNP	1	1	1	1
Schottky-diode	1	1	1	1
ESD-diode	2	2	2	2
Varactor-diode	n.a.	n.a.	1	1
Metal layers	3	3	3	3

2.1.3.4.5 Atmel's CMOS & BiCMOS Processes with Non Volatile and Mixed-signal Capability

Atmel's mixed-signal processes are based on a 0.8 to 0.35 μm CMOS or on a 1-micron BiCMOS technologies.

These processes are Mixed-Analog oriented with high voltage (20 V to 60 V) capabilities. A dedicated process with high temperature (up to 200°C) is also available. Non-volatile memories combined with optimized linear components are integrated in attractive CADENCE design kits.

Customers can rely on wafers fabricated in different sites qualified according to ISO/TS16949/ISO14001.

Processes:

Name	BICMOS2	0.8 μm	SCMOS3E	SCMOS3EE	0.35 μm
	BICMOS	CMOS	CMOS	CMOS	CMOS
Litho (μm)	1.0	0.8	0.5	0.5	0.35
Substrate	Si	Si	Si	Si	Si
NV Memory option			EPROM/OTP	EEPROM	EEPROM
Design Kit	Y	Y	Y	Y	2004Q1
Bipolar	Y	N	N	N	N
HV -(Vdmax)	60 V	N	N	20 V - 42V*	N
High Temperature	N	N	200°C	N	N
Linear high value resistor	N	Y	Y	Y	Y
Linear Capacitor	N	Y	Y	Y	Y

- 42V in development

2.1.3.4.6 BCD-on-SOI/SMARTIS Process

Atmel's BCD-on-SOI process is a 0.8 (0.5) µm technology called SMARTIS, and supports operation up to 85 V. This technology is based on a 20-mask process, single poly and third-metal layers, optimized in terms of energy capability and on-resistance.

With an average gate density of 4000 gates/qmm, this process enables system integration of medium-complex logic like state machines or microcontroller cores together with high-voltage DMOS components.

The DMOS devices are available for 25 V, 45 V, 65 V and 80 V breakdown voltages. The on-resistance values, depending on the breakdown voltage, are in a range of 0.06 to 0.15 Ohm/ mm2. The maximum available junction temperature is Tj = 200°C.

Customers can rely on wafers fabricated in Heilbronn/Germany and qualified according to VDA6, Part 1/ ISO9001 for automotive products.

Atmel can provide foundry wafers or packaged/ tested dies.

SMARTIS Applications:
The benefits of the SMARTIS technology (enormous chip size reduction in comparison to bulk technology, improved EMC features, reduced standby current and latch-up effects) make this process highly efficient and very attractive for IC design applications in many areas:

- Power management systems
- 42-V automotive board network
- Class D audio amplifiers
- Smart motor control/ CD drivers
- ADSL line drivers
- lasma monitor driver

SMARTIS Performance:
Main Electrical Parameters

	Bipolar				
		LNPN	LPNP		
Current Gain	hFE	60	12		
Early Voltage	VEarly (V)	40	-25		
Breakdown Voltage	BVCEO (V)	15	40		
		DIODES			
		Free-wheeling	Zener		
	BV(V)	80	6.2 / 24.5		
	CMOS				
		NMOS	PMOS		
Threshold Voltage	Vth (V)	0.9	-0.9		
Breakdown Voltage	VDSmax (V)	5.5	5.5		
		DMOS			
	N/P	LVMOS	NVMOS	HVMOS	UVMOS
Threshold Voltage	Vth (V)	+/- 0.9	+/- 0.9	+/- 0.9	+/- 0.9
ON-resistance	rdson (Ohm mm2)	0.06/0.35	0.11/0.7	0.13/0.85	0.15
Breakdown Voltage	VDSnax (V)	25/-25	45/-45	65/-65	80/-80

2.1.3.4.7 BCDMOS

Atmel's BCDMOS process, which is in mass production since 1999, is a 0.8-micron BCDIII technology and supports operations up to 80 V. This technology is based on a 19-mask process and covers industrial and automotive requirements for mixed-signal applications.

With an average gate density of 1740 gates/qmm, medium-complex logic like state machines can be realized with competitive chip size. This is also supported by the driver stages' low on-resistance of 0.5 Ohm/mm2 at Tj= 150°C junction temperature. The product line includes NPN and PNP transistors, 0.8-µm NMOS and PMOS for digital functions (5 V), Zener diodes, various resistances and capacitances. The DMOS transistors are available as NMOS and PMOS isolated and non-isolated components for 60-V and 85-V breakdown voltages.

Customers can rely on wafers fabricated in Heilbronn/Germany and qualified according to VDA6, Part 1/ ISO9001 for automotive products.

Atmel can provide foundry wafers or packaged /tested dies.

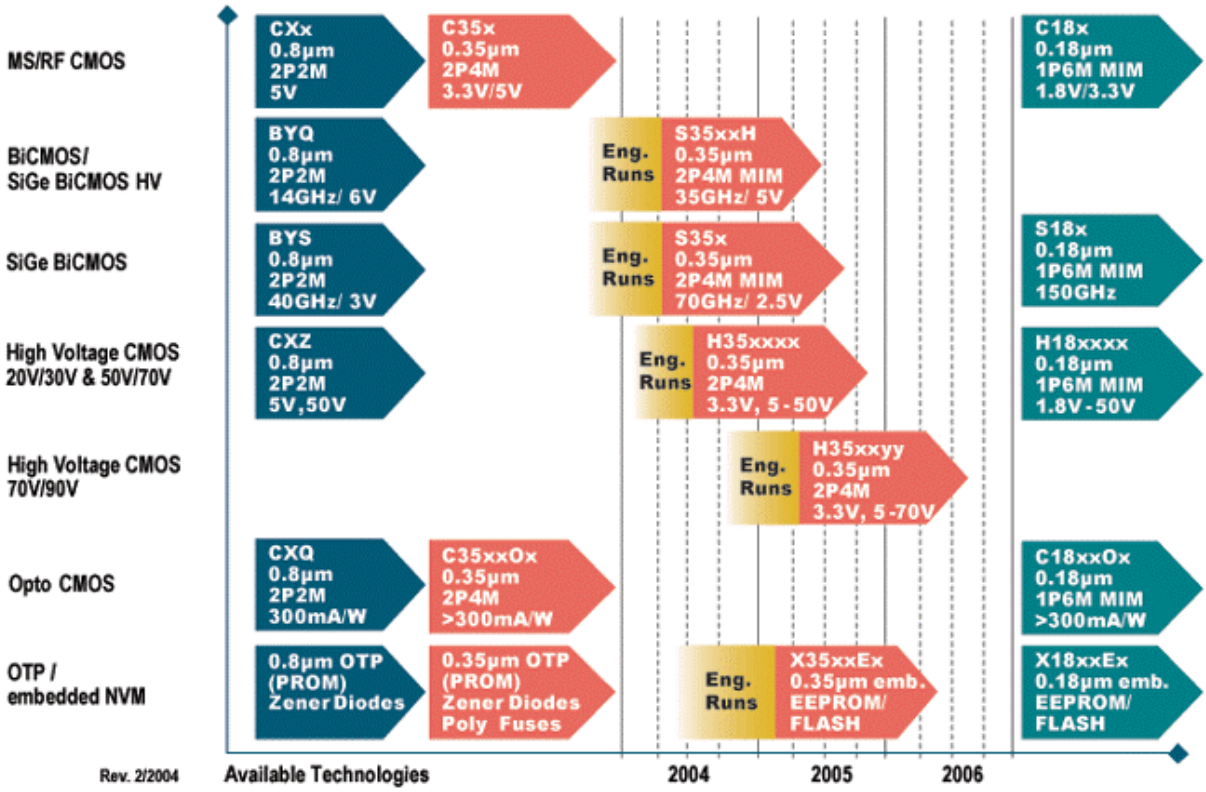
2.1.3.5 Austrian Microsystems (http://www.austriamicrosystems.com/)

Technology:
Technological development is progressing towards ever smaller geometries "deep sub micron" enabling the integration of complete integrated electronic systems on a single chip ("system-level integration"). With a view to the future such products can only be realized on a 200 mm line.

The specialized processes, such as high-voltage CMOS, BiCMOS and SiGe-BiCMOS, offer a unique process base for Application Specific Integrated Circuits (ASIC) and Application Specific Standard Products (ASSP) products that are exceptionally challenging from a technical manufacturing point of view. The realization of the new production line allows these special technologies to be produced with geometries in the range of 0.8 µm and 0.35 µm.

The new facility is prepared to develop and manufacture future technology generations down to 0.18µm.

Capacity:
The new production line offers a capacity of at least 3,000 Wafer Starts Per Week (WSPW) with a clean room floor area of 2,600 square meters, a significant increase over existing in-house Semiconductor production capacity. Production has started in January 2002 with a capacity of 600 WSPW (Waferstarts per Week), The currently installed capacity is 1200 WSPW and will be increased to 1500 WSPW soon.



2.1.3.5.1 0.35 µm CMOS Process Technology

Applications:
Digital, Analog and Mixed Signal Systems Key Features

- 0.35µm CMOS polycide-gate process
- Four unrestricted layers of metal
- Second layer of poly for linear capacitors and linear resistors
- Peripheral cells with high driving capability
- High performance digital and mixed signal capabilities

Key Specifications:
C35B3C0 2P/3M 3.3V CMOS Mixed Signal, PIP
C35B3C1 2P/3M 3.3V CMOS Mixed Signal, PIP, 5V periphery
C35B4C3 2P/4M 3.3V CMOS Mixed Signal, PIP, high-res poly, 5V periphery
Minimum Feature Size: 0.35µm gates
Supply Voltage: CMOS 3.3V; periphery up to 5.5V
Gate Delay: 0.10ns (NAND2 typical)

Description:
austriamicrosystems' 0.35µm CMOS process family is fully compatible to the 0.35µm mixed signal base process licensed from TSMC. The high density CMOS standard cell library optimized for synthesis and 3- and 4-layer routing guarantees highest gate densities. Peripheral cell libraries are available for 3.3V and 5V with high driving capabilities and excellent ESD performance. Qualified digital macro blocks (RAM, diffusion programmable ROM and DPRAM) are available on request. A variety of high performance analog-to-digital and digital-to-analog converters can be provided for integration on the same ASIC.

2.1.3.5.2 0.8 µm CMOS Process Technology

Applications:
Digital, Analog, Mixed Mode Circuits
Instrumentation
Fast High Precision Mixed Signal Circuits
AD/DA Converters
Analog Frontends for Sensors and Transducers

Description:
CXB 2.5-5.5V p-sub, 2-metal, 1-poly
CXE 2.5-5.5V p-sub, 2-metal, 2-poly
CXQ 2.5-5.5V p-sub, 2-metal, 2-poly, hr-poly Key Features

- 0.8 µm CMOS Si-Gate process technology with linear capacitor module
- Two unrestricted layers of metal
- Second layer of poly options for linear capacitors
- High resistive poly options
- High voltage variants available
- TTL and CMOS interfacing capability
- Peripheral cells with high driving capability
- High performance digital and mixed signal capabilities

2.1.3.5.3 CMOS Technology Selection Guide

Process Name	units	C35B3C0	C35B3C1	C35B4C3	CXB	CXE	CXQ
Process Type		**mixed signal CMOS**			**mixed signal CMOS**		
Drawn MOS Channel Length	µm	0,35			0,8		
Operating Voltage	V	2.5 - 3.6	IO -5.5	IO -5.5	2.5 - 5.5		
Number of Masks		14	17	20	11	12	13
Number of Masking layers		19	21	24	12	13	14
Number of Metal Layers		3	3	4	2	2	2
Number of Poly Layers		2	2	2	1	2	2
Substrate Type		p			p-		
Diffusion Pitch	µm	0,9			2,2		
Metal1/2/3/4 Pitch	µm	0.95 / 1.1 / 1.1 / 1.2			2.1 / 2.3 / - / -		
Metal1/2/3/4 conacted Pitch	µm	1.05 / 1.2 / 1.2 / 1.3			2.55 / 2.7 / - / -		
Poly1 Pitch	µm	0,8			1,7		
High Resistive Poly	kOhm/ #	-	-	1,2	-	-	1,2
Poly1/Poly2 Precision Caps	fF/µm²	0,9	0,9	0,9	-	0,9	0,9
N/PMOS Channel Length	µm	0.30/0.30			0.65 / 0.79		
N/PMOS Saturation Current	µA/µm	520 / 240			400 / 195		
Flip-Flop Delay	ns	0,8			1,4		
NAND2 Delay *)	ns	0,1			0,16		
NAND2 Area	µm²	54,6			516		
NAND2 Power	µW/MHz	2			5		

High Voltage Processes:
The 0.8µm high voltage process platform is optimized for complex mixed signal circuits up to 70V operating conditions. In addition to the standard CMOS transistors, a variety of high voltage transistors are available: HV-NMOS, -PMOS, -DMOS transistors, N-junction FETS, isolated NPN bipolar transistors, and isolated LV-NMOS transistors.
High voltage and standard devices can be easily combined into the same chip. Low power consumption and fast switching speed provide a wide range of applications in the automotive and industrial segments. Further applications are targeted towards high precision analog Frontends for sensors and transducers.
In combination with the proven 0.8µm mixed signal libraries the new process family represents the ideal solution for high voltage designs.

2.1.3.5.4 High Voltage Technology Selection Guide

Process Name	CXT	CXY	CXZ	H35A2IA	H35A3I0	H35B3A2	H35B3B2	H35B4D3	H35B4D7
Process features	2M,1P,S	2M,2P,S	2M,2P,HP,S	2M,1P	3M,1P,S	3M,2P,S	3M,2P,S,5V	4M,2P,S,5V,HP	4M,2P,S,5V,HP, FI, TM
number of masks	15	16	17	13	16	19	22	25	26
Design blocking voltage NMOSH [V]	50			50					
Absolute max. voltage NMOSH [V]	55			55					
Design blocking voltage PMOSH [V]	36, 40 for 20000s			50					
Absolute max. voltage PMOSH [V]	55			55					
specific R_on* NMOSH [Ohm mm^2]	0.34			0.13					
specific R_on* PMOSH [Ohm mm^2]	0.8			0.22					
Drawn LVMOS Channel Length, [µm]	0.8			0.35					
Operating voltage LV MOS[V] **	5V			3.3V , 5V					

2M.....2 metal layers
1P.....1 poly layer
2P.....2 poly layers
HP?..high resistive poly
S..?..substrate related LV devices
FI ?...Fully isolated NMOS
TM .... Thick Metal
5V??5V Logic

* the specific R_on is calculated from the minimum transistor source drain pitch. The value does not include design related substrate contacts or guard rings.

** Isolated LVMOS logic can be raised up to 50V Design blocking voltage

Applications:
Applications for the 12V Automotive Standard
Environment with High Voltage Spikes
Analog Frontends for Sensors & Transductors
Display Drivers & Industrial Markets

Description:
The High Voltage processes of austriamicrosystems are developed to fulfill the modern demands in high voltage products. The technology is based on a high voltage extension of the standard CMOS base process. This strategy provides a variety of high-voltage devices which are suitable for numerous design requirements. The process is realized by a low number of masks and alignments.

Key Features:
Two unrestricted layers of metal and two layers of poly for linear capacitors
Poly-to-poly capacitors (CXY, CXZ)
High resistive poly options (CXZ)
High voltage N and PMOS transistors with maximum VGS of 20.0V Documentation & Support

Design Rules & Process Parameters documents and simulation parameters are available at austriamicrosystems' technical web server http://asic.austriamicrosystems.com

BiCMOS and SiGe BiCMOS technologies:
The BiCMOS processes are optimized for high frequencies up to several Giga-Hertz. The applications cover circuits for mobile communication to high speed networks.
The latest introduction of a SiGe BiCMOS technology has considerably enhanced the competitive edge among international competition. These advanced processes offer high-speed bipolar-transistors with excellent analog performance, such as high fmax and low noise, complementary MOS transistors, very low-parasitic linear capacitors, linear resistors and spiral inductors.
The careful characterization and modeling of all active, passive, and parasitic devices of this process result in simulation models for different circuit simulators guaranteing the optimum use of these new processes.

2.1.3.5.5 0.35µm Technology Selection Guide

Process Name	units	S35D3H1	S35D4H2	S35D4H5	S35D3M2	S35D4M2	S35D4M5
Process Type		HV-SiGe BiCMOS			SiGe-BiCMOS		
Drawn MOS Channel Length, Drawn Emitter Width	µm µm	0.35 0.40			0.35 0.40		
Operating Voltage CMOS	V V	3.3/5	3.3	3.3/5	3.3	3.3	3.3/5
Number of Metal Layers		3	4	4	3	4	4
Number of Poly Layers		4	4	4	4	4	4
Substrate Type		p			p		
Diffusion Pitch	µm	0.9			0.9		
Metal1/2/3 Pitch	µm	0.95/1.1/1.2			0.95/1.1/1.2		
Poly1 Pitch	µm	0.8			0.8		
Thick Metal 4 pitch	µm	-	4.5	4.5	-	4.5	4.5
High Resistive Poly	kOhm/#	-	-	1.2	-	-	1.2
Poly1 / Poly2 Precision Caps	fF/µm²	0.9	0.9	0.9	0.9	0.9	0.9
Metal 2 / Metal 3 Precision Caps	fF/µm²	-	1.25	1.25	1.25	1.25	1.25
N/PMOS Active Channel Length	µm	0.30/0.30			0.30/0.30		
N/PMOS Saturation Current	µA/µm	540/240			540/240		
Gain	-	160			160		
Early Voltage VAF	V	100			100		
HS-HBT: BVceo	V	-	-	-	2.7	2.7	2.7
ft / fmax	GHz	-	-	-	60 / 70	60 / 70	60 / 70
HV-HBT: BVceo	V	5.5	5.5	5.5	-	-	5.5
ft / fmax	GHz	35 / 50	35 / 50	35 / 50	-	-	35 / 50

Multi Project Wafer:
The Multi Project Wafer (MPW) service is a low-price, fast prototyping service, which allows customers to share mask as well as wafer costs with other customers. The co-operation with organizations like MOSIS, Europractice, Fraunhofer-IIS and TIMA-CMP enables highest flexibility in this service. Currently the MPW program is offered from 0.8 µm to 0.35 µm processes including the following special technologies:

CMOS Mixed Signal, CMOS High Voltage (50 to 90 Volts), BiCMOS and SiGe-BiCMOS

The standard MPW service includes the delivery of 30 dice for design verification.

Packaged engineering samples are offered within 2 days (ceramic) and 3 weeks (plastics) cycle time, respectively. The total turnaround time from MPW deadline to delivery is app. 6 weeks (CMOS).

2.1.3.6 Filtronic (http://www.filtronic.com/)

Filtronic Compound Semiconductors (FCS) is a high volume, high yield 6" (150mm) wafer GaAs semiconductor manufacturing company. FCS produce an expanding and innovative line of pHEMT merchant RF devices.

In addition to merchant market products FCS also offer foundry services and are currently providing advanced solutions to a number of large OEMs. Considerable advantage can be obtained through the facility's economies of scale on the modern, state of the art wafer production line.

A true global division with engineering design and sales and marketing located in Santa Clara USA and Newton Aycliffe UK, FCS is able to provide fast response and support for customer requirements. The primary GaAs technology is pHEMT.

This division of Filtronic provides high volume discrete chips, packaged FETs, MMICs, and RF modules as well as customer specific foundry services.

FCS's manufacturing facility in Newton Aycliffe, County Durham, UK, is amongst the world's first and largest 6-inch wafer GaAs semiconductor operations.

Technology:
The 6-inch pHEMT process at the Durham facility can be categorized in the following capabilities:

- 6-inch GaAs substrate qualification
- MBE growth and characterization of 6-inch PHEMT wafers
- Stepper based 0.25 & 0.5 micron lithography
- Silicon nitride passivation and MIM capacitor
- TaN resistor
- Air bridge interconnect process
- Wafer grinding and chemical thinning processes
- RIE via hole process
- Wafer back-end, de-mounting, taping processes
- Die separation process
- Automated PCM and RF testing

Foundry Services:
In addition to merchant products FCS offer a comprehensive foundry service to its customers on both 0.50 micron and 0.25 micron processes. This service allows customers to gain considerable cost advantage for volume semiconductor manufacture.

Filtronic Compound Semiconductors is engaged in research and development and manufacture of III-V semiconductor components. The fabrication facility at Newton Aycliffe is committed to continual development of materials processes, models and circuits on the base of, D & E mode pHEMT GaAs.

Filtronic Semiconductor Division has successfully designed discrete's with fT up to 50 GHz and MMICs from 40 MHz to 30 GHz operating frequency.

Investment in state of the art technologies has been significant and on going in software, hardware tools and up to-the-minute measuring equipment all of which are critical to optimum product peformance.

Filtronic welcome enquiries from customers who have requirements in GaAs based compound Semiconductors.

Key Differentiators:

- Largest 6 inch GaAs Fab in Europe
- High Engineering Skills
- Strong R&D focus

Process Capabilities:
End to end process capabilities FCS provide

- In-house epitaxy layering utilising MBE
- 0.25mm and 0.5mm stepper lithography
- Full range of passive components including capacitors, resistors and inductors
- Through substrate vias
- On-wafer DC and RF testing available
- Support and development by internal Foundry Manual on both 0.25mm and 0.5mm processes

Applications:
GSM, DCS1800, PCS1900, IS95, UMTS Front-end
DECT, PHS, Bluetooth, Home-RF Front-end
ISM Receivers, Transmitters and Transceivers for: 868MHz, 915MHz, 2.4GHz, 5.6GHz
GPS, Glonass
Wireless LAN, Hyper LAN up to 5.6 GHz
ATM, Sonet, Fibre Channel Transceivers up 10-20Gb/s
Satellite Direct Receivers
Clock recovery circuits up to 10 GHz

Key Features:
S35D4M2 4P/4M SiGe BiCMOS Mixed Signal, RF, PIP+MIM, thick metal
S35D4M5 4P/4M SiGe BiCMOS Mixed Signal, RF, PIP+MIM, thick metal, HR poly, 5V periphery

Feature Sizes: 0.35µm gates / 0.40µm emitters
Supply Voltage: CMOS 3.3V; periphery up to 5.5V
Ft > 60 GHz, Fmax > 70 GHz
Bvceo > 2V

Description:
austriamicrosystems 0.35µm SiGe-BiCMOS process is based on the proven 0.35µm mixed-signal CMOS process and includes an additional high performance analog oriented SiGe HBT transistor module. This advanced RF-process offers high-speed HBT-transistors with excellent analog performance such as high fmax and low noise as well as complementary MOS transistors with the option of 5V I/O CMOS transistors. Accurately modeled high linear precision capacitors are available as Poly1 / Poly2 or Metal2 / Metal3 versions. The modular integration of linear resistors, high quality varactors and thick Metal 4 spiral inductors makes this process ideally suitable for a wide range of high performance RF applications up to 20 Gb/s.

Design Kits and Product Evaluation:
Upon request, *austria**micro**systems* provides design kits consisting of library elements, component models, process-specific parameters, and interface programs for CAD software to foundry customers who develop their own chips. Furthermore, specific product evaluation in a state-of-the-art lab is offered.

Design Support:
Service is the company's highest priority. austriamicrosystems can provide cell libraries for various technologies, and supports its customers with geometrical design data, simulation models, as well as with extensive documentation.

Based on state-of-the art design software provided by various software vendors, austriamicrosystems offers a comprehensive process design kit called HIT-Kit.

The HIT-Kit enables product developers to concentrate on **IC design** rather than on setting up and mastering the EDA enviroment. This leads the Partners to:

- Shorter Time to Market
- Complete Environment for First Time Right Designs
- More Efficient Designs (Die Size, Performance, Yield)

The Advantages and Benefits of the HIT-Kit are:

- All major EDA tools supported
- All process technologies supported with latest versions of EDA tools
- "Plug and Play" for IC designers
- All devices supported throughout the whole design flow
- Complete modeling of active and passive devices
- Supports complete flow for RF and mixed signal (devices, models, libaries,...)
- Full mixed-signal library concept: digital, analog, special libraries (for noise sensitive applications)
- HIT-Kit is fully comliant with the QS9000 quality flow and well tracked with release control, patches and customer interface system
- HIT-Kit developers provide technical support

Libraries for schematic capture, logic and circuit simulation can be provided for tools from a wide variety of software vendors.

2.1.3.6.1 BiCMOS Technology Selection Guide, 0.8µm

Process Name	units	BYB	BYE	BYQ	BYS	BYR
Process Type		BiCMOS			SiGe-BiCMOS	
Drawn MOS Channel Length, Drawn Emitter Width	µm µm	0.8 0.8			0.8 0.8	
CMOS Operating Voltage	V	5.5			5.5	
Number of Masks		15	16	17	18	19
Number of masking layers		19	20	21	22	23
Number of Metal Layers		2			2	2
Number of Poly Layers		2			3	3
Substrate Type		p			p	
Diffusion Pitch	µm	3.8			3.8	
Metal1/2/3 Pitch	µm	2.4/2.8/-			2.4/2.8/-	
Poly1 Pitch	µm	1.8			1.8	
Thick Metal 4 pitch	µm				-	
High Resistive Poly	kOhm/#	-	-	1.2	-	1.2
Poly1/Poly2 Precision Caps	fF/µm²	-	1.8	1.8	1.8	1.8
Metal 2 / Metal 3 Precision Caps	fF/µm²	-	-	-	-	-
N/PMOS Channel Length	µm	0.66/0.75			0.66/0.75	
N/PMOS Saturation Current	µA/µm	420/200			420/200	
HV HBT		> 6.0			> 3.0	
Bvceo	V	> 6.0			> 3.0	
Gain		100			100	
Transit Frequency	GHz	12			35	
Maximum Oscillation Freq. Fmax	GHz	14			40	

2.1.3.6.2 0.8µm BiCMOS Process Technology

Applications:
fast mixed signal circuits
ATM up to 1.24 GBit/s, wireless communication up to 2.4 GHz
high speed AD/DA converters up to 200 MHz

Description:
The austriamicrosystems BiCMOS process is based on the proven 0.8 µm analog CMOS process and includes an additional high performance analog oriented bipolar module providing mixed signal ECL, BiCMOS, and CMOS design capabilities.

Key Features:

- 0.8 µm CMOS Si-Gate process technology with poly emitter 12 GHz bipolar module
- Two unrestricted layers of metal and two layers of poly for linear capacitors
- Poly-to-poly capacitors (BYE, BYQ), High resistive poly options (BYQ)
- Optimized for RF applications
- ECL, CML, BiCMOS and CMOS cell library
- Full swing BiCMOS outputs allow unrestricted mix of CMOS and BiCMOS core cells
- ECL, TTL and CMOS interfacing capability

- Peripheral cells with high driving capability
- Fully differential ECL/CML cell variants for noise immunity
- High performance mixed signal capabilities
- IEEE 1149.1 boundary scan macros/cells

Key Spezification:
BYB 2.5-5.5V p-sub, 2-metal, 2-poly
BYE 2.5-5.5V p-sub, 2-metal, 2-poly, poly-poly capacitors
BYQ 2.5-5.5V p-sub, 2-metal, 2-poly, poly-poly capacitors, hr-poly

2.1.3.6.3 0.8µm SiGe-BiCMOS Process Technology

Applications:
GSM, DCS1800, PCS1900, IS95, UMTS Front-end
DECT, PHS, Bluetooth, Home-RF Front-end
ISM Receivers, Transmitters and Transceivers for: 868MHz, 915MHz, 2.4GHz, 5.6GHz
GPS, Glonass
Wireless LAN, Hyper LAN
ATM, Sonet, Fibre Channel Transceivers
Satellite Direct Receivers
Low Voltage (< 1V) Radios

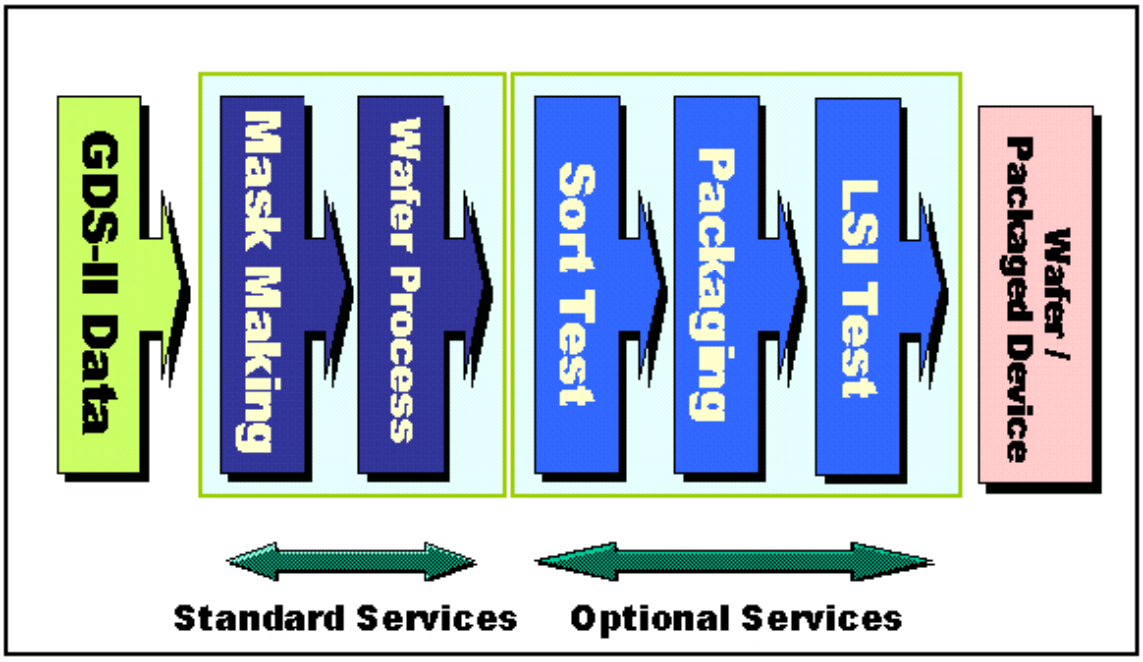
Description:
austriamicrosystems Silicon-Germanium HBT-CMOS process is based on the proven 0.8 µm mixed-signal CMOS process and includes an additional high performance analog oriented heterojunction-bipolar-transistor module. This advanced process offers high-speed npn-transistors with excellent analog performance such as high fmax and low noise, complementary MOS transistors, very low-parasitic linear capacitors, linear resistors, and spiral inductors.

Key Features:
BYS 2.5-5.5V p-sub, 2-metal, 3-poly
BYR 2.5-5.5V p-sub, 2-metal, 3-poly, hr-poly
Feature Sizes: 0.8 µm gates/emitters
Supply Voltage: up to 5.5V
rb = 500 Ohm µ
Ft = 35 GHz, Fmax= 40 GHz
BVceo> 3V

2.1.3.7 Fujitsu (http://www.fujitsumicro.com/)

FUJITSU offers "mask making" and "wafer processing" as standard services, and "wafer sort", "packaging" and "LSI testing" as optional services.

A multi-project wafer service called SiExpressTM to minimize customers' pre-production sample costs is provided.



Technologies:

FUJITSU provides customers with state-of-the-art 90nm node CMOS technology in addition to well-established 0.35um / 0.25um / 0.18um / 0.11um mixed-signal and pure CMOS technologies. Copper wiring together with expertise based on experience is available with 0.13um / 90nm node CMOS technologies.

Some application-specific process technologies such as backplane LSI for liquid crystal on silicon (LCOS), microdisplays, and CMOS image sensors are also available.

- High-end CMOS (130nm node or less)
- CMOS
- CMOS High-voltage
- Liquid Crystal On Silicon (LCOS)
- CMOS image sensor
- Micro Electro Mechanical System (MEMS)

In order to provide state-of-the-art CMOS technologies, technical difficulties that have never before been encountered have to be faced and solved. Such difficulties include not only microfabrication technology at the gate but also Cu wiring with low-k film technology. Few companies in the world bring out products that use Cu wiring + low-k film technology.

FUJITSU has established its expertise in copper wiring + low-k film technology at an early stage. The Cu wiring technology applies to 180 nm node CMOS products and newer products. Because of this experience, a distinction over other competitors in the development of mass production technology for 90nm node CMOS has been achieved.

FUJITSU supports greater business opportunities for customers by offering state-of-the-art technologies.

- CS100A (90nm node)
- CS90A (130nm node)

High-end CMOS technologies - key features:

Technology (node)		CS100A (90nm)	CS90A (130nm)
Physical Gate Length (nm)		60/80	110
Supply Voltage (V)		1.0/1.2	1.2
Available Interface (V)		1.2/2.5	1.2/2.5/3.3
Available Poly/Metal Layers		1P10M	1P8M
Substrate		P-sub	P-sub
Mixed-Signal	Triple-well	Yes	Yes
	Diffusion Resistor	Yes	Yes
	Capacitor	Metal-Metal*2 and Bulk-Poly	
Mass Production Availability		2003.3Q	Now

*1: No limitation in the combination of the Mixed-Signal Options.

*2: Metal-Metal Capacitor being planned.

2.1.3.7.1 SiExpress™

Silicon Express™ is a pre-production service where customers save costs by sharing MASK sets and wafer, called multi-project-wafer. High-quality, consistent samples, because Silicon Express™ uses the same process as that for the ASIC products can be supplied. FUJITSU can provide customers with a packaged sample on request.

SiExpress™ service information:

Process	Metal	I/O	Analog Option
CMOS 130nm node (CS90A)	8 Metal	1.2V/3.3V	yes
CMOS 0.18um	5 Metal	1.8/3.3V	yes
CMOS 0.25um	4 Metal	2.5V/3.3V	yes

2.1.3.7.2 CMOS Technologies

The main characteristics of the standard CMOS technologies are outlined below.

CMOS technologies - key features

Technology		0.18 um	0.25 um	0.35 um	0.50 um
Supply Voltage (V)		1.8	2.5	3.3	3.3*2
Available Interface (V)		1.8/2.5/3.3	2.5/3.3	3.3/5.0	3.3/5.0
Available Poly/Metal Layers		2P6M*1	2P5M	2P4M	2P4M
Substrate		P-sub	P-sub	P-sub	P-sub
Mixed-Signal Options*3	Triple-well	Yes	Yes	Yes	No
	Diffusion Resistor	Yes	Yes	Yes	Yes
	Capacitor	Poly-Poly & Bulk-Poly	Poly-Poly	Poly-Poly & Bulk-Poly	Bulk-Poly
Mass Production Availability		Now	Now	Now	Now

*1: "2P6M" means Poly 2 Layers + Metal 6 Layers.
*2: Please contact us, before using the 0.50um technology at 5 V.
*3: No limitation in the combination of Mixed-Signal Option.

2.1.3.7.3 CMOS High-voltage

FUJITSU offers CMOS High-voltage technologies for a variety of drivers (LCD, Organic EL, etc.).
The main characteristics of the CMOS High-voltage technologies are outlined below.

CMOS High-voltage technologies - key features

Technology	0.25 um		0.35 um		0.50 um	0.65 um	
Logic Voltage (V)	2.5		3.3		3.3	5.0	
High-voltage (V)	32V 40V	12V 18V 25V	40V	12v 18V 25V 32V	12v	25V	20V
Available Poly/Metal Layers	2P5M		2P4M		1P3M	1P2M	
Capacitor*1	Bulk-Poly /Poly-Poly		Bulk-Poly /Poly-Poly		Bulk-Poly	-	
Resistor*1	Diffusion /Poly resistor		Diffusion /Poly resistor		Diffusion resistor	-	
Data Acceptable	August 2003	June 2003	June 2003	Now	Now	March 2003	Now

*1: The "Capacitor" and "Resistor" items are options.

2.1.3.7.4 CS90A (130nm Node) Technology

Features

1-Poly and 8-Metal(7Cu + 1Al)
Retrogate Twin Wells on P-Epi Substrate
Shallow Trench Isolation (STI)
Salicide Gate
Salicide Source and Drain

CMP Planarization
Dual Damascene Cu
SiO_2 & Low-k Interlayer Dielectric
Stackable Contact and Vias
Oxide/Nitride Passivation

Mask Data Acceptance: Now
Production availability: Now

Process Parameters and Transistor Characteristics

	UHS	HS	ST	LL
Gate Length (Printed)	140 nm	140 nm	140 nm	140 nm
Gate Length (Physical)	110 nm	110 nm	110 nm	110 nm
Gate Oxide (Electrical)	2.9 nm	2.9 nm	2.9 nm	2.9 nm
VDD (V)	1.2	1.2	1.2	1.2
Ids_Nch (μA/μm)	780	678	570	390
Ids_Pch (μA/μm)	-321	-276	-218	-150
Ioff_Nch (nA/μm)	36	4.2	0.18	0.005
Ioff_Pch (nA/μm)	-18	-3.1	-0.22	-0.015
Ig (nA/μm)	0.01	0.01	0.01	0.01
Gate Delay (ps)	14	17	28	45

2.1.3.7.5 CS100A (90nm Node) Technology

Features

1-Poly and 10-Metal(9Cu + 1Al)
Retrogate Twin Wells on P-Epi Substrate
Shallow Trench Isolation (STI)
Salicide Gate
Salicide Source and Drain

CMP Planarization
Dual Damascene Cu
Full Low-k Interlayer Dielectric
Stackable Contact and Vias
Oxide/Nitride Passivation

Mask Data Acceptance: Now
Production availability: 2003.3Q

[1]

Process Parameters and Transistor Characteristics (LL Type)

	UHS	HS	LL
Gate Length (Printed)	100 nm	100 nm	100 nm
Gate Length (Physical)	80 nm	80 nm	80 nm
Gate Oxide (Electrical)	2.9 nm	2.9 nm	2.9 nm
VDD (V)	1.2	1.2	1.2
Ids_Nch (μA/μm)	820	715	450
Ids_Pch (μA/μm)	-395	-320	-200
Ioff_Nch (nA/μm)	30	3.0	0.01
Ioff_Pch (nA/μm)	-30	-3.0	-0.01
Ig (nA/μm)	0.01	0.01	0.01
Gate Delay (ps)	11	13	22

Process Parameters and Transistor Characteristics (G Type)

	UHS	HS	ST
Gate Length (Printed)	100 nm	100 nm	100 nm
Gate Length (Physical)	60 nm	60 nm	60 nm
Gate Oxide (Electrical)	2.2 nm	2.2 nm	2.2 nm
VDD (V)	1.0	1.0	1.0
Ids_Nch (μA/μm)	740	630	480
Ids_Pch (μA/μm)	-330	-280	-200
Ioff_Nch (nA/μm)	30	5.0	0.5
Ioff_Pch (nA/μm)	-30	-5.0	-0.5
Ig (nA/μm)	0.5	0.5	0.5
Gate Delay (ps)	<10	<13	<20

Process Parameters and Transistor Characteristics (HP Type)

	HS	ST
Gate Length (Printed)	100 nm	100 nm
Gate Length (Physical)	60 nm	60 nm
Gate Oxide (Electrical)	1.9 nm	1.9 nm
VDD (V)	1.0	1.0
Ids_Nch (μA/μm)	910	640
Ids_Pch (μA/μm)	-410	-260
Ioff_Nch (nA/μm)	50	1.0
Ioff_Pch (nA/μm)	-50	-2.0
Ig (nA/μm)	50	50
Gate Delay (ps)	9	11

2.1.3.8 IBM Microelectronic (http://www.ibm.com/chips/)

Technologies:
Demonstrating industry leadership and commitment to customers, IBM offers a range of leading-edge and industry-standard CMOS, RF CMOS, and silicon germanium BiCMOS process technologies ranging in transistor size from 0.5-µm to 90-nm.

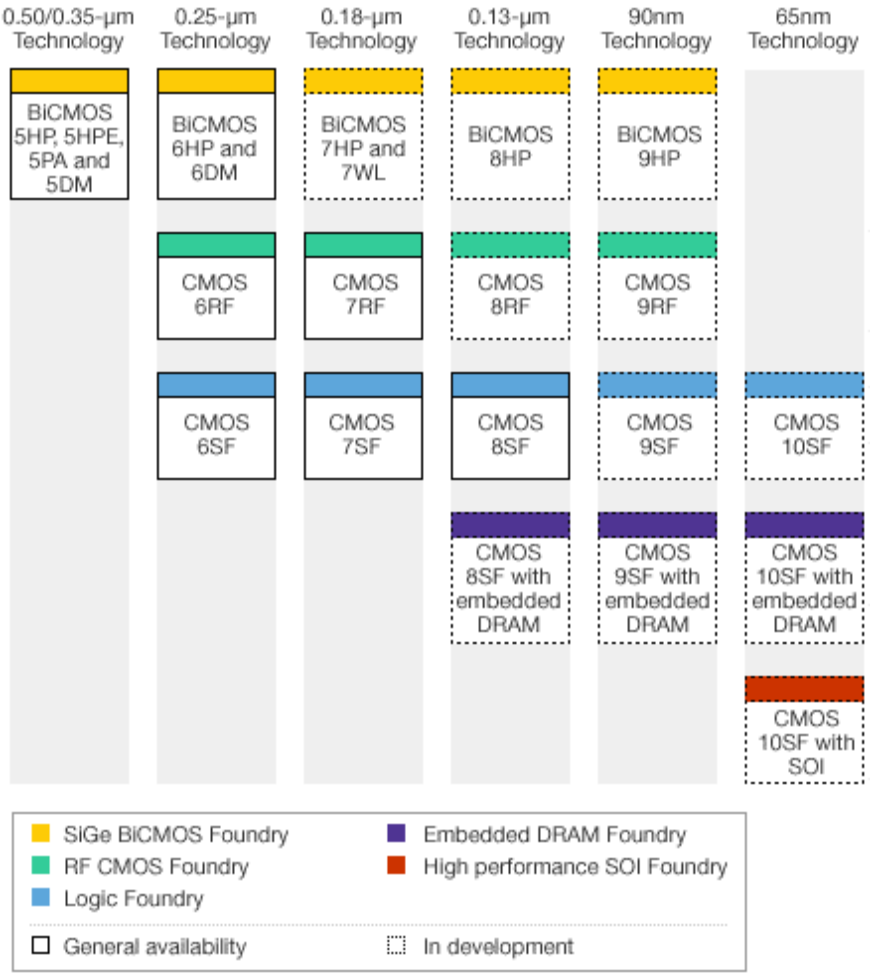
With over 1000 microelectronic patents in 2002 alone, IBM has an unsurpassed track record of sustained innovation. IBM is adept at integrating new materials, devices and design methodologies and consistently deliver technological advancements to the market ahead of the competition - and offer you one of the most diverse offering portfolios in the industry.

CMOS technology:
IBM offers technology advancements like copper interconnects and silicon-on-insulator (SOI) to differentiate their products.

SiGe BiCMOS technology:
Invented by IBM, Silicon Germanium (SiGe) technology provides high performance with low noise and low power.

RF CMOS technology:
High frequency efficiency in a low cost solution.

Foundry roadmap:
IBM's technology roadmap provides a path for ongoing innovation.



2.1.3.8.1 CMOS

In applications for home, business and everywhere in between, IBM continues to be the first to provide semiconductor technology advancements like copper interconnects and silicon-on-insulator (SOI) to differentiate their products in the market.

IBM has a long-standing commitment to the semiconductor industry with its standard CMOS technology supported by experienced engineering teams to help decrease overall product time-to-market and manufacturing risks. The broad spectrum of offerings and advanced capabilities offer diverse options for a complete turn-key solution.

CMOS technologies:
130 nm CMOS technology (CMOS 8SFG)
180 nm CMOS technology (CMOS 7SF)
250 nm CMOS technology (CMOS 6SF)

2.1.3.8.2 RF CMOS

High frequency efficiency in a low-cost solution
IBM's proven CMOS technology and suite of industry-leading analog passive devices merge into a technology that provides you with the wireless performance you need in a cost-effective solution. RF CMOS is making its way into products such as low function wireless LANs, pagers, cordless phones and RF identification tags.

RF CMOS technology:
130 nm RF CMOS technology (CMOS 8RF)
180 nm RF CMOS technology (CMOS 7RF)
250 nm RF CMOS technology (CMOS 6RF)

2.1.3.8.3 SiGe BiCMOS

IBM's Silicon Germanium (SiGe) BiCMOS technologies offer peak performance for applications requiring high transfer of data, low noise, high linearity and low power consumption such as wireless devices, multi-action mobile telephone systems, and optical networking components. The heart of IBM's SiGe technology is an heterojunction bipolar transistor (HBT) doped with germanium to increase electron transfer. This high-performance material is manufactured using conventional silicon CMOS production tooling, allowing high integration of functions and enabling smaller chip size.

180 nm technologies:
BiCMOS 7HP: A SiGe technology with very high performance devices optimized for high performance applications such as high frequency wireless and optical. **BiCMOS 7WL**: A SiGe technology optimized for mainstream wireless applications - having good performance and lower cost.

250 nm technologies:
BiCMOS 6HP: A unique and versatile process integrating a 47-GHz high-performance, SiGe HBT with a 2.5-V CMOS base offers high performance transistors with low power consumption.

350 nm technologies:
BiCMOS 5HPE: A SiGe technology which integrates a high-speed, 43-Ghz SiGe HBT with a 3.3/5.0-V CMOS base offers high performance transistors with low power consumption.

500 nm technologies:
BiCMOS 5HP: A SiGe technology which integrates a high-performance SiGe HBT with a 3.3 V CMOS base.

BiCMOS 5PA: A SiGe technology which integrates a high-performance SiGe HBT with a 3.3 V CMOS base optimized for applications requiring high voltage capability and high linearity such as power amplifier designs.

BiCMOS 5DM: A SiGe technology which integrates a high-performance SiGe HBT with a 3.3 V CMOS base. This dual metal technology offers increased inductor and capacitor density which is ideal for designs with high proportion of passive elements.

BiCMOS

Key technology specifications

	5HP/AM/DM	5PA	5HPE	6HP	7HP	7WL
Isolation:	STI/DT	STI/DT	STI	STI/DT	STI/DT	STI/DT
HP fT/fMAX (GHz)**:**	51.5	51.5/65	43/45	47/65	120/100	60/85
HB fT/fMAX (GHz)**:**	29/50	23/50	19/35	27/50	30/50	45/73
HP BVceo (V)**:**	3.3	3.3	3.3	3.3	1.8	3.3
HB BVceo (V)**:**	5.5	7	9.6	5.7	4.2	6.0
Min. WE Drawn (µm)**:**	0.5	0.5	0.32	0.32	0.2	0.24
CMOS generation	5S0	5S0	5SF	6SF	7SF	7SF
CMOS Lg drawn (µm)**:**	0.5	0.5	0.4	0.25	0.18	0.18
CMOS supply (V)**:**	3.3	3.3	5.0,3.3	2.5,3.3	1.8,3.3	1.8,3.3
BEOL metal type:	Al	Al	Al	Al	Cu+Al	Cu+Al
M1 current density:	1×	1×	1.16×	0.89×	1.24×	1.24×
Masks FEOL/BEOL:	24/8	24/8	18/7	22/7	22/9	15/7
RPT (days) **3LM:**	24.8	24.8	17.7	23.9	25	15.1

2.1.3.9 IHP (http://www.ihp-ffo.de/)

Multiproject Wafer (MPW) & Prototyping Service:
IHP provides to customers and partners access to four SiGe:C BiCMOS technologies (SGC25A, B, C and SGB25VD) as described below. Runs start on a regular basis.

A cadence mixed signal design kit is available. Additionally, IHP's reusable blocks and IPs for wireless and broadband can support customer designs.

IHP technologies available for Multiproject Wafer & Prototyping Service:

2.1.3.9.1 0.25 µm SiGe:C BiCMOS (SGC25A)

Parameter	High Performance	High Voltage
Bipolar Section		
A_E	0.42 x 0.84 μm^2	
Peak f_{max}	100 GHz	90 GHz
Peak f_T	80 GHz	50 GHz
BV_{CE0}	2.4 V	3.2 V
V_A	>50 V	
ß	150	
CMOS Section (0.25 µm)		
Core Supply Voltage	2.5 V	
nMOS V_{th}	0.60 V	
nMOS I_{Dsat}	540 µA/µm	
nMOS I_{off}	3 pA/µm	
pMOS V_{th}	-0.56 V	
pMOS I_{Dsat}	230 µA/µm	
pMOS I_{off}	3 pA/µm	
Passives		
MIM Capacitor	1 $fF/\mu m^2$	
N^+ Poly Resistor	95 Ω/[]	
HBT Poly Resistor	370 Ω/[]	
Varactor C_{max}/C_{min}	3	
Inductor Q@2.4 GHz	12 (1 nH), 6 (15 nH)	
Inductor Q@5.8 GHz	16 (1 nH), 10 (2 nH)	

2.1.3.9.2 0.25µm baseline CMOS Process

Key process features:

15 mask levels (7 DUV, 8 I-Line)
Shallow trench isolation
5 nm gate oxide
n- and p- surface channel devices
Cobalt salicide
Local interconnect
3 level Al metal
Oxide and tungsten CMP
Advanced passivation stack
"Copy exactly" from Motorola

Design rules:

Design rule	Pitch (µm)
NWELL	3.15
ACTIVE	0.875
GATE	0.63
LI	0.77
METAL 1	0.77
METAL 2/3	0.845

Process parameter:

Parameter	NMOS	PMOS	Remark
Short channel Vt	0.60 V	-0.55	@Vd=0.1V
Long Channel Vt	0.62 V	-0.61	@Vd=0.1V
Effective channel length	0.235 µm	0.245	
Saturation current IDS	540 µA/µm	-230 µA/µm	@Vd=2.5V
Saturation current IDS	310 µA/µm	-120 µA/µm	@Vd=1.8V
Leakage current	<1pA/µm	<0.2 pA/µm	@Vd=2.5V
Sheet-rho salicide	5.5 Ohm/sq	6 Ohm/sq	@min wpoly

2.1.3.9.3 0.25µm SiGe:C BiCMOS Process

Key process features:

4 Metal layers including 2µm thick inductor metal
Isolated NMOS devices
MIM capacitors
Linear Resistors

Target bipolar parameters

Parameter	Name	Value	Remark
Intrinsic base sheet rho	Rs_{bi}	1.3kOhm/sq	
Current gain	ß	200	@V_{BE}=0.7V
Early voltage	V_A	90 V	@I_B~5nA,V_{CE}~1.2V
Emitter-Col breakdown	BV_{CEO}	3.2 V	@I_C<2mA
Peak transit frequency	f_t	50 GHz	@V_{CE}=2V
Peak maximum osc. frequency	f_{max}	90 GHz	@V_{CE}=2V
Low current f_t	f_t	10 GHz	@I_C=10µA
Minimum noise figure	NF_{min}	2 dB	@12 GHz

Integration flow

5 nm gate oxide	
Gate poly deposition	Deposition of Oxide/Nitride protection layer stack
Gate patterning	***1st mask:*** Removing protection layers from HBT regions + high energy well implantation
Spacer formation	***2nd mask:*** Defining poly-emitter windows
NMOS S/D implantation	Depositing in-situ As doped silicon
NMOS drive	***3th mask:*** Structuring emitters
_	Self aligned external base implantation
PMOS S/D implantation	***4th mask:*** Structuring external base regions
S/D drive	Wet protection layers removal
resistor formation	
Salicidation	

2.1.3.9.4 0.25µm SiGe:C BiCMOS Process

modules for wireless communication

Process Modules	**Masking steps required**
Digital Base Process	15
SiGe:C Bipolar Module	4-5
Dual BV_{CEO}	0-1
Signal Isolation (Deep Trench)	1
Dual V_t (low leak, or high speed)	2
Dual Vdd (3.3 or 5V)	1-2
Linear Resistors	1-2
Linear Capacities (MIM)	1
High Q Inductors	0-1

2.1.3.10 MicroFab (http://www.microfab.com/)

Technologies:

1 surface micromachining
2 bulk micromachining
3 silicon deep etching (DRIE, Bosch process)
4 electro plating

2.1.3.10.1 Photolithography

microFAB Bremen GmbH's photolithography department is located in a class 10 clean room cell. Several positive photoresist systems in the thickness range between 1.1 and 60 µm are available. One Dai-Nippon track system and two Convac spinners are set up for resist coating. All layouts are on 5 or 7 inch chrome-on-glass masks.

Two SUSS mask aligners (MA150, MA6) and two Electronic Vision (AL6, AL4) mask aligners are available for alignment & exposure. Backside alignment (± 2 µm overlay accuracy) is possible. The maximum resolution of 0.8 µm (lines/spaces) is achived with a 1.1 µm AZ1518 positive resist. Resist developement is done on the Dainippon track system or the Convact tools.Thick positive resist (AZ4562) is used for microform application with thicknesses of 20, 30, 40, and 60 µm and aspect ratios of up to 6:1.

2.1.3.10.2 Dry etching

Dry etching techniques (RIE, ion beam and plasma etching) are intensively used at microFAB for patterning of dielectrics, polysilicon and metal layers. Further important applications are the photoresist stripping and the anisotropic deep silicon trench etching.
State-of-the-art monochromatic end point detection is applied with most RIE processes, ensuring a minimum of substrate loss due to overetching. Various etch masks (photoresist, SiO2, Ti, Cr, plasmanitride) can be combined, depending on the materials to be etched.

All processes were optimized regarding troughput, etch rate selectivity toward mask and substrate, CD loss (undercut), and etch profile (taper).

At the present time, microFAB operates 8 dry etching systems of which there are 2 RIE systems (STS multiplex and Alcatel 601E) for dielectrics and metal etch, 1 ICP mode RIE system (STS multiplex) for deep silicon trench etching, 1 physical ion beam etcher (STS 340 PC) for noble metal etch, and 4 plasma etchers for resist strip processes (2 downstream MTI-Afterglo and 2 Tepla barrel type etchers).

There are several standard processes available:

- RIE/ICP deep silicon trench etching (ASE process, up to 300 µm, aspect ratio 50:1)
- anisotropic RIE of dielectric layers (SiO_2, Si_3N_4, Si:ON), up to 2000 nm
- anisotropic RIE of polysilicon (up to 2000 nm)
- isotropic RIE of polysilicon (up to 2000 nm)
- anisotropic RIE of Al and AlSiTi metal layers (up to 3000 nm)
- anisotropic RIE of bulk mono silicon (up to 5000 nm)
- isotropic RIE of Cr, Ti and WTi10 metal layers (up to 500 nm)
- anisotropic ion beam etching of Au and Pt layers (up to 500 nm)
- anisotropic RIE of polyimide and photoresist (up to 10 µm)
- isotropic strip of photoresist (up to 100 µm)

2.1.3.10.3 Wet etching

Wet chemical etching is commonly used for uniform stripping or patterning through a mask of dielectric and metallization layers. In contrast to RIE all processes are more or less isotropic and mask underetching is present. Selectivities toward mask and substrate materials are usually much better than with RIE processes. Another special wet etching process used in bulk micromaching technology is the anisotropic, crystal-oriented, KOH or TMAH etch. Standard RCA process (SC1, SC2, HF-dip) is used for wafer cleaning. Special Solvent bathes are available for resist stripping. All standard etch bathes are SPC controlled (etch rate monitoring).

The following standard processes are available:

- BOE (buffered oxide etch, NH4F/HF/H2O)
  Used for etching of thermal oxide, LPCVD oxide (LTO), PECVD oxide, and PECVD. Patterning can be done using a positive AZ resist of 1.2, 1.8 or 6.5 µm thickness.
- TMAH and KOH silicon etch
  Used for crystal oriented anisotropic etching of mono silicon. Thermal oxide or LPCVD nitride masks are commonly used for patterning
- HF-dip
  Used for etching of thin silicon oxide (gate oxides, native oxide layers)
- Phosphoric acid (H3PO4)
  Used for uniform stripping of silicon nitride layers (LPCVD nitride/LOCOS process, PECVD nitrides).
- Aluminum etch
  A special mixture of acids is in use for etching of aluminum layers (e.g., interconnection lines)
- Polysilicon etch
  A mixture of HF and HNO3 is in use for isotropic etching of polysilicon layers
- Special etch application
  There are many further reagents in use for etching of metal layers (Au, Cr, Ni, Cu, Ti).

2.1.3.10.4 Deep reactive ion etching - DRIE

DRIE is a high aspect ratio, deep trench silicon etching process. The principle of the deep trench silicon etching process is an alternating fluorine based etching and passivation of the structures. This results in sidewall profiles of 90°±1° with aspect ratios of up to 40:1. Masking layers can be made of photo resist or silicon oxide.

The main benefits of the DRIE are:

- etch rate of up to 6 µm/min
- aspect ratio up to 40:1
- selectivity to positive resist > 75:1
- selectivity to silicon oxide >150:1
- etch depth capability 10 to 550 µm (through wafer etching)
- sidewall profile 90°±1°
- feature size 1 to >500 µm

Alcatel's deep plasma etch technology is designed to deliver superior process performance and maximum process flexibility to meet the needs of a broad range of deep silicon etch applications.

- Applications in MEMS and microsystems fabrication include:
- high aspect ratios, etch depths of as great as 500 µm, etching through-the-wafer, etching into a buried cavity in the wafer, or etching onto buried oxide.
- Applications in deep trench isolation include:
- etching bulk silicon or silicon-on-insulator structures with vertical or positive profiles with very high etch rates for high throughput.

2.1.3.11 Northrop (http://www.es.northropgrumman.com/es/atc/)

Gallium Arsenide Capabilities
Using MESFET, PHEMT and HBT transistor technologies, Northrop Grumman has developed a family of GaAs MMIC products focused on power generation for radar, missile guidance and communications applications. The MESFET process uses 0.4 µm electron beam defined gates for moderate performance requirements up to 18 GHz.

In addition to power, the process is used for the fabrication of digital phase shifters and attenuators. The PHEMT process features 0.25 µm T-gates and has been used primarily for mm-wave power generation.

The HBT process is based on the GaAs/AlGaAs materials system and has optically defined 2.0 µm emitters. It was designed to address high yield, high efficiency requirements in X and Ku-band.

Future upgrades will reduce the gate length of the PHEMT process to 0.1 µm to extend frequency coverage to W-band. Similarly, critical dimensions in the HBT process will be reduced to extend the applicability of this process to 35 GHz. The process will also be migrated to the GaAs/InGaP materials system for improved reliability.

Foundry Services
Northrop Grumman provides a complete foundry service for Gallium Arsenide (GaAs) power amplifiers and control circuits within the 1-40 GHz range. The standard FET/HEMT service uses 4-inch GaAs wafers with MBE epitaxial layers and either 0.25 or 0.5? gates generated with E-beam. This ensures quality amplifiers with state-of-the-art power and efficiency. HBT standard service is also available.

Proven Quality and Reliability
Customer-designed amplifiers and circuits are processed in the same cleanroom facility used to produce Northrop Grumman's system devices. This leading edge facility provides complete on-wafer DC and RF test capability.

Northrop Grumman pioneered on-wafer power measurements of MMICs. All fabricated MMICs can be completely evaluated at the wafer level to provide known good die.

Northrop Grumman's foundry process achieves maximum quality and reliability by providing:

- Device uniformity through the use of MBE GaAs material with stringently controlled doping
- MIMIC program-qualified process line
- E-beam written gates for consistent performance
- Double-recessed gates for state-of-the-art RF power performance
- SiN passivation
- Proven production history

2.1.3.11.1 0.25 µm PHEMT Features

- f_T= 40 GHz
- Low noise
- Efficient RF power
- High gain
- Low DC power
- Direct-write E-beam gates, 0.25?µm T-gate
- 5x stepper lithography for all other levels
- MBE, 4 inch wafers
- Profile: double heterostructure, superlattice buffer
- Channel structure: wet etched; double recess; InGaAs channel
- Substrate thickness: 4 mils
- MIM capacitors/passivation: Silicon nitride
- Two-level metal with 3?µm thick airbridge plating
- Overlay metal is 2?µm thick; plating is 3?µm thick; bias lines can be 5?µm thick
- Resistors: TiPt; active layer

0.25 µm PHEMT Performance Characteristics

- 30% PAE; 0.2 Watt: 6 dB assoc. gain; 0.5 mm at 30 GHz; 50% Idss bias point; Idss 350 mA/mm; Imax 600 mA/mm; Vpinchoff 1.2V; BVDGO 10V (11V typ); VDS 5V

2.1.3.11.2 HBT Features

- f_T= 40 GHz, Vce 2V
- f_T=26 GHz, Vce 7V
- Highest linearity
- Lowest phase noise
- Low DC power
- Analog/digital integration
- Highest efficiency
- Very high circuit density
- 5x stepper lithography for all levels (I-line, 0.6?µm resolution)
- MOCVD, 4-inch wafers
- Carbon-doped base, 4 x 1019cm-3, 1000 Ang thick
- Non-self-aligned process; higher Beta, lower 1/f noise than a self-aligned process
- Thermal shunt cell design; lowers thermal resistance by 40%
- Substrate thickness: 4 mils
- MIM capacitors/passivation: Silicon nitride

- Two-level metal airbridges; airbridge plating is 6?µm thick
- Overlay metal is 2?µm thick; plating is 6?µm thick; bias lines can be 8?µm thick
- Resistor: TiPt

HBT Performance Characteristics

- 55% PAE; 0.5 Watt; 9 dB assoc. gain at X-band: 2?µm x 20?µm x 12?µm
- Class B operation where the operating current is four times the quiescent current
- Two processes: Vce 7V, Bvceo 15V; Vce 9V, Bvceo 20V
- Larger devices at lower frequencies such as C-band grow in overall length not width

2.1.3.11.3 MESFET Features

- Direct-write E-beam gates, 0.5 µm
- 5x stepper lithography for all other levels
- MBE, 4-inch wafers
- Profile: spike doped with superlattice buffer
- Channel structure: wet etched, double recess substrate thickness: 4 mils
- MIM capacitors/passivation: silicon nitride
- Two-level metal with airbridges; airbridge plating is 3?µm thick
- Overlay metal is 2?µm thick; plating is 3??µm thick; bias lines can be 5??µm thick
- Resistors: TiPt; active layer

MESFET Performance Characteristics

- 45% PAE; 1 Watt; 9 dB assoc. gain; 2.2 mm at X-Band; 20% Idss bias point
- Idss 225 mA/mm; BVDGO 19V (20.5V typ.); Vpinchoff 2.2V; VDS 9V

2.1.3.12 Tronics (http://www.tronics-mst.com/)

2.1.3.12.1 Bulk Micromachining

TRONIC'S Microsystems also provides expert bulk micromachining services. This refers to the fabrication of thick 3D microstructures in the bulk of the wafer using two basic etching methods:

- anisotropic chemical etching with KOH and TMAH
- Deep, dense silicon plasma etching using deep reactive ion etching (DRIE)

While KOH and TMAH, both anisotropic etchants, etch the silicon at different rates depending on the crystallographic planes, deep RIE allows the creation of vertical structures with a high aspect ratio and extensive design freedom.

Together these techniques can be used to produce

- beams and springs
- membranes and cavities
- V- and U-grooves
- deep through holes

TRONIC'S Microsystems has extensive experience in using these techniques to manufacture

- SOI piezoresistive sensors
- micro-fluidic devices
- SiOB devices
- precision microstructures

2.1.3.12.2 Metal Surface Micromachining

TRONIC'S Microsystems has developed a special process for producing custom RF MEMS devices based on integrated coils and variable capacitances:

- RF filters
- tunable capacitors
- RF switches

The process makes use of metal deposition, selective etching, and the controlled release of metal structures on the surface of a wafer.

Using this proprietary technology, TRONIC'S Microsystems can produce different RF MEMS devices for customer- specific telecommunications and military applications.

2.1.3.13 TSMC (http://www.tsmc.com/)

TSMC Unveils Nexsys 90-Nanometer Process Technology:

TSMC unveiled its full 90-nanometer technology under the brand name Nexsys and, at the same time announced that 90-nanometer risk production would start in second quarter of 2003. Volume production of the Nexsys 90-nm process will be manufactured on 300mm wafers.

Nexsys technology satisfies the power, performance and integration requirements of a broad spectrum of applications and includes high-performance, low-power, mixed-signal/RF, and embedded memory options.

TSMC established the Nexsys brand for its next-generation SoC process technology platform. The company's 90-nm technology is the first TSMC process to adopt this brand. Nexsys offers a unique triple gate oxide option that facilitates three different oxide thicknesses on a single chip. The triple gate oxide feature removes design restrictions caused by various core/IO combination requirements and should lead to more innovative SoC designs. With 70-75% linear shrinkage and a two-times performance improvement, compared to TSMC's 0.13-Micron technology, Nexsys is poised to become the de-facto SoC process technology platform standard.

2.1.3.13.1 The 90-nm process technology features

- Core supply voltage ranging from 1.0V to 1.2V
- I/O and analog blocks ranging from 1.8V to 3.3V
- Multiple threshold voltage (Vt) option for optimized transistor speed and power consumption trade-offs
- Extremely tight process control for 50-nanometer gate length - the high speed process
- Ni-salicide for better sheet resistance (Rs) in narrow line widths
- Nine-layer copper interconnect, with an extra redistribution layer optional for flip-chip package
- Low-k dielectrics with k less than 2.9 for the lowest RC delay and power consumption

2.1.3.13.2 0.18-Micron

TSMC 0.18-Micron technology is a single poly, six metal layer process with low-k dielectrics. TSMC defines its "true" 0.18-Micron process technology as not only CMOS FET gates with a drawn dimension of 0.18-µms, but also layout and interconnect design rules that are appropriate to the new generation. TSMC's 0.18-Micron technology boasts the industry's tightest metal pitches with 0.46-µm contacted metal layer 1, 0.56-µm contacted metal layers 2 through 5, and 0.90-µm on metal layer 6. These pitches provide a higher gate density and more die per wafer, which leads to a lower cost per chip.

The 0.18-Micron process technology offers the optimal combination of density, speed and power to serve a broad range of computing, communications and consumer electronics applications. The design rules allow densities over 100,000 gates per mm² and an SRAM cell size of only 4.65-µms². The process performance boasts logic speeds of over 400 MHz and on-chip memory speeds of over 500 MHz. Power gate dissipation, with a 1.8V supply, is less than 30 nW/MHz. Early applications include high-performance 3D graphics chips, next-generation digital set-top boxes, high capacity programmable logic devices, and chips for advanced wireless products.

Deployed in seven fabs, TSMC's 0.18-Micron process is the industry's leading platform for system-on-chip designs. Building on a 1.8V foundation, designers can add 2.5V and 3.3V transistors for mixed-signal cores and I/O, precision capacitors and resistors for high-performance mixed-signal functions, as well as high-quality inductors, varactors, and diodes for RF functions.

2.1.3.13.3 0.15-Micron

TSMC's 0.15-Micron process has led the industry with excellent yields and device performance. Acceleration to high volume has begun since the third quarter of year 2000. Deployed in seven fabs, TSMC has installed ample capacity for customers to take full advantage of 0.15-Micron technology for their high-performance designs. This technology reduces die size over 25 percent and provides performance improvements over 30 percent compared to the same device on TSMC's leading 0.18-Micron process technology. When compared to TSMC's high-volume 0.25-Micron process, the new 0.15-Micron process results in less than half the die size and nearly twice the performance.

TSMC's 0.15-Micron technology employs seven layers of metal and has a poly gate length as small as 0.11-µm. The 0.15-Micron technology family will include core-logic, high performance, ultra-high-speed and low power processes. The core-logic, high-performance and low power processes are beginning production now, while the ultra-high-speed processes will begin production in the third quarter of 2000. Features include 1.2V and 1.5V core options and I/Os from 1.8, 2.5 to 3.3V. The technology's 6T SRAM cell size is 3.42µm² , the smallest in the industry. This enables the use of up to 16M of SRAM on a single die, making the technology ideal for a variety of system-on-chip (SOC) applications in the networking, computing and consumer market segments.

2.1.3.13.4 0.13-Micron

TSMC is working diligently on the 0.13-Micron process, with easy integration a top priority during its development. The new technology will reduce die size by more than 20 percent and provide performance improvements for 30 percent when it is compared to the same device on TSMC 0.15-Micron process technology. When compared to the 0.18-Micron process, the new 0.13-Micron process results in less than 60 percent the die size and nearly 70 percent improvement in performance.

TSMC 0.13-Micron technology employs eight metal layers and has a poly gate length as small as 0.08£gm. The technology family will include core-logic, high performance, high speed and low power processes. There will be 1.0 V, 1.2V and 1.5 V core options, and I/Os of 2.5 V and 3.3 V. The 6T SRAM cell size of 2.43µm² makes the technology ideal for a variety of system-on-chip (SOC) applications in the networking, computing and consumer market segments. To reduce RC delay for improved performance, TSMC offers all copper interconnect and low k intermetal dielectrics for 0.13-Micron technology and beyond.

Recognizing that many customer products would need specific performance requirements, multiple Vt options are added to TSMC standard 0.13-Micron offerings for maximum design flexibility. This strategy has attracted tremendous customer interests for a new technology.

Two MPU products started production in 4Q '00, which is more than one full year ahead of ITRS schedule. TSMC has experienced the fastest customer adoption rate at 0.13-Micron in its history, as evidenced by the record number of early tapeouts. Acceleration to high volume has begun in the second half of 2001. Over the next few years, 0.13-Micron technology will be deployed in many of TSMC fabs with ample capacity for customers to take full advantage of having leading-edge technology for their high-performance designs. TSMC is committed to deliver the industry's leading technology to customers for the best performance and value.

Copper Interconnect:
The electrical resistance of copper interconnects is less than two-thirds that of tungsten-aluminum interconnects. The series resistance of copper via runs as low as 20% that of tungsten plugs. Starting from the 0.18-micron process, TSMC has offered customers the option of copper interconnects for the top two layers, which are commonly used for power, clock routing and bonding pads. With this option alone, customers can realize 15% RC delay reduction.

TSMC provides both top two-layer and all-layer copper options at the 0.15-micron process. While copper offers the greatest performance advantage when implemented to the top two metal layers, TSMC also offers an all-layer copper option. In fact, TSMC's 0.13-micron process and beyond will be built on an all copper interconnect architecture.

The lower electrical resistance due to copper leads to improved power distribution and device performance throughout the chip. Copper also improves the electromigration resistance, a major concern in IC's long term reliability, by as much as 50 times. Furthermore, copper's lower resistance helps to reduce cross-talk by providing a better control over the tight metal pitch.

In summary, advanced technology demands extremely high routing density that necessitates copper interconnects. TSMC made its commitment early and has successfully developed the industry-leading copper process.

2.1.3.13.5 SiGe BiCMOS

TSMC is the first pure-play foundry to offer silicon germanium (SiGe) BiCMOS technology, which is expected to be in high demand for high performance and low power communications applications. Combining the integration and cost benefits of standard CMOS with the speed of more esoteric and expensive technologies, such as Gallium Arsenide (GaAs), Silicon Germanium is ideally suited for communications and wireless/optical networking designs. Products designed for and manufactured on TSMC's Silicon Germanium process provide dramatically greater function with fewer chips. As a dedicated foundry company, TSMC has provided customers a very secure manufacturing environment.

TSMC's 0.35-Micron SiGe BiCMOS features an operation voltage of 3.3-volts. The optimized process has 3 NPN bipolar devices with a unit gain frequency (F) of 62/40/25 GHz(HS/ST/HV) and a unit power gain frequency (F) of 70/60/40 GHz at different break down BVceo voltages (>2/3/5V). A deep trench isolation provides superior noise immunity in bipolar devices, a critical consideration in RF designs.

TSMC has also collaborated with one of the industry's leading EDA providers to create a complete design kits including technology files and Process Design Kits (PDK). The PDK includes schematic symbols, simulation models, a layout generator, and tech files. With this powerful PDK, designers can efficiently reduce their development time of foundation libraries. Created and supported by this EDA partner, distributed by TSMC free of charge, the PDK is now provided to TSMC customers directly through TSMC-Online.

2.1.3.13.6 High Voltage

TSMC's high-voltage process technologies are provided to support for 12V, 18V and 40V devices working on 0.35-μm and the above design rules. TSMC offers a range of cost effective and advanced high-voltage processes for innovative fabless IC companies, Integrated Device Manufacturers and Systems Houses.

TSMC offers comprehensive high-voltage technologies suitable for high-voltage and power integrated circuits. TSMC's high-voltage processes allow designers to integrate high-voltage, high-power devices with generic low-voltage logic and mixed-mode devices for system-on-a-chip applications. The ability to embed high-voltage modules into baseline logic and mixed-mode processes maximizes design flexibility and cost effectiveness in producing systems with reduced chip counts.

The high-voltage technologies offer high performance transistor based on TSMC generic logic process. The electric performance of low-voltage logic part is identical to the respective logic process. There are two kinds of high-voltage transistor families are approached. The first one is DDD (Double Diffused Drain) CMOS structure, which is for high-voltage equal or below 18V application. The second one is LDMOS (Lateral Diffused MOS) structure, which is for high-voltage equal or below 40V application.

TSMC's high-voltage technologies provide cost effective and flexible manufacturing processes for display driver ICs, power supplies, power management, telecommunications, automotive electronics and industrial controls.

2.1.3.13.7 Mixed Signal / RF

TSMC is the only dedicated foundry to have shipped over one million wafers for mixed signal / RF CMOS technologies, ranging from industry leading 0.13-Micron production to mature 0.18-Micron, 0.25-Micron, 0.35-Micron, 0.5-Micron, 0.6-Micron, 0.8-Micron, 1.0-Micron, and 1.2-Micron processes. The next generation 90-nm mixed signal/RF process is targeted for production in early 2003 using 300mm wafers.

TSMC's Mixed Signal / RF CMOS processes provide designers with smaller device dimensions, increased performance and lower costs than BiCMOS and gallium arsinide processes. TSMC provides comprehensive design kits for either logic-based or full-featured MS/RF technologies. Plug-in databases and models are ready-to-use, which help significant reductions in design cycle time. These advancements lead to accurate performance prediction and higher levels of integration for TSMC customers.

2.1.3.14 UMC (http://www.umc.com/)

UMC is one of the world-leading semiconductor foundries, specialized in the contract manufacturing of customer designed ICs for high performance semiconductor applications. Since entering the pure-play foundry industry in 1995, UMC has been the sector's fastest growing company. UMC delivers the cutting-edge foundry technologies that enable sophisticated system-on-chip (SOC) designs, including 0.13um copper/low k, embedded DRAM, and mixed signal/RFCMOS. In addition, UMC has strong position in 300mm manufacturing with strategically located 300mm fabs to serve global customer base: Fab 12A in Taiwan and UMCi in Singapore. UMC employs over 9,500 people worldwide and has offices in Taiwan, Japan, Singapore, Europe, and the United States.

300mm Manufacturing:
The first foundry to produce chips on 300mm wafers. UMC's 300mm fabs in Singapore and Taiwan are currently in volume production manufacturing advanced products.

2.1.3.14.1 90-Nanometer: The Standard for Foundry High Performance Technology

UMC has been shipping customer products based on its 90-nanometer (0.09-um) logic process since March of 2003, making UMC the first dedicated foundry company to announce the delivery of working customer IC's built on the industry's advanced manufacturing technology. The achievement is a product of intense collaboration between the engineering teams of UMC and its customers, and is a testimony to UMC's proven ability to provide the industry's leading-edge process technologies in a timely fashion. Currently, UMC is product qualified and in volume production for multiple customers' 90nm products. UMC is also the only foundry to offer both low-k or FSG for 90nm manufacturing, giving customers the flexibility to choose the dielectric material best suited for their particular product application.

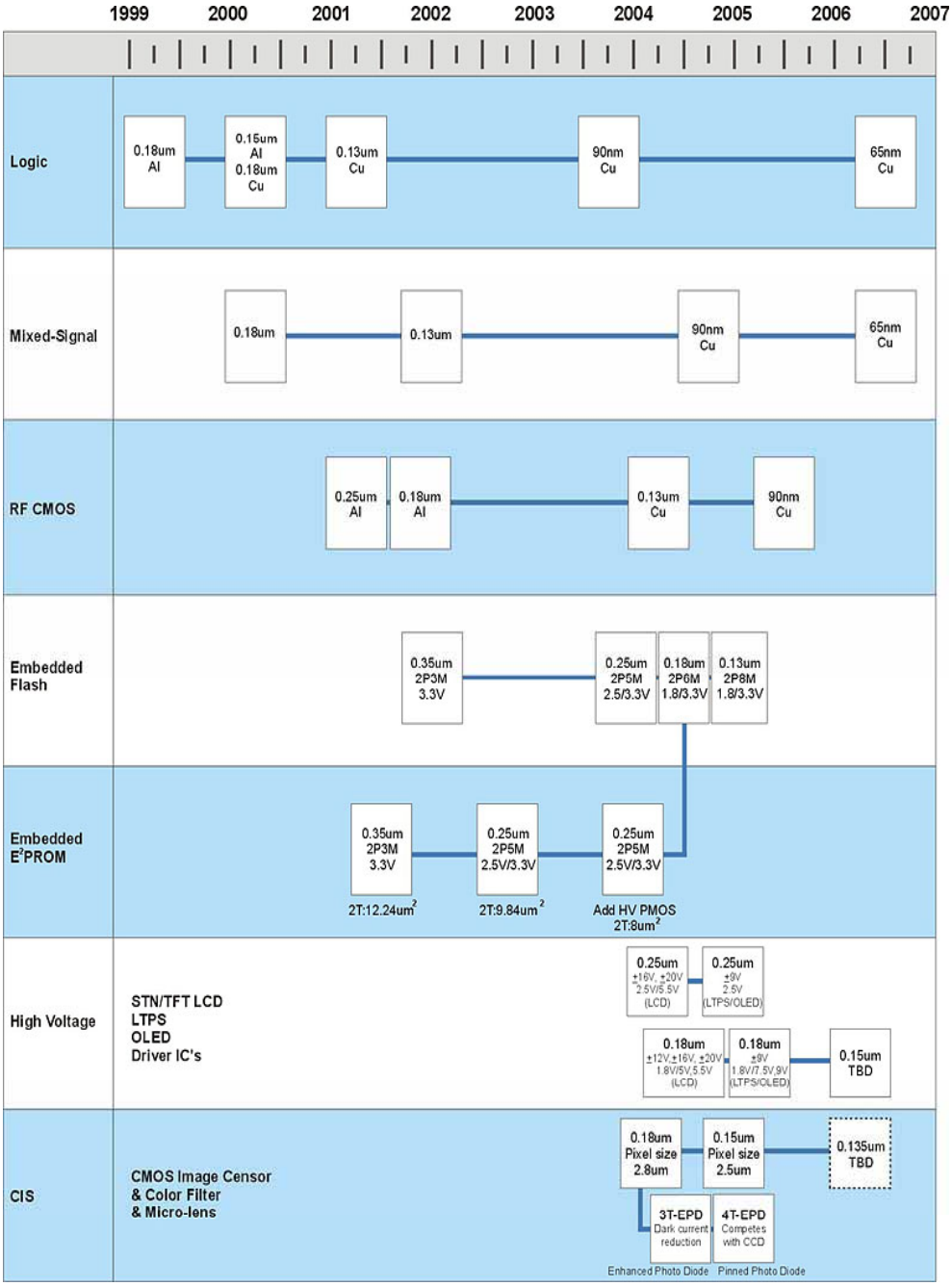
Key Features of UMC 90-nanometer technology:

- 193nm Lithography
- Retrograde Twin Well (Triple Well Option)
- Multiple Vt Option for optimized SOC Application
- Dual Nitridized Gate Dielectric (Triple Oxide Option)
- Dual Poly Gate with $CoSi_2$
- Up to nine Cu Metal/Via Layers with Low-k or FSG options in the thin metal layers
- Wire Bond/Flip Chip
- 1.16/0.99um_2 SRAM Bit Cell
- Same Process for Logic & Mixed Mode (for SOC Applications)

UMC's extensive experience at the 0.13-um generation has helped smooth the transition to 90nm production. Many of the materials and techniques that were first introduced at the 0.13um generation also benefit 90nm production, including copper interconnects and low-k dielectric materials. UMC's 90nm process pushes the technology envelope by incorporating up to nine copper metal layers, triple gate oxide and other advanced features. Companies demanding ultimate performance, density, and power consumption will benefit from UMC's progress in 90nm technology.

UMC has achieved multiple product successes from the close, collaborative work with customers for their products based on UMC's 90nm process. With successful production ahead of the ITRS industry roadmap, UMC has further illustrated its commitment to offering the leading-edge technology solutions to help customers realize their market objectives. Two platforms of the advanced 90-nanometer technology, L90 and L90G, were offered to meet the specific product application.

Competitiveness through Productivity:
300mm wafers have over twice the usable area as 200mm wafers, delivering productivity advantages of up 2.5 times the number of chips. This translates directly into greater competitive advantages for customers. UMC's 300mm facilities utilize state-of-the-art computer integrated manufacturing (CIM), which together with the extensive 300mm experience, has allowed UMC to achieve 300mm yields and cycle times comparable to 200mm manufacturing. Larger Die Sizes More Efficiently Utilize 300mm Wafer Area.



2.1.3.14.2 Mixed Signal/RFCMOS

Applications such as WLAN, Bluetooth, 3G, Gigabit Ethernet, and portable communications devices are fueling the demand for advanced Mixed Signal/RFCMOS processes. UMC provides a logic-based technology platform with Mixed Signal/RF devices--a high performance, low cost solution for SOC designs. Besides providing a common technology platform, UMC also provides a design environment to support Mixed Signal/RF designs, meeting customers' time to market needs. The design environment includes Mixed Signal/RF foundry design kits, accurate models and P cells, automatic schematic driven layout environments, simulation, and verification flow.

Logic Based Technology:

- Retrograde Twin Well
- Shallow Trench Isolation (STI)
- Co salicide for Gates & S/D
- W plug for contact
- CMP IMD with Low-k or FSG
- Cu or Al metal via

Mixed Signal/RFCMOS Key Features

Technology	0.18um	0.13um
Core / I/O Voltage	1.8V / 3.3V	1.2V/3.3V
Transistor Vt (Core & I/O)	Nominal, Low-Vt, Zero	Nominal, Low Vt, Zero Vt
Metal / Metal Capacitor	1fF/um²	1.0 fF/um2
HR Resistor	1000 ohm/sq.	1000 ohm/sq.
Inductor	2um Al,	2um (Cu)
Qmax for L = 2.8nH	Q>10 @2.4GHz	Q>12@2.4GHz
Varactor	Vc>45%/V	Vcc>45%/V
Triple Well	Available	Available

RF Characteristics

Technology	0.25um	0.18um	0.13um
Ft	30GHz	45GHz	105 GHz
Fmax	20GHz	35GHz	90 GHz
Noise Figure	0.8 dB@2.4GHz	0.6 dB@2.4GHz	0.58 dB @2.4GHz
Inductor	2um Al	2um Al	2um Cu
Qmax for L=2.8nH	Q=10@2.4GHz	Q=10@2.4GHz	Q >12 @2.4GHz

2.1.3.15 UMS (http://www.ums-gaas.com)

Foundry Service:
The UMS foundry, based in Orsay outside Paris, is dedicated to delivering a range of products and services that bring value and benefit to its client base. State-of-the-art systems, design kits and an extensive data base of metrics and reliability models, support the development and production of customer specific integrated circuits.

Training and mentoring is available from highly experienced professionals, who have depth and breadth of experience in the design and application of GaAs technology.

The Benefits:
Many benefits can be gained from working with the UMS foundry to develop custom ASICs using leading edge gallium arsenide technologies.

It is widely recognised that ASICs give the freedom to balance functionality and performance to create an ideal solution.

Efficiencies and cost reductions can be gained from:

- functional integration on a single die
- - reduced component count
- - improved power management
- However, ASICS offer significant strategic benefits helping organisations:
- - create and protect IPR
- - win and maintain competitive advantage
- - simplify inventory and lifecycle management

2.1.3.16 XFAB (http://www.xfab.com/)

X-FAB is the leading European-American foundry group that specializes in mixed-signal applications. With its three manufacturing sites in Germany, the UK and the USA, X-FAB has a combined capacity of more than 28,000 8" equiv. wafer starts per month at its disposal and employs approximately 1.000 employees worldwide.

Services:
X-FAB, as a pure-play foundry supplier, combines ultra-modern, modular CMOS and BiCMOS process technologies with excellent service and first-class support during IC development.

On top of these, the services include attractive, customer oriented solutions to prototyping needs as well as subcontracting test and assembly services to external partners.

Multi Product Wafer (MPW) and Multi Layer Mask (MLM) services as cost-effective solutions to reduce customer's development expenses are provided. Additional services include design reviews, DRC checks, mask generation and several configuration options for the delivery of die.

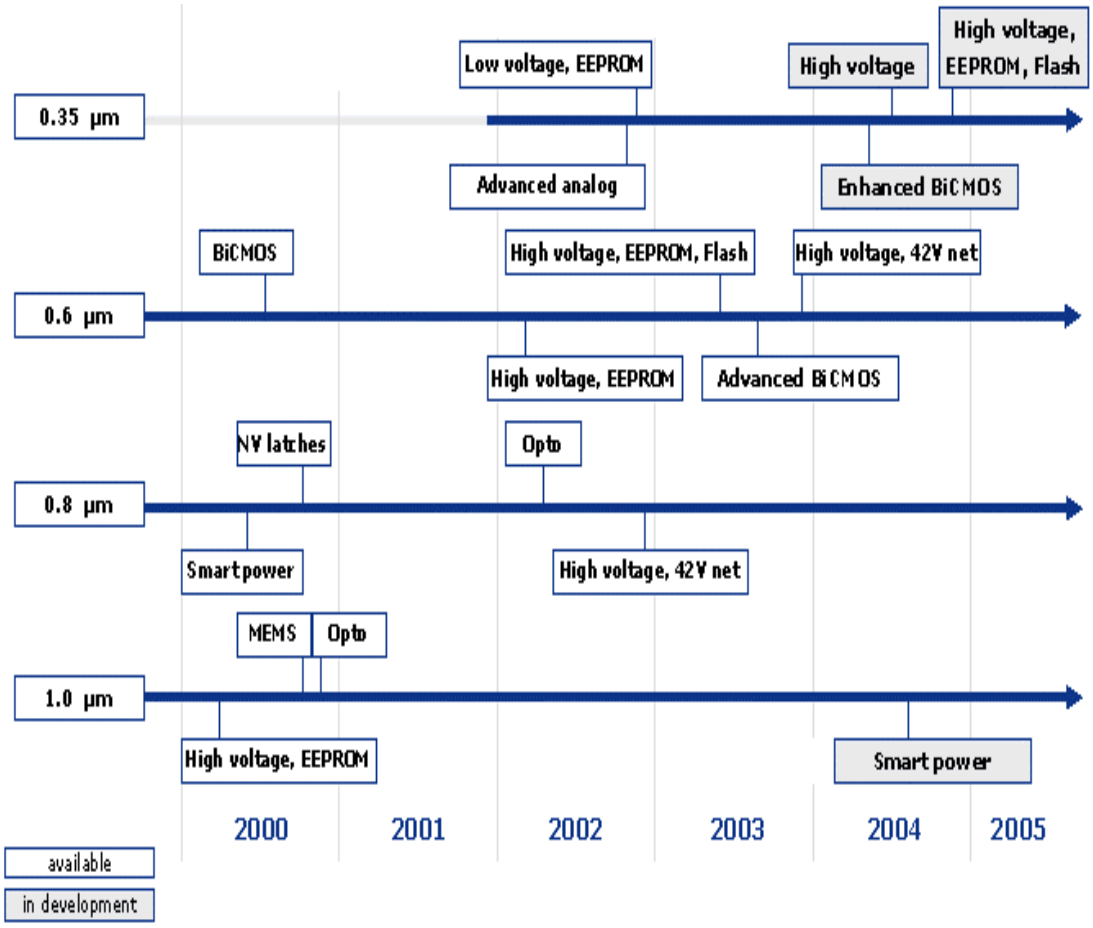
Business offering:
When manufacturing silicon wafers for analog and mixed analog-digital integrated circuits, X-FAB, as a pure-play foundry supplier, combines ultra-modern, modular CMOS and BiCMOS process technologies with excellent service and first-class support during IC development.

In addition, from the early product development phase through to batch production, X-FAB offers outstanding online support, with full access to technical documentation.

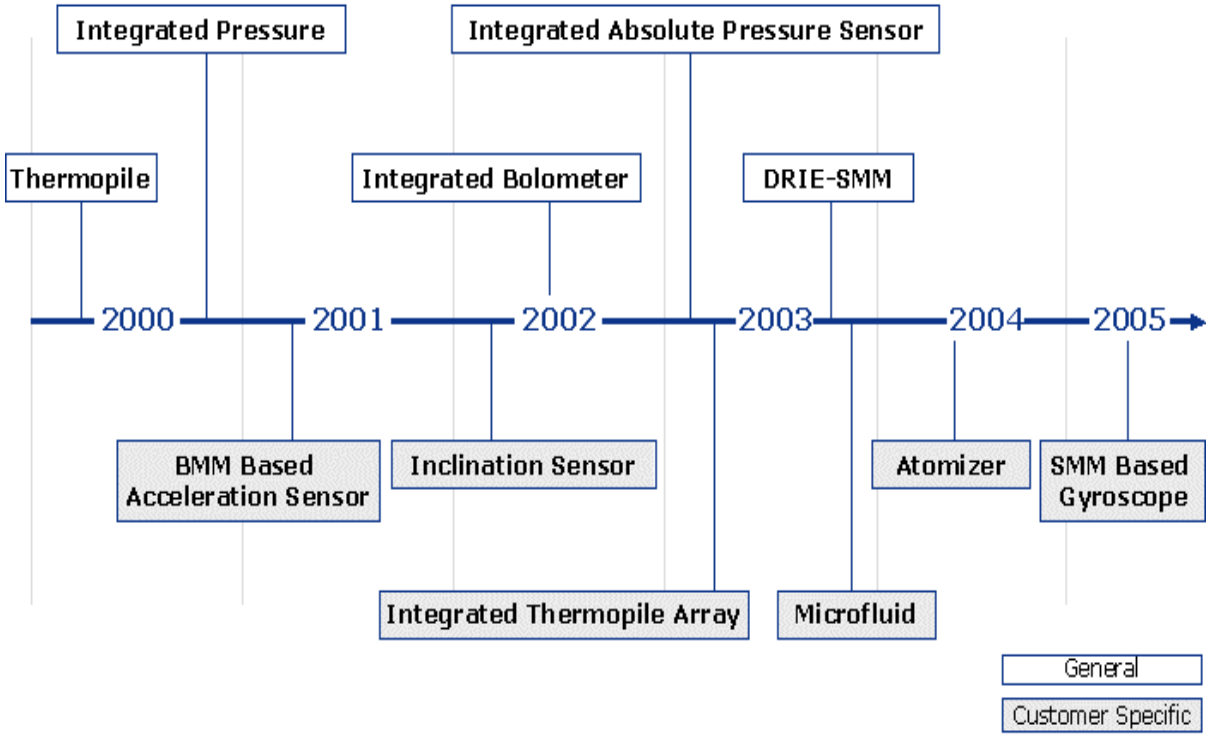
X-FAB continually expands its available process technologies with additional analog functions and modular options. At the same time, existing experiences and performance features from the analog sector are integrated into new process families. Special processes for new user markets complement the product offering.

- **CMOS Technologies:** 1.0 - 0.35 µm modular mixed-signal CMOS technologies on silicon substrates
- **BiCMOS Technologies:** 0.6µm BiCMOS & 0.35µm (in development) technologies
- **SOI-CMOS Technologies:** 1.0µm CMOS technology on SOI substrate and DiMOST technologies
- **MEMS Technologies:** Microelectromechanical sensor technologies (can be combined with CMOS)
- **Customer Specific Technologies:** Proven competence for installing MOS and MEMS technologies on Si, SOI and quartz wafers

2.1.3.16.1 X-FAB Mixed-Signal Processes - Evolution



2.1.3.16.2 X-FAB Spezial-Processes - Evolution - MEMS



2.1.3.16.3 X-FAB Spezial-Processes - Evolution - SOI Type

CMOS Technologies							
	Advanced analog	Mixed-signal (2. Poly)	High voltage	Non-volatile	Bipolar	Metall Options	Opto
X-CMOS 1.0	x	x	x	x	x	x	x
X-CMOS 0.8	x	x	x	x	x	x	x
X-CMOS 0.6	x	x	x	x	x	x	x
X-CMOS 0.35	x	x	x		x	x	i.d.
X-CMOS 0.35 LV	x	x	x	x	x	x	i.d.
X-CMOS 0.35 HV	i.d.	i.d.	i.d.	i.d.	i.d.	i.d.	

2.1.3.16.3.1 X-CMOS 1.0

[XC10Nxx]
1.0 µm state of the art CMOS process with additional options

Key Features

- Cost effective one micron single poly, single metal N-well core process on P epi
- High voltage (100 V) N-MOS transistors available in the core process (no additional mask)
- Double poly module for resistors and capacitors
- High-voltage (50 V) option for P-MOS transistors
- Low-voltage option (1.5 V instead of 5 V operating voltage)
- Special devices:
  - · depletion and zero transistors,
  - · Schottky and Zener diodes,
  - · high-ohmic resistors,
  - · bipolars
- Double metal option
- Power metal option
- High precision BSIM3V3 SPICE models
- Excellent analog performance with accurate device matching
- Digital core cell library with typical 600 effective gates per mm²
- Typical gate delays (digital) of 3.5 ns
- I/O cell library
- Electrostatic discharge (ESD) protection in accordance with MIL-STD
- Memories: RAM, ROM, EPROM, EEPROM
- Parameter trimming by poly-fuses or non-volatile latches
- Development kits for major EDA tools
- Megafunctions and IP's available
- Optional ESD layer for higher ESD protection
- Optical window module

2.1.3.16.3.2 X-CMOS 0.8

[CX08Nxx]
0.8 µm state of the art n-well CMOS Process with additional optional features

Key Features

- 0.8 micron single poly, double metal N-well core process with 11 masks
- Double poly module for poly-poly capacitors
- High-resistive poly resistor module
- High-voltage option up to 50V DC for HV NMOS, PMOS, DMOS, JFET and bipolar devices with ad-vanced EMC and latch-up immunity and reduced substrate noise due to triple well concept
- Extended high-voltage module - NMOS, PMOS, DMOS for 42V board net automotive application
- EEPROM module for NV-latches
- Power-metal option (third metal) for smart power applications
- Large number of primitive elements
- High precision BSIM3V3 SPICE models
- Excellent analogue performance with accurate device matching
- Various digital core cell libraries optimized for most typical applications 1200 to 1500 effective gates per mm²
- Typical gate delays (digital) of 160 ps
- 5V and 3.3V I/O cell libraries
- IEEE 1149.1 boundary scan macros
- Electrostatic discharge (ESD) protection in accordance with MIL-STD
- Analogue library
- High-density RAM, DPRAM. ROM blocks
- OTP options: poly-fuses, zener-zaps
- Development kits for major EDA tools
- Megafunctions and IP's available

2.1.3.16.3.3 X-CMOS 0.6

[XC06]
n-well CMOS process with 15 available, very flexible combinable modules such as high voltage, extended high voltage, embedded EEPROM and Flash

[CX06]
state of the art n-well CMOS process with reduced number of available modules

XC06
Key Features

- 0.6-micron single poly, double metal N-well CMOS basic process
- Triple metal option for high density circuits
- Different medium and high voltage options with 8 to 40 V DC operating conditions for NMOS and PMOS transistors
- Extended high-voltage modules with = 60V DC operating conditions - NMOS, PMOS and DMOS for 42V board net automotive application
- Triple well isolated CMOS transistors
- Different bipolar transistors
- Double Poly-Si capacitor
- Linear poly capacitor module
- High-resistive Poly-Si resistor
- High precision BSIM3V3 SPICE models for CMOS and Gummel Poon model for bipolars
- Excellent analog performance with accurate device matching
- Embedded EEPROM with ready to use EEPROM blocks
- Embedded Flash memory with ready to use Flash blocks
- Different digital core cell libraries optimized for speed, low power or low noise
- High density RAM, DPRAM and ROM blocks
- Analog library
- About 2500/4500 effective gates per mm2 (2ML/3ML)
- 5V and 3.3V I/O cell libraries with CMOS / TTL interfacing capability
- Electrostatic discharge (ESD) protection in accordance with MIL-STD
- Optional ESD layer for higher ESD protection
- Development kits for major EDA tools

CX06

Key Features

- 0.6-micron single poly, double metal N-well CMOS basic process
- Triple metal option for high density circuits
- Double poly capacitor
- High-resistive poly resistor module
- High precision BSIM3V3 SPICE models for CMOS and Gummel Poon model for bipolars
- Excellent analogue performance with accurate device matching
- Three digital core cell libraries optimized for most typical applications 2000 to 2500 effective gates per mm^2
- Typical gate delays (digital) of 160 ps
- 5V and 3.3V I/O cell libraries
- IEEE 1149.1 boundary scan macros
- Electrostatic discharge (ESD) protection in accordance with MIL-STD
- High-density RAM, DPRAM. ROM blocks
- OTP options: zener-zaps
- Development kits for major EDA tools

2.1.3.16.3.4 X-CMOS 0.35

[XC035]

State of the art 0.35µm 3.3V CMOS process with 5V module and additional optional features for mixed signal applications

[XC035LV]

mixed signal, low voltage 0.35µm CMOS process with embedded non-volatile memory and optional features

XC035

Key Features

- 3.3V Logic Layout & performance compatible with the industry standard
- 0.35-micron single poly, triple metal N-well CMOS basic process
- 3.3V Core, 5V tolerant I/O's
- Silicided source & drain
- 5V NMOS / PMOS Module (with 18V LDMOS)
- Double Poly module for poly-poly capacitors
- Four layer metal options for high density circuits with up to 18000 gates per mm^2
- High Value Polysilicon resistor module
- Typical and worst-case models - BSIM3v3.1 (MOS, BJT, RES, CAP)

XC035LV

Key Features

- 3.3V Logic Layout & performance compatible with the industry standard
- 0.35-micron double poly, triple metal N-well CMOS basic process
- Silicided source & drain
- <1V & 3.3V Core, 5V tolerant I/O
- Double Poly Capacitor
- High Voltage transistors to support EEPROM programming
- Four layer metal options for high density circuits with up to 18000 gates per mm²
- Additional optional components: floating gate EEPROM and Schottky diodes
- Typical and worst-case models - BSIM3v3.1 (MOS, BJT, RES, CAP)
- MOS 1/f noise characterized & included in model

2.1.3.16.4 BiCMOS Technologies

	Advanced analog	Mixed-signal (2. Poly)	High voltage	Non-volatile	Bipolar	Metall Options	Opto
X-BiCMOS 0.6	x	x	x	i.d.	x	x	x
X-BiCMOS 0.35	i.d.	i.d.		i.d.	i.d.	i.d.	

x = available i.d. = in development

2.1.3.16.4.1 X-BiCMOS 0.6

[XB06]

0.6 Micron BiCMOS Technology for RF circuits and high precision analog applications mixed with standard digital parts in CMOS

Key Features

- 0.6-micron double poly, double metal N-well CMOS process
- High frequency npn transistor with poly emitter and buried collector
- Large number of bipolar primitive devices; well adjusted for most typical requirements
- Double poly capacitor module with high capacity per area
- High-resistive poly resistor module
- High precision BSIM3V3 SPICE models for CMOS and Gummel Poon model for bipolars
- Excellent analogue performance with accurate device matching
- Three digital core cell libraries optimized for most typical applications

- 2000 to 2500 effective gates per mm²
- Typical gate delays (digital) of 160 ps
- 5V and 3.3V I/O cell libraries
- IEEE 1149.1 boundary scan macros
- Electrostatic discharge (ESD) protection in accordance with MIL-STD
- High-density RAM, DPRAM. ROM blocks
- OTP options: zener-zaps
- Development kits for major EDA tools

2.1.3.16.5 SOI & DIMOS Technologies

	Advanced analog	Mixed-signal (2. Poly)	High voltage	Bipolar	Metal Options
X-SOI-CMOS	x	**x**	**x**		**x**
X-DiMOST 2.5 500V Smart Power			**x**	**x**	**x**
X-DiMOS 1.0 650V Smart Power	x	**x**	**x**	**x**	

x = available i.d. = in development

DIMOS: Double Implanted MOS

2.1.3.16.5.1 X-SOI 1.0µm

[XI10]
1.0 µm Silicon-On-Insulator Technology

- 1.0µm single poly, 3metal layer SOI process
- Fully dielectric isolated twin well
- Isolated diodes
- Floating body and body tied 5 V N- and PMOS transistors
- DMOS for n and p channel up to 130V
- High temperature option (250°C)
- Linear capacitor
- High resitive poly module
- Hall plate for magnetic field detection
- High precision BSIM3V3 SPICE models
- Excellent analogue performance with accurate device matching
- Low power, high temperature digital core library
- 5V I/O cell library

- Electrostatic discharge (ESD) protection in accordance with MIL-STD
- Development kits for major EDA tools

DIMOST

500 V Dielectric Isolated MOS Technology

- 500V N-Channel Vertical DMOS Transistor
- 300V P-Channel MOS Transistor
- 15V Analog CMOS
- 5V Digital CMOS
- Bipolar Transistors (Vertical NPN; Lateral PNP)
- Zener Diodes
- HV Diodes
- Poly Si Resistors
- Oxide Capacitor
- Wide variety of MOS and Bipolar Devices on the same die
- Using of different Voltage Levels (500V; 300V, 80V; 15V; 5V)

2.1.3.16.5.2 X-DiMOS 1.0µm

[XD10H]

1.0 µm 650 Volt Trench Insulated BCD Process for Smart Power applications

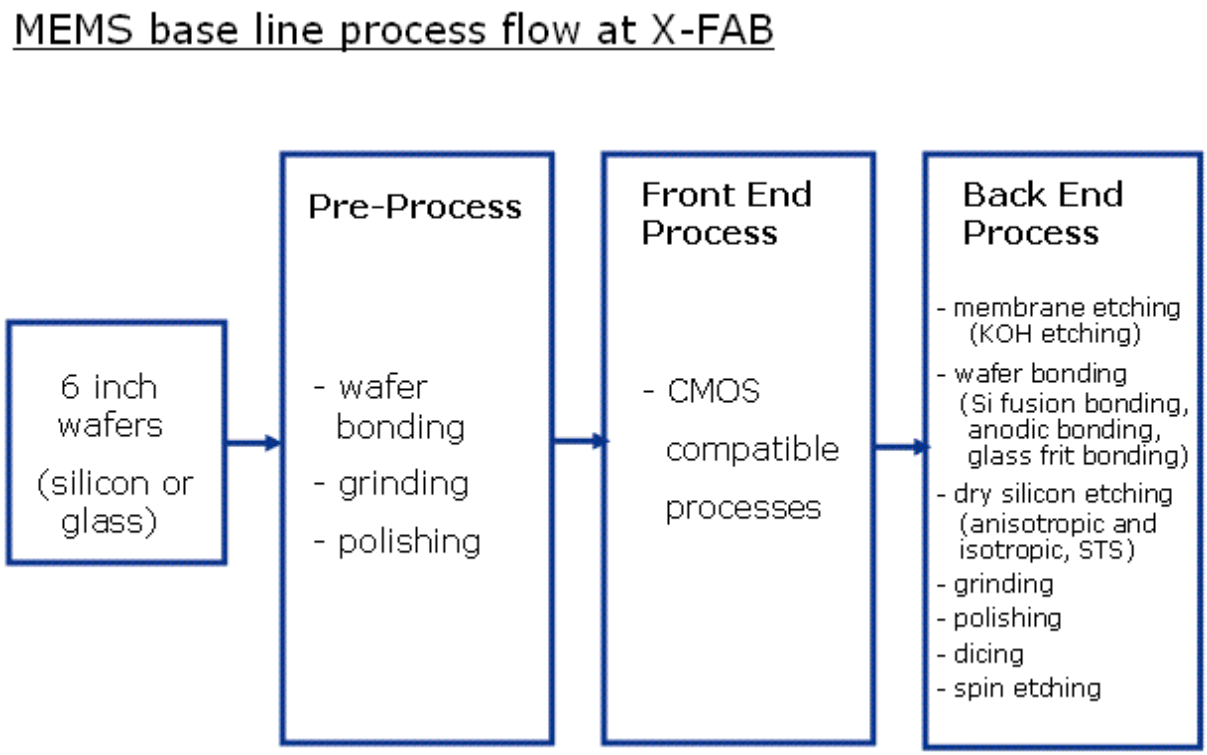
Key Features

- 650 and 350 Volts n-channel DMOS
- 330 Volts PMOS
- CMOS transistors with different voltage levels
- NPN and PNP transistors with different voltages
- High voltage and zener diodes
- Gate oxide and high voltage capacitors
- Poly resistors with different sheet resistivities
- Triple level metal, third metal 2.3µm thick
- Optional third poly for high value resistor or poly-poly capacitor
- Doped oxide / polyimide passivation
- 1µm design rules enable the integration of complex CMOS logic
- High precision BSIM3V3 SPICE Models
- Excellent analog performance with accurate device matching
- Digital core cell library
- 5V I/O cell library
- Electrostatic discharge (ESD) protection in accordance with MIL-STD
- Development kits for major EDA tools

2.1.3.16.6 MEMS Technologies

X-FAB Microelectromechanical Sensor Technologies:

- Since 1995 has X-FAB experience in development and production of micro machining processes and is world wide the first pure play MEMS foundry.
- Wafer foundry in well proven X-MS production technologies for dedicated MEMS devices is offered.
- Moreover XFAB is in a outstanding position for customization of the MEMS base line to meet customer`s requirements.
- Transfer of customer specific technologies to X-FAB is also possible, enabling you to access engineering competence and equipment base.



Specific MEMS Process Steps	
Front-to-Backside Alignment	Full automatic alignment system to pattern backside masks in alignment to front side structures
Membrane etching	KOH wet etching with electrochemical etch stop or time controlled etching
Dry Silicon etching	Etching through Silicon membranes or trench etching (ASE / BOSCH process)
Sacrificial layer etching	Removal of polyimide from beneath features, to realise free-standing components
Wafer bonding	Silicon fusion or anodic wafer bonding, glass frit bonding in development
Spin etching	Removing of oxide or nitride layers without protecting of the opposite wafer side preparing of wafer back sides for KOH etch masks
Grinding and polishing	Wafer thinning
Glass wafer processing	Patterning of Borofloate® wafers

2.2 SURVEY OF PACKAGING FACILITIES AND ASSOCIATED TECHNOLOGIES

2.2.1 Chip Level

2.2.1.1 Interconnection technology

2.2.1.1.1 Flipchip, Wire Bonding

In this section, two widely used interconnection technologies, flip chip and wire bonding, are described and compared. There are numerous books, articles, and web pages on the topic, e.g. [1-10].

Flip chip and wire bonding microelectronic assemblies are technologies for the connection of electronic device onto a substrate, circuit board, or carrier. Flip chip technology is also called by descriptive name direct chip attach (DCA) [4]. In the flip chip assembly, the device is mounted face-down i.e., it is "flipped". The connection to the substrate pads is made with conductive bumps. In wire bonding technology, the device is placed face-up and conducting wires from substrate pads to device pads are used to produce the electrical connection. In the wire bonding, the used wires are typically 1-5 mm in length, and 25-35 μm in diameter. In the flip chip assembly bumps are typically 50-100 μm high, and 100-125 μm in diameter [8,9].

Flip Chip Assembly

Flip chip technology is first developed by IBM in 1960's [4]. There are basically three steps in the flip chip process: 1) bumping of the die or the wafer, 2) attachment of the die on the substrate, and 3) underfilling of the space between the die and the substrate with resistive material [4,5]. These steps can also be further divided [4,5].

1. There are several tasks for the conducting bumps. In addition to the electrical conduction, bumps provide thermal conduction from device to substrate. Also, the bumps provide space between the device and the substrate preventing unwanted electrical contacts. There are several techniques for making the soldering bumps requiring different number of processing steps [4,7,9]. In addition to conductive metal suitable for soldering, the bumps may be of conductive adhesive.
2. The assembly of device is made by placing it face-down on top of the substrate. The attachment of bumps can be done by different processes including soldering, joining with thermocompression, thermosonic joining, and joining with conductive or non-conductive adhesives.
3. The non-conductive underfill between the device and substrate board provides additional mechanical strength for the assembly and it also protects the device from moisture and other environmental hazards [4].

2.2.1.1.2 Suppliers for Flip Chip Technology

Flip Chip International, http://www.flipchip.com/

FlipChip is an international provider of merchant Wafer Level Packaging (WLP) and flip chip bumping to the semiconductor market through its Phoenix Arizona, USA, facility and five

global licensees. Services provided include: Standard flip chip (SFC, formally known as Flex-on-Cap™), redistributed SFC, wafer Ultra CSP™, Spheron™ (high frequency RF packaging), EliteCSP™ (a low cost E-less Nickel bumping WLCSP), and Polymer Collar™. FlipChip provides wafer bumping services from engineering prototypes to high volume manufacturing.

IBM, http://www-03.ibm.com/chips/about/technology/makechip/interconnect/11.html

IBM provides electronic manufacturing services including design, test and supply chain management. IBM provides interconnect technologies such as ball grid arrays, micro BGAs and flip chip.

Nexxsystems, http://www.nexxsystems.com/flipchip_apps.htm

Nexxsystems (USA) provide manufacturing equipment for flip chip packaging, including wafer bumping, wafer cleaning, photoresist strip, and related technologies.

Kyocera, http://americas.kyocera.com/

Kyocera offers complete flip chip packaging capabilities in San Diego, California manufacturing plant. The facility specializes in high-quality, high-yield assembly of a wide variety of packages. Assembly capabilities are value added with test services.

Süss MicroTec, http://www.suss.com

Süss MicroTec (USA) provides manufacturing equipments for flip chip assembly

Fraunhofer Institut Zuverlässigkeit und Mikrointegration IZM, http://www.pb.izm.fhg.de/izm/EN/

Fraunhofer Institute for Reliability and Microintegration IZM together with the Research Center for Microperipheric Technologies at the TU Berlin provides research, development and service, e.g., in the area of wafer processing and MEMS technologies. In the field of chip interconnection technologies the department focuses on flip chip, TAB and chip & wire bonding. This includes die attach using adhesive or solder alloys as well as underfill and glob top encapsulation.

Accelonix UK, www.accelonix.co.uk

Accelonix is a solution provider for many types of test application in electronic production and development environments with expertise in EMC/RF and the high technology fields of automated test equipment and advanced microelectronics packaging equipment production. Accelonix represents companies in the field of flip chips:

- Datacon Technology GmbH provides flip-chip bonders
- Hesse & Knips provides flip-chip bonders

Pac Tech, Germany, www.pactech.de

Pac Tech offers subcontractor wafer bumping for the Flip Chip and CSP Technology. It also offers the assembly of flip chips for prototyping and small volumes in cooperation with Smart Pac.

TWI UK, www.twi.co.uk

TWI has a FINETECH GmbH Lambda flip chip bonder. The manual bonder has +/-1µm placement accuracy and capability for a wide range of flip chip bonding techniques, including

solder reflow (up to 400°C), thermosonic, anisotropic adhesive, thermocompression, cold pressure welding and ultrasonic. TWI provides a path to volume manufacturing using its knowledge of wafer bumping and flip chip assembly subcontractors and equipment manufacturers.

Finetech GmbH & Co. KG., http://www.finetech.de/enid/2.html

Finetech manufactures flip chip bonders for flip chip assembly.

REEL Service, http://www.reelservice-europe.com/

The Reel Service Group is a worldwide services and manufacturing organisation providing tape and reel packaging services and supplies to the electronic components manufacturing industry. Their key services include tape & reel packaging, fully automated device inspection, component programming and other related component handling services. They have facilities in Germany, Singapore, California and the Philippines.

Wire Bonding Assembly

Wirebonding is the first technique of device assembly: Bell Laboratories published the first results in 1957 [10]. In wire bonding, the thin wire is welded to the device and substrate pads with heat, pressure and/or ultrasonic energy referring to three bonding processes: thermocompression bonding, ultrasonic bonding, and thermosonic bonding [10]. The wirebond is formed when the wire is brought in contact with the pad surface and electron sharing or interdiffusion of atoms is taking place. First in the wirebonding process, the chip is attached to a chip carrier using either an organic conductive adhesive or a solder. Then the wires are welded with a special welding tool producing the wirebond. There are two types of wirebond: ball bond and wedge bond (see Figure 2.2-1). [10]

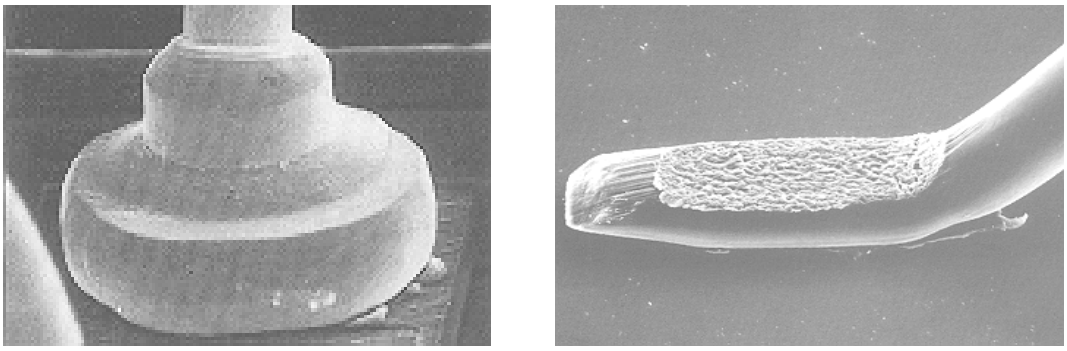


Figure 2.2-1. (lhs) Ball bond (after APROVA Bonding tool) [10], (rhs) wedge bond (after K&S Micro-Swiss) [10].

Thermosonic gold ball bonding is the most widely used bonding technique: it is faster than competing ultrasonic aluminum bonding. The ball bond is also beneficial as once the ball bond is made, the wire can be moved in desired direction without stress on the wire[10]. The wire bonding speed can reach 100-125 ms per wire interconnection using two welds and a wire loop). [10]

Wire bonding is the most widely used interconnection technology and applications include: single and multitiered cofired ceramic and plastic ball grid arrays (BGAs), single chip and multichip, ceramic and plastic quad flat packages (CerQuads and PQFPs), chip scale packages (CSPs), and chip on board (COB). Wirebonding is probably going to dominate

memory and commodity packaging for relatively small I/O counts (< 500 I/O) in the future. [10]

The main limitation in the wire bonding method is that the device pads have to be placed in periphery of the device, otherwise the crossing wires would easily cause short circuits. This limits the number of I/O connections. [10]

2.2.1.1.3 Suppliers for Wire Bonding

Fraunhofer IZM, http://www.pb.izm.fhg.de/

Fraunhofer IZM provides several wire bonding techniques including ultrasonic bonding, thermocompression bonding, and thermosonic bonding. Chip metallization can be aluminium, gold, or copper. Aluminium and gold wires are used. Typical applications are micromechanical components, single chips and fabrication prototypes.

TWI's Microtechnology Centre, http://www.twi.co.uk/j32k/unprotected/band_1/tfwirebo.htm

TWI's Microtechnology Centre has developed wire bonding for over 30 years. Its R&D work and technical support for industry covers:

- aluminium, gold, copper & insulated wires
- 7µm - 1mm diameter
- ball/wedge & wedge/wedge
- ultrasonic, thermosonic & thermocompression
- rigid, soft & compliant substrates

TWI's resources includes:

- automatic & manual wire bonding equipment
- fatigue, mechanical & non-destructive testing
- environmental & metallurgical test equipment
- troubleshooting, feasibility studies & process development
- tailored & scheduled training courses

Microhybrids, http://www.microhybrids.com/wire_bonding.htm

Microhybrids Inc. provides thermosonic gold ball bonding. Typical wire diameters are from 0.0007 inch to 0.002 inch. They have fully automatic wire bonding ensuring high volume consistent wire attachment. The wire bonds are pull-tested to ensure reliability. Gold ribbon bonding is also available.

Unaxis Assembly & Packaging, www.unaxis.com

Assembly & Packaging (ESEC) is a global supplier of chip assembly equipment and system solutions for manufacturers of semiconductors. Assembly & Packaging's core products are die bonders and wire bonders. It has also production systems for flip-chip bonding. Headquarters is in Cham (Switzerland), and the division has eight service centers in Europe, the USA, and key Asian markets.

Labtech, UK, http://www.labtech.ltd.uk

Labtech Microwave and Labtech Circuits are manufacturer of custom microwave and circuit components and services. It provides for example chip & wire assembly and test.

Mühlbauer, Germany, http://www.muehlbauer.de/

Mühlbauer offers the complete IC module production equipment for standard and flip chip production. From die bonding to electric and optical inspection the whole chain is covered.

HYMEC, The Netherlands , http://www.hymec.nl/

HYMEC provides chip assembly for example wirebonding and flip chip.

Microelectronic Assembly Frankfurt (Oder) GmbH, http://www.maf-gmbh.de/eindex.htm

Microelectronic Assembly Frankfurt provides wire bonding (gold-wire diameters from 20µm to 50µm).

Comparison between Flip Chip and Wire Bonding Assembly

The wire bonding technology has a large infrastructure of knowledge on the technique, manufacturing people, equipment vendors and materials [10]. The wire bonding technique is more mature than the flip chip technology. However, the flip technology has also advantages over the wire bonding. The required area for the flip chip assembly is much less than are needed for wire bonding assembly. Up to 95 % reduction in board area can be obtained using flip chip instead of wire bonding [4]. Also, the required height is smaller than for the wire bonding. However, the wire bonding is seen attractive solution with I/O counts less than 500 [11].

The possible number of I/O is much larger for flip chip technology. In wire bonding the pads have to be in the perimeter of the chip. A flip chip can have few thousands of I/Os [11]. The short interconnect length provides low inductance, resistance, and capacitance, small electrical delays and thus good high frequency performance. The underfill gives more reliability on the flip chip. The back side of the device gives efficient cooling for the device. [4,5,6]

There are also disadvantages concerning the flip chip technology: testing of bare dies is difficult, a separate process for making the bumps for the chips is needed (no chip modification in wire bonding), inspection of the hidden joints is difficult (an X-ray equipment is needed), accurate alignment in the assembly is required, and repairing of the assembly is difficult. [4,5,6,10]

High frequency Limitations of Flip Chip and Wire Bonding Assembly

In the wire bonding technology the length of the interconnection is relatively long thus increasing losses as the frequency increases. Flip chip technology is more advantageous as the interconnection length is very short. Thus it is expected that flip chip has good performance even at frequencies over 100 GHz [12]. Krems et al. have studied the performance of chip interconnection performance at millimetre waves both with modelling the interconnections and with experiments [12]. For an interconnection with a return loss better than 10 dB bond-wire length less than 0.033 wavelengths is required, e.g., at 94 GHz it is 100 microns. This can be improved by introducing an additional matching network. E.g, a 410 micron wire has 18 dB return loss at a frequency range from 55 GHz to 90 GHz. However this requires additional area on the chip [12]. The interconnection compensation circuits are studied also by others for millimetre wave applications, e.g. for flip-chip technique

at 38 GHz [13], flip-chip and wire bonding techniques for 51 GHz (measurements up to 75 GHz) [14], and flip chip interconnects for multichip modules at the frequency range from 10 to 100 GHz [15,16]. Jentzsch et al. report that return losses beyond 20 dB up to the frequency of 80 GHz can be achieved with flip chip technology [16].

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[9] http://www.flipchips.com/tutorial04.html

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2.2.1.1.4 EM coupling

It is desirable in some circumstances to eliminate the need for bond wires in the front-end of a system, by using electromagnetic coupling between the antenna and the circuit medium containing the active components. The benefits of eliminating bond wires include reducing costs, improving repeatability and removing parasitic reactances. The second two effects are particularly important in the mm-wave bands.

The idea of forming the antenna itself in the top metallic layer of a MMIC substrate has been investigated by several researchers, including at Birmingham [Singh et al. 2000]. In the low microwave bands this leads to a difficult trade-off between size and cost on the one hand and antenna performance on the other hand. Reduced size microstrip H-antennas for around 6 GHz were demonstrated, but showed very low gain, as expected from fundamental electromagnetic considerations. This led to the idea of forming a leaky semi-lumped element resonator on the MMIC, with a parasitic patch antenna positioned above it and coupled to it to form a more efficient radiating element, as illustrated in Figure 2.2-2[Song et al. 2003]. The parasitic antenna can be mounted conveniently onto the semiconductor package.

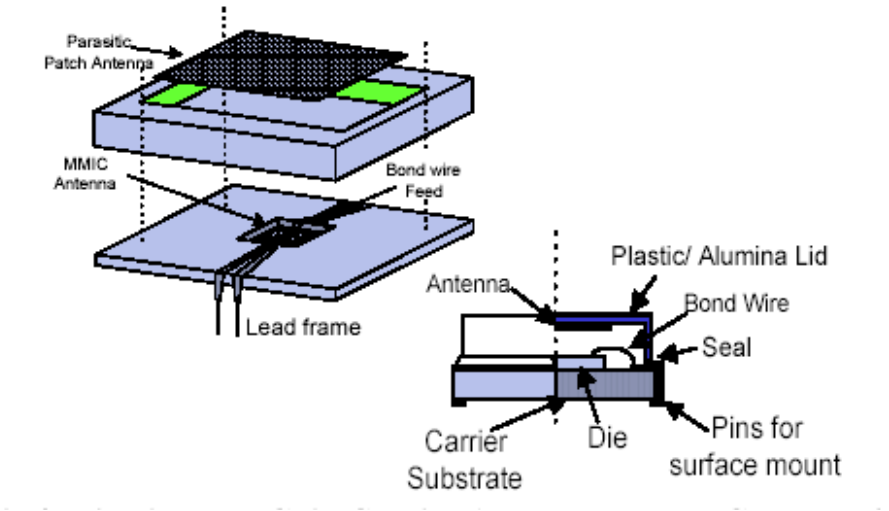


Figure 2.2-2: Parasitic Antenna on a Chip Package

Another form of EM coupling is the aperture coupled patch antenna. A common ground plane is sandwiched between two substrates, one for a microstrip circuit and one for a microstrip antenna. A resonant aperture slot in the ground plane couples energy between the two. To maximise the coupling, the feeding line on the circuit side is normally terminated in an open circuit, and the aperture is positioned under the line, approximately a quarter of a guided wavelength back from the open circuit, thus creating a maximum in the H field to excite the slot.

Aperture coupling of this sort has been demonstrated at Birmingham by Ma, Gardner and Hall [Ma et.al. 2001] , as illustrated in Figure 2.2-3, with a dual band U slot antenna, operating at 920 and 1828 MHz. Investigations of higher levels of integration are underway, in which the high current needed to excite the aperture will be generated using two closely spaced active devices, driven differentially, instead of the conventional distributed line method.

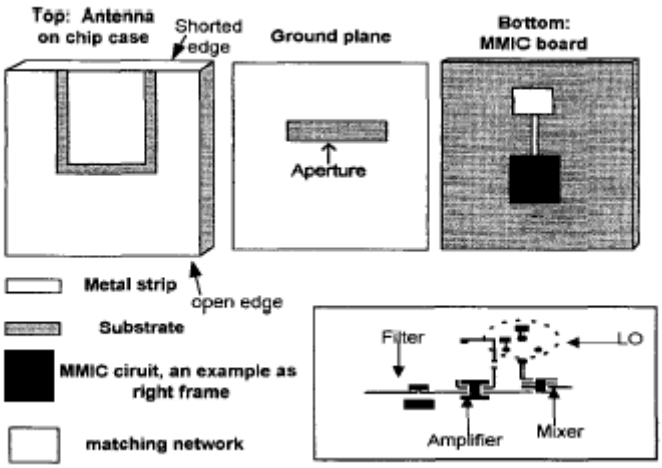


Figure 2.2-3: Aperture Coupled Dual Band Antenna on a Chip Package

References

[1] Singh, D., Kalialakis, C., Gardner, P. and Hall, P.S., Small H-shaped antennas for MMIC applications," Antennas and Propagation, IEEE Transactions on , Volume: 48, Issue: 7 , Pages 1134 – 1141. 2000

[2] Song, P.C.T., Hall, P.S. and Ghafouri-Shiraz, H., "Novel RF front end antenna package," Microwaves, Antennas and Propagation, IEE Proceedings, Volume: 150, Issue: 4 , Pages 290 – 294. 2003

[3] Ma, G., Gardner, P. and Hall, P.S., "Dual band antenna mounted on chip case," Antennas and Propagation Society International Symposium, 2001. IEEE , Volume 3, Pages 436 - 439 vol.3. 2001

2.2.1.1.5 Waveguide – Microstrip – Transition

In high-frequency applications the questions arises how millimeter wave circuits can be handled and how antennas can be measured. In particular, the task is to handle frequencies above 50 GHz in the so called V- and W-band.
Up to now waveguide technology is used for circuits in V- and W-band. Waveguides offer the advantage of low losses and a well established standardisation. However, these waveguide measurements suffer from bulky and sensitive circuits. During the last years, first V-band connectors came onto the market. These connectors are basically coaxial connectors similar to common SMA connectors except size and price. Furthermore, a standard for V-band connectors has not been defined so that right now each supplier offers its own V-band connector. This situation is even worse for W-band connectors as wavelength limits physical size and demands very high mechanical precision during manufacturing and handling.

In Fig. 2.2-4 a waveguide measurement setup is shown for measurement of S-parameters. The conversion between RF and IF is performed in the mixers close

the waveguides reducing losses as only the comparably low IF frequency needs to be transmitted to the vector-network analyser. In this configuration for antenna measurements, only the waveguide and the mixer for down conversion have to be mounted onto a turntable for radiation pattern measurements.

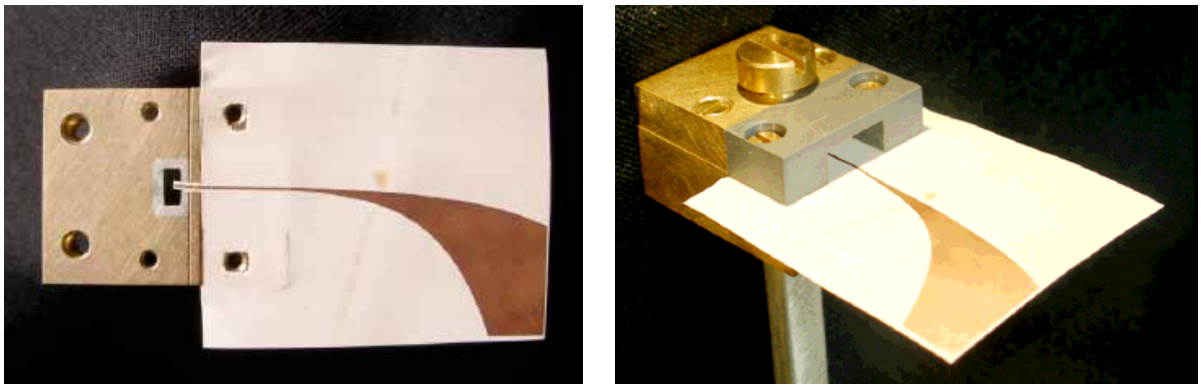


Figure 2.2-4: V-band wavguide-microstrip transition with stub-coupling and Vivaldi-Antenna.

For higher frequencies the physical dimensions of the waveguide and the transition have to be further reduced. The standardised waveguide dimensions for W-band are 1.28mm by 2.54mm and require high precision for fabrication and during measurements.

In Fig. 2.2-5 a waveguide to microstrip transition is shown with a tapered transition within the waveguide. The taper is replaceable to feature different shapes which can be optimised for the desired frequency. Additionally, a second transition can be placed in propagation direction to enable transmission measurements. In this setup microstrip lines can be measured without any constrains on their length. This 2-port configuration allows additionally in combination with a 180°-Hybrid-Tee the measurements of a Push-Pull type of antenna feed which is desirable at high frequencies due to the reduced power levels of the available sources.

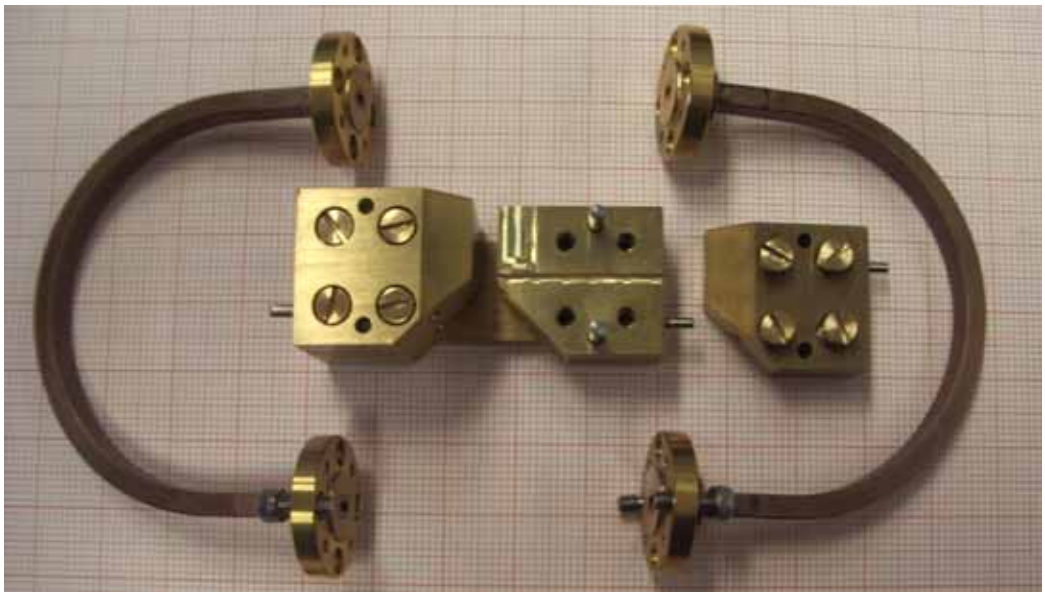


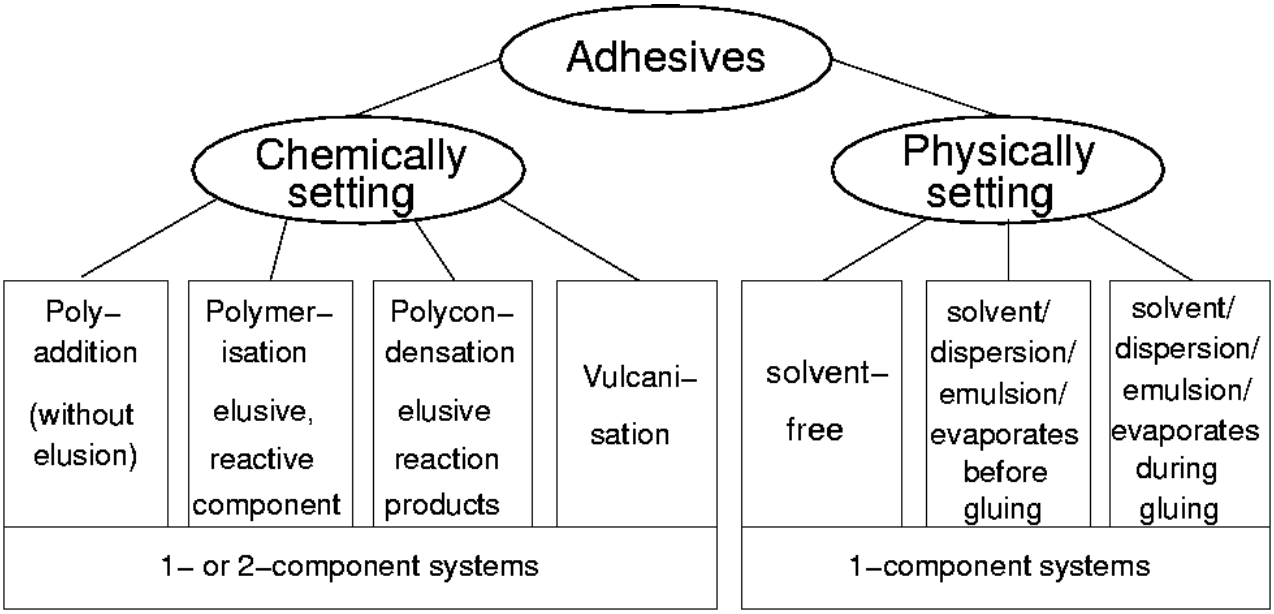
Figure 2.2-5: W-band wavguide-microstrip-waveguide transition with tapered transition for transmission measurements and for application in a Push-Pull setup.

Above 50 GHz measurement equipment is mainly waveguide based. There exist few commercially available setups for measurement on chip, but due to the lack of standartisation many measurements are performed by specialised equipment. This transition work well for laboratory purpose. High mechanical precision is demanded to adjust the matching in the transition.

2.2.1.2 Mounting Technologies

2.2.1.2.1 Gluing

The following document gives a short introduction into commercially available adhesives. Adhesives are coarsely separated into physically and chemically setting adhesives.



Physically setting adhesives:

This type of adhesives are directly brought to the joint/gap, i.e the polymer itself is put there. This approach requires a procedure to bring the glue into a processable form to the joint, and, later to harden it at the joint.

Solvent-containing wet-glues:

In the case of solvent-containing wet-glues, the polymer is dissolved in an organic solvent and can be directly processed on one surface. The connection has to be performed in a time-frame so that there is enough solvent in the glue to wet the second surface. The setting takes place by evaporation of the solvent and results in more toughness and finally hardens due to physical interaction between polymer chains.

Another possibility is cold welding (diffusive gluing) of thermo-plastics. In this case, the glue is applied to both surfaces and the solvent etches the surfaces. After as short time the two surfaces are pressed together. This results in a connection between polymer chains of both surfaces, which are pressed together. After evaporation of the solvent, the connection remains due to cohesive forces.

Dispersion glue:

Dispersion glues use water as a mobile phase, which carries the glue constituents. After application to the surface, the dispersion breaks due to water vaporization or change of the pH-value and forms a thin film, which then connects the surfaces.

Dispersion glues are preferred in comparison to wet-glues because they are not as combustible and explosive and do not have adverse health effects. The disadvantage either is the long time or the required amount of energy for hardening. Beyond that, they are not as frost-resistant as wet glues.

Hot-melt glue:

Hot-melt glue is solid at room temperature and can be processed after melting. The melted glue is applied to one surface. The surfaces are attached before cooling down in a certain time-slot. Directly after cooling down, the joint is hard and functioning. This enables direct further processing of the structures. Usually, hot-melt glues are free of solvents but their application is limited to temperature resistant surfaces due to the high processing temperatures (120... 240 °C). On the other side, hot-glue is reversible, which in consequence results only in limited temperature resistance (temperature range: -30°... +150 °C) .

Contact glue:

Contact glues can be either solvent containing wet-glues or dispersion glues, which are processed using a contact glueing approach. Initially, the glue is uniformly applied to both surfaces. After drying at air and detecting only a small adhesion strength, the surfaces must be accurately put together during the processing time. Afterwards, a correction or later adjustment is not possible. For good adhesion, the contact area must be pressed for a short time with high pressure. In the case of a flexible substrate, one has to use a roll for high line pressure. The joint can work under pressure directly afterwards. The final joint strength is reached after a few days.

Pressure sensitive adhesive:

Pressure sensitive adhesives remain sticky after application e.g. by pressure on a substrate. This glue is typically used for eticetts or adhesive foil among others.

Plastisol:

In the case of plastisols, small polymer balls are distributed in a liquid phase. The plastisol gelatinizes after thermal activation. The polymer balls absorb the liquid - which usually is a diluent -, swell and form a homogeneous layer. This kind of glue is typically used by car manufacturers for joint sealing or underbody coating (PVC-plastisol). Due to the low hardness and the high elasticity, the plastisols are assigned rather to sealing than to adhesives. (Gelatinizing temperature: 140° -200° C, hardness: 10 N/mm^2)

Chemically setting adhesives:

In the case of chemically setting adhesives - also called reactive adhesives - the single glue components are applied in a certain ratio to the joint. The hardening results from a chemical reaction between these components.

Basically, one distinguishes between two- or more component reactive glues and one-component reactive glues e.g. synthetic resin.

For 2-component adhesives, two constituents A and B, which can be resin and hardener, have to be intermingled before application to the surfaces. By mixing a chemical reaction starts and results in the adhesive polymer. In consequence, these glues are only processable during the so-called pot-time (maximum processing time). The progressing reaction results in continuous hardening, which after the pot-time does not allow the application of the glue to the surfaces. After application of the adhesive to the joint a certain time (setting time) is necessary for reaching final mechanical stability. The setting time is strongly influenced by external factors, especially temperature. An increase in temperature results in faster reaction and mostly in higher stability, while lower temperatures reduce reaction speed.

For 1-component adhesives, the glue is applied as is to the joint. The adhesive hardens due to a change of environmental conditions, which can be temperature increase, humidity increase, oxygen exclusion or contact to the surfaces.

The chemical reaction is coarsely separated in polymerization, polycondensation and poly-addition.

Cyanoacrylate adhesives:

Cyanoacrylate adhesives are commonly known as super-glues (in German: Sekundenkleber). They are low-viscosity or by purpose concentrated cyanoacrylic acid ester, in the case of 1-component glues usually monomers, reacting in the joint by polymerization to the adhesive polymer. A requirement for the initiation of the hardening process is the existence of polar groups, e.g. OH-ions, in the wet layer at the surfaces. The polymerization reaction occurs very quickly, and in consequence, mechanical stability is reached in seconds. This kind of glues is used for metal, glass or ceramics, which allow very small joints. For broader joints, the viscosity is increased (typically used for EPDM-rubber seals). Cyanoacrylate adhesives neither are humidity resistant nor temperature resistant because under these conditions the polymers are disrupted again.

Methyl methacrylate adhesives:

Methyl methacrylate adhesives are 2-component reactive adhesives, for which the used monomer - methyl ester or methyl acrylate acid - reacts by polymerase chain reaction. The reaction is initiated by a reactive radical, mostly originating from a peroxide, if mixed with an accelerator. Finally, the 2 components are only required for the initiation of the radical reaction. The peroxide is available as one component in methyl methacrylate monomer while the accelerator is diluted in the base monomer of the second component. By mixing both components the radical chain reaction is initiated and the adhesive hardens.

Another approach uses as the first component the entire monomer and the peroxide in one component and the accelerator as the second component. In this case, no mixing is required, if the first component is put on one surface and the second to the other. The chain reaction starts by attaching the two surfaces. This kind of adhesives is commonly used for metal gluing.

Anaerobic hardened adhesives:

This group of adhesives is used as 1-component system. The monomers of (modified) acrylate Esther harden by polymerase chain reaction comparable to methyl methacrylate adhesives. The peculiarity of this system is that the hardening reaction only takes place in the absence of oxygen (anaerobic reaction), if oxygen is excluded in a tight metallic joint. This behavior makes this adhesive usable for screw locking or flanch-shaft connections. (Pressure resistance: 40 N/mm^2, Temperature range: -55°... 200 °C)

Radiation hardened adhesives:

This group of 1-component glues hardens by polymerase chain reaction resulting in solid polymers, while the beginning formation of radicals is initiated by irradiation with UV-light (or other radiating sources, e.g. electrons). The wavelength of the UV-light has to be adjusted to the used adhesive system and at least one assembly component has to be transparent.

Phenol formaldehyde resin:

The basic components of this adhesive are Phenol (or Phenol-derivatives) and formaldehyde which condense as a polymer. This was one of the first reaction leading to a synthetic material (Bakelite). For gluing a Phenol formaldehyde mixture is used, which is not highly-molecular polymerised, and a formaldehyde supplier. This mixture is introduced into the joint as a dilution and powder and continues the condensation as a consequence of a temperature increase to 160... 180 °C. The two surfaces must be pressed together because water is generated as a decomposition product. The resulting adhesive has a very good temperature stability making it favorable for temperature loaded metal bonding. One field of application is the bonding of friction pads e.g. for friction brake pads or clutches.

Silicone:

Silicone polymers differ substantially from the other polymers mentioned in here because the backbone does not consist of carbon chains like for other organic polymers. In contrary, silicon and oxygen atoms alternate in the main chain. Organic structures only arise in the lateral chains. For gluing and sealing system pre-polymers are used, which have functional groups at chain ends, so that it hardens after exposure to humidity (1-component silicone) or after addition of a hardener (2-component system). Typical application is the sealing of joints in sanitary area.

Epoxy resin:

Epoxy resin or poly-epoxy resin are polymers from epoxy-segments. A 2-component system is used for the polymerization. It consists of resin and hardener. Polymer components with epoxy-groups at their end are used for Epoxy resin. Those are reaction products from Bisphenol-A and Epichlorhydrin. After intermingling with the hardener (containing Amino- or Mercapto-groups), they form a stable Duroplast. The hardening process takes place either at room temperature or at higher temperatures. The higher the temperature is, the higher usually is stability. The very high cohesion makes this adhesive usable for structural modifications e.g. with cars. A special case are the 1-component epoxy resin glues, for which the resin and the hardener component are intermingled in the correct ratio during fabrication and react after temperature activation. Those are especially used in the automotive industry as carcass adhesives.

(1-component: Temperature resistance up to 150 °C, Hardness: up to 29 N/mm^2, 2-component: temperature range: -30...+100 °C, Hardness: 30 - 40 N/mm^2)

Some suppliers:

- Ellsworth Adhesives http://www.ellsworth.com
- Wacker Chemie AG http://www.wacker.com
- Master Bond Inc. http://www.masterbond.com
- Adhesives Research GmbH http://www.adhesivesresearch.com
- Holdtide Adhesives http://www.holdtite.com

2.2.1.2.2 Soldering

Soldering uses a filler metal and an appropriate fluxing agent. The filler metal is typically an alloy with a melting temperature which is lower than the one from the pure metal (typ. below 350°C). The elemental filler metals which are typically used to form an alloy, their melting temperatures and resisitivities are given in the following table:

Elemental filler metal		Melting Temperature	Resistivity at 20 °C	
Tin	(Sn)	232 °C	115 nΩ·m	(at 0 °C)
Lead	(Pb)	327 °C	208 nΩ·m	
Antimony	(Sb)	631 °C	417 nΩ·m	
Bismuth	(Bi)	272 °C	1.29 µΩ·m	
Indium	(In)	157 °C	83.7 nΩ m	
Gold	(Au)	1064 °C	22.14 nΩ·m	
Silver	(Ag)	962 °C	15.87 nΩ·m	
Cadmium	(Cd)	321 °C	72.7 nΩ·m	
Zinc	(Zn)	420 °C	59.0 nΩ·m	
Copper	(Cu)	1085 °C	16.78 nΩ·m	

The most common solder is tin/lead-based. The eutectic version, Sn63/Pb37 has a melting temperature of 183 °C, the Sn60/Pb40 variation has a melting range of 183-188 °C. Higher lead versions of this alloy system have higher melting ranges. Often, 2% silver is added to the Sn63/Pb37 alloy to strengthen the alloy or to prevent excessive silver dissolution from silver plated circuitry. This alloy, Sn62/Pb36/Ag2 has a melting range of 179 °C – 188 °C.

As heat is gradually applied to solder, the temperature rises until the alloy's solidus is reached. The solidus is the highest temperature at which an alloy is completely solid. At temperatures just above the solidus the solder is a mixture of liquid and solid component. With further increasing the temperature, the liquidus is reached. The liquidus is the lowest temperature at which the alloy is completely melted. The solder remains in the fully liquid or melted state at temperatures above the liquidus. When removing the heat source, the cycle is reversed and the solder's physical form changes from completely liquid to liquid+solid and then to completely solid. Graphs that plot temperature vs. composition are known as phase diagrams and are widely used to determine the phases and intermetallic compositions of solder at a given temperature.

The range between the solidus and liquidus is known as the plastic region or zone of the solder. If the solder joint is mechanically disturbed while the assembly is cooling through the plastic region, the solder crystal structure can be disrupted, resulting in a high electrical resistance. Such solder joints with high electrical resistance are referred to "cold solder joints" and are undesirable. To avoid this problem, it is best to select a solder that has a narrow plastic range. There are some solder alloys that have no plastic region (liquidus equals solidus). These solder alloys are known as eutectic alloys. As heat is applied to a eutectic alloy, the solder passes directly from solid to liquid instantaneously at the eutectic melting point of the solder.

Solder paste is a mixture of a prealloyed solder powder and fluxing agent with high viscosity. The fluxing agent portion of the paste is made with rosin, activators, viscosity control additives, chemicals, stabilizers and solvents. The ratio of powder to fluxing agent varies with different alloys and different applications. Solder pastes are commonly used in electronics assembly for printed circuit PCB assembly in surface mount technology applications. An example of a typical use would be in the assembly of PCB used in computers and cellular (mobile) phones. Pastes can be "printed" through a stencil onto the circuitry. After printing, components are placed onto the bonding pad areas of the printed circuit and are held temporarily by the adhesion of the paste. Boards are then sent through a reflow oven where a specific temperature profile is used to evaporate the solvent, activate the fluxing agent, and melt the solder alloy. The type of fluxing agent used is dependant on the desired activity and whether or not cleaning is an option.

The fluxing agents usually contain rosin, acids (organic or mineral) and/or halides, depending on the desired fluing agent strength. These ingredients reduce the oxides on the solder and connecting pieces.

The purpose of a fluxing agent is to remove surface oxides on the substrate metallization, component leads, and the solder itself, to allow adequate wetting of the surface. The choice of flux is based on the substrate/component metallization to be soldered and/or the desired cleaning procedure. Metallizations that are likely to form persistent oxides will require a stronger flux. Similar to solder paste fluxing agents, liquid fluxing agents can be cleaned by solvent, water or they do not require a cleaning process at all. Fluxing agents are an integral part of the soldering process. In order for a good solder bond to form, the solder alloy must "wet" adequately to the substrate metal.

This means that no surface oxides can be present. Because most non-precious metals and alloys oxidize to some degree, the oxides must be removed. Flux performs have three basic functions:

1) Chemically dissolving oxides on the surface of the substrate metallization and the solder alloy itself.
2) Coating the solder joint location thereby displacing air, protecting the surface so that oxides do not reform during the soldering process. Since soldering requires elevated temperatures, there is more energy to form oxydes. Therefore, this function of preventing reoxidation during soldering can be just as important as removing the initial oxides.
3) Promoting the flow of the solder. Melted solder alloys are subject to surface tension physics just like any other liquid.

Some suppliers:

- IBL-Löttechnik GmbH http://www.ibl-loettechnik.de
- Advanced Integrated Technologies http://www.a-i-t.com
- SAB innotec http://www.reflowsystems.com
- CALEO Engineering http://www.robotherm.com
- Harotech http://www.harotec.ch
- Exselect Engineering Limited http://www.exselect.com

2.2.2 Module Level

2.2.2.1 Ceramic Packaging technologies

The primary ceramic package applications today fall into two categories: single-chip and multichip packages. Single-chip PGAs are the dominant ceramic package application. The highest-volume applications for PGA packages include computer and telecommunications products. The growth in multichip packaging is driven by the increased demands of advanced personal computers, workstations, mainframes, supercomputers, and evolving HDTV applications. Ceramics have also had improvements in materials, design, and process technologies. The state-of-the-art in ceramic packaging (see Figure 2.2-6), indicates that the current wiring dimension is about 50 micron and line spacing is about 100 micron. The number of layers used in ceramic packages is typically 20; however, IBM has used a 63-layer multichip module (MCM) in its R6000 workstation.

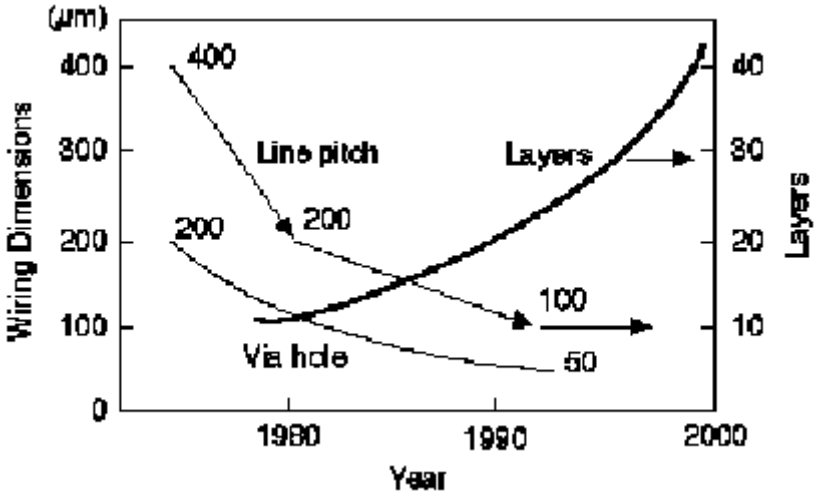


Figure 2.2-6: Ceramic packaging trends.

Materials

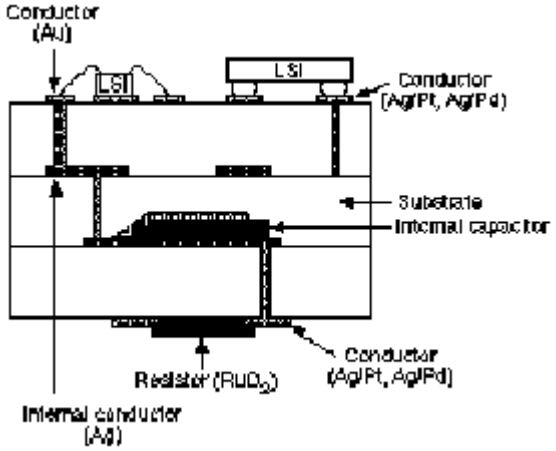
Table 2.2-1 shows the variety of materials being used with ceramic substrates. These materials include Al(sub)2O(sub)3, AlN, mullite, and a variety of glass-ceramics that include both glass added to alumina and crystalizable glasses. Whereas most of these low-temperature ceramics are metalized with Ag, Ag/Pd, or Au as fired in air, a few firms are beginning to co-fire with copper using special binders, or special atmosphere cycles, to remove organics from greensheets.

	Alumina	Mullite	AlN	Glass-Ceramic					
			(Ibiden)	Kyocera	Panasonic	Oki	Fujitsu	NEC	NTK
Thermal Conductivity (W/mk, RT)	18	5	180	2	2	2	2	2	2
T.C.E. (10^{-6}/°C) 40-400 °C	7.0	4.4	4.5	4.0	–	4-6	4.5	3.5	3.2
Dielectric Constant (1 MHz, RT)	10.0	6.8	8.9	5.0	7.4	4-5	5.6	4.4	5.0
TAN δ (1×10^{-4})	24	10	1	20	–	–	–	–	–
Conductor Metal	W, Mo	W, Mo	W	Cu	Ag, Cu	Au/Ag	Cu	Au	Cu
Sheet Resistance (mΩ/sq)	10	10	15	3	2 ~ 5	5	3	3	5

Table 2.2-1: Japanese Ceramic Substrate Materials

Technology

Of particular interest to the consumer electronics industry is the aspect of ceramic technology often referred to as LTCC (low-temperature ceramic carrier), currently metalized with Ag/Pd and co-fired with capacitors and resistors. The LTCC illustrated in Figure 2.2-7 was designed and developed for use in VCRs and other consumer video products by Panasonic at its plant in Saijo.



- Substrate (glass ceramic)
  - Dielectric constant 7.4
  - Thermal expansion coefficient 6.1 × 10^{-6}/°C
  - Flexural strength 2500 kg/cm²
- Conductor
  - Top Ag/Pd 15mΩ/□
  - Ag/Pt 5mΩ/□
  - Inner Ag 3mΩ/□
  - Ag/Pd 15mΩ/□
- Resistor
  - Top RuO_2 (10~1mΩ/□)
  - Inner -
- Capacitor
  - Top -
  - Inner
    - Capacitance 30nF/cm²
    - Dissipation factor 1.2%
    - Temp. char. Y5T

Figure 2.2-7: Consumer ceramic substrate (Panasonic).

Panasonic also designed and developed a low-cost process technology for co-firing with copper that is illustrated in Figure 2.2-8. This process involves forming thick films with CuO and co-firing in air to initially remove organics from greensheets and paste, and then reducing the oxide in forming gas, and finally forming a bond between glass that flows from ceramic walls and slightly oxidized copper in the via in Nitrogen atmosphere.

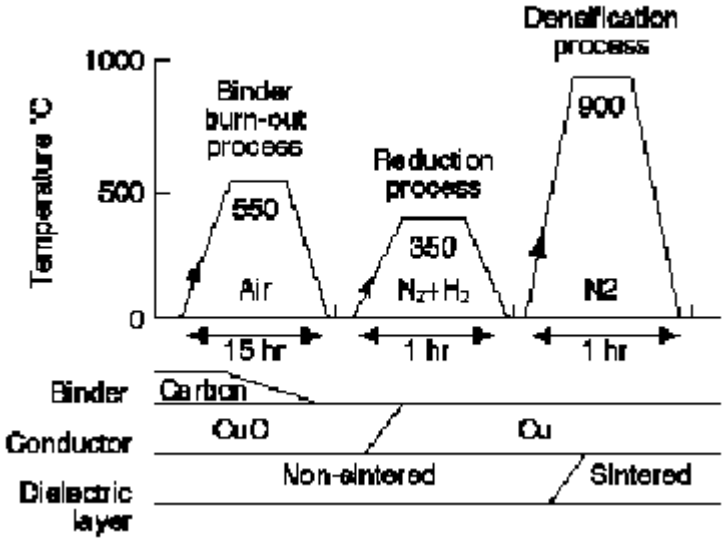


Figure 2.2-8: Low-cost ceramic co-firing process with copper.

Panasonic package designers expect to integrate capacitors and resistors into the substrate in the near future. Figure 2.2-9 illustrates glass ceramic/copper with surface resistors currently practiced by Panasonic.

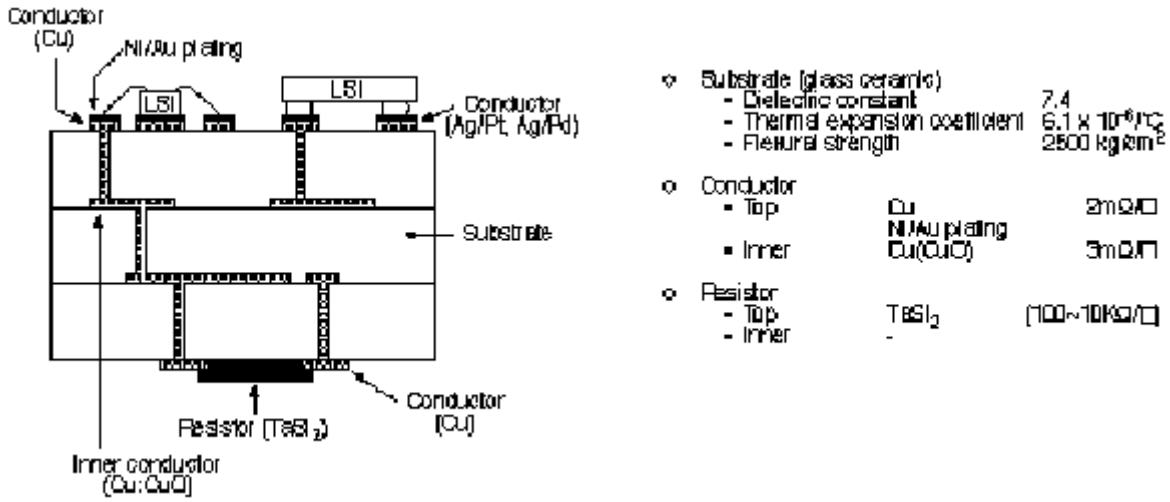


Figure 2.2-9: Consumer ceramic substrate with Cu (Panasonic).

The ceramic packaging technology roadmap followed by NEC during the last fifteen years is illustrated in Table 2.2-2.

1980	1985-1990 (G10)	1990	1995 (G100)
Alumina with W	Glass + Ceramic with Ag/Pd	Alumina + Glass Glass + Ceramic Ag Rich/Pd	Cordierite + Glass Glass + Ceramic Gold
$E_r = 9$ $\rho = 15\ \mu \cdot \Omega \cdot cm$	$E_r = 7.8$ $\rho = 10\ \mu \cdot \Omega \cdot cm$	$E_r = 4.4$ $\rho = 3.5\ \mu \cdot \Omega \cdot cm$	$\rho = 3.0\ \mu \cdot \Omega \cdot cm$

Table 2.2-2: NEC's Ceramic Roadmap

NEC is exploring ways to achieve an even lower effective dielectric constant. One approach is to develop hollow space between ground and signal planes (Figure 2.2-10). Plotting dielectric constant and signal propagation delay for various NEC materials, including the new material with and without the above hollow structure (Figure 2.2-11), shows that 4.4 material behaves normally with signal propagation delay of 7.6 nsec/m, but the hollow structure behaves as if it has dielectric planes. The transmission properties are greatly influenced by the configuration of ground plane and wiring plane open area and signal line channel.

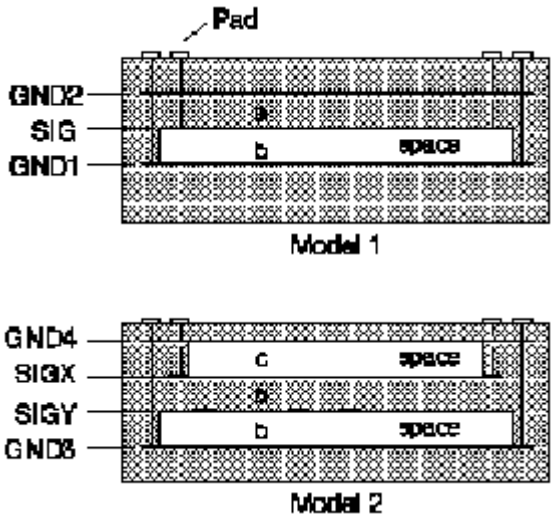


Figure 2.2-10: Hollow structure in ceramic for improved dielectric constant.

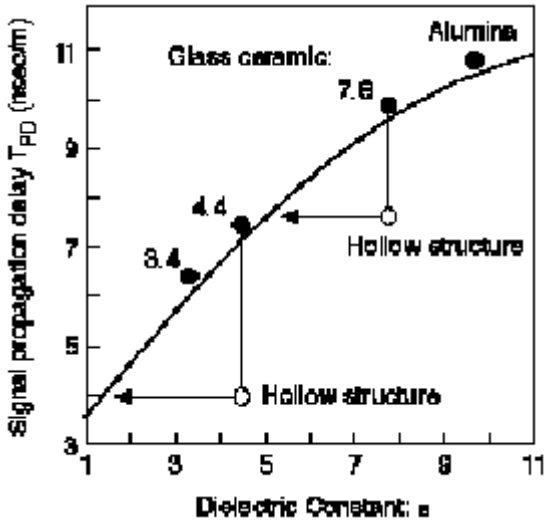


Figure 2.2-11: Propagation delay versus dielectric constant.

As illustrated in Figure 2.2-12, the rectangular open area seems to give constant overlap area between ground pattern and signal line, thus minimizing the capacitance variation that is typical of conventional square mesh patterns. NEC has applied this new material for a medium-cost, 156 Mb/s optical inter-connection module. In this application this technology has reduced (i) the number of modules to one from two from previous SMT/PWB technology, (ii) the volume size by one-seventh, and (iii) the power consumption by one-third. The total size of the final unit is 10 cc. NEC expects to use this new ceramic package in its personal computers as an interface to the CRT.

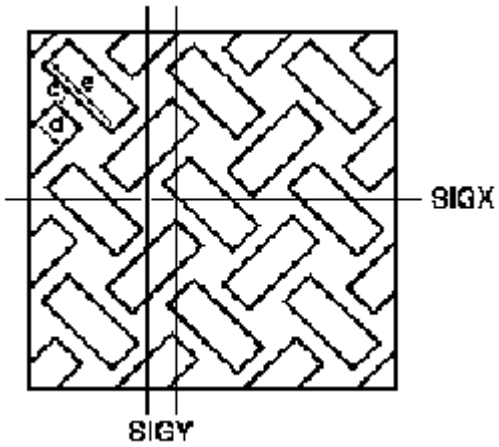


Figure 2.2-12: Package design improvement.

Use of aluminium nitride (AIN) is much more emphasized in Japan than in the United States. Ibiden, Kyocera, NTK, NEC, Toshiba, and Sumitomo Electric are some of the firms that have invested very heavily in developing and producing AIN pin grid arrays, as well as high-thermal-conductivity heat sinks. Ibiden, for example, makes a large substrate by hot pressing to achieve a thermal conductivity of 180 W/mk. NEC claims to have achieved as high as 200 W/mk and has transferred the technology to its subsidiary. The Japanese market for AIN

is currently estimated at $100 million per year, much less than previously projected. The primary reason for this slow growth has been attributed to the twenty to thirty times higher raw material cost over standard alumina and the one-half to two times higher substrate cost. NEC expects to use AIN for high-performance applications requiring higher thermal conductivity, where the additional cost can be justified. A new ceramic substrate approach being pursued by Ibiden involves bonding epoxyglass FR-4 layers to porous ceramic. Such a structure, illustrated in Figure 2.2-13, improves TCE, dielectric constant, and mechanical strength, and permits direct flip chip bonding.

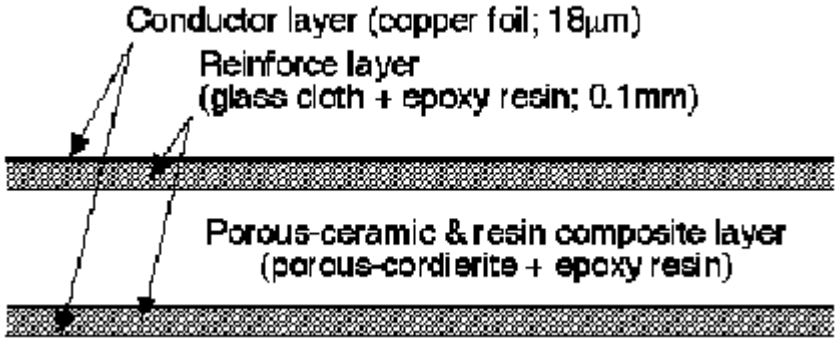


Figure 2.2-13: Ceracom substrate with low TCE and low dielectric constant.

The following Table shows IBM Single-chip module (SCM) and multichip module (MCM) configurations for product types with two I/O pitches

	CBGA		CCGA		LGA	
Substrate size mm	# I/O 1.27mm pitch	# I/O 1.00mm pitch	# I/O 1.27mm pitch	# I/O 1.00mm pitch	# I/O 1.27mm pitch	# I/O 1.00mm pitch
21x21	256	376				
21x25	304	456				
25x25	361	552	361	552	361	552
27x27	441	652	441	652	441	652
25x32.5	475	720	475	720	475	720
32.5x32.5	625	937	625	937	625	937
32.5x42.5			825	1247	825	1247
37.5x37.5			840	1272	840	1272
42.5x42.5			1089	1657	1089	1657
45x45			1144	1825	1144	1825
47.5x47.5			1284	2092	1284	2092
50x50			1432	2280	1432	2280
52.5x52.5			1588	2577	1588	2577

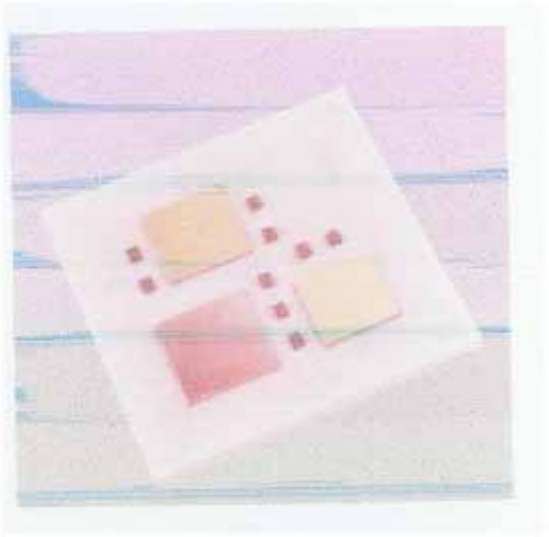


Figure 2.2-14: IBM multichip in alumina ceramic with flip-chip decoupling capacitor

The following Table shows IBM substrate dimensional properties for alumina and glass ceramic products.

	Dielectric Material	
Properties	**Alumina (9211) ceramic**	**Cordierite glass ceramic**
Fired layer thickness	0.110, 0.150, 0.200 mm	0.090, 0.113 mm
Number of layers	5-100+	5-100+
Body size	21.0-127.0 mm (JEDEC for SCM)	21.0-166.0 mm (JEDEC for SCM)
Line width	35, 50, 80, 90, 100 µm	70, 75, 100 µm
Line height	30-35 µm	22 µm
Line spacing	55-145 µm	110 µm min.
Minimum line pitch	112.5 µm	187.5 µm
Minimum via diameter	64 µm	75 µm
Via pitch	150, 225, 450 µm	187.5, 225, 450 µm
Edge/corner chamfer	Customer specification	Customer specification
C4 pitch	150, 200, 225, 250 µm	200, 225, 250 µm
C4 area array	Partial and full	Partial and full
Min. via cap diameter	76 µm	90 µm
BSM I/O type	BGA, CGA, LGA	BGA, CGA, LGA
BSM I/O pitch	1.00, 1.27 mm	1.00, 1.27 mm
LGA pad metallurgy	0.75 µm Au (electroless)	0.75 µm Au (electroless)

The following Figure 2.2-15 shows MLC cross section with three different SMT configurations and advanced cooling capability.

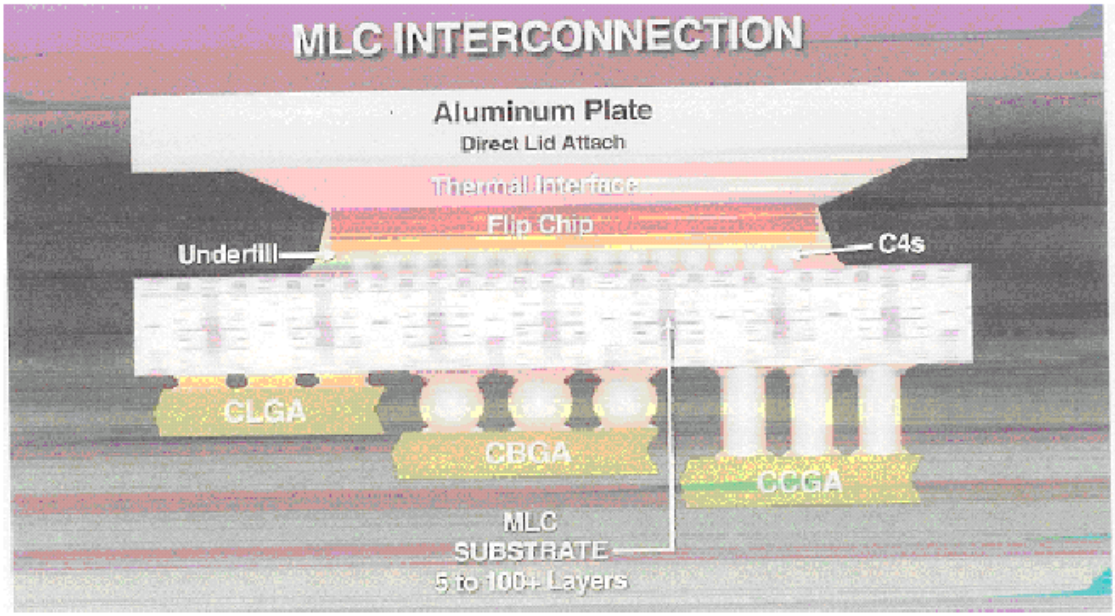


Figure 2.2-15

The following Table shows IBM substrate properties for alumina and glass ceramic product.

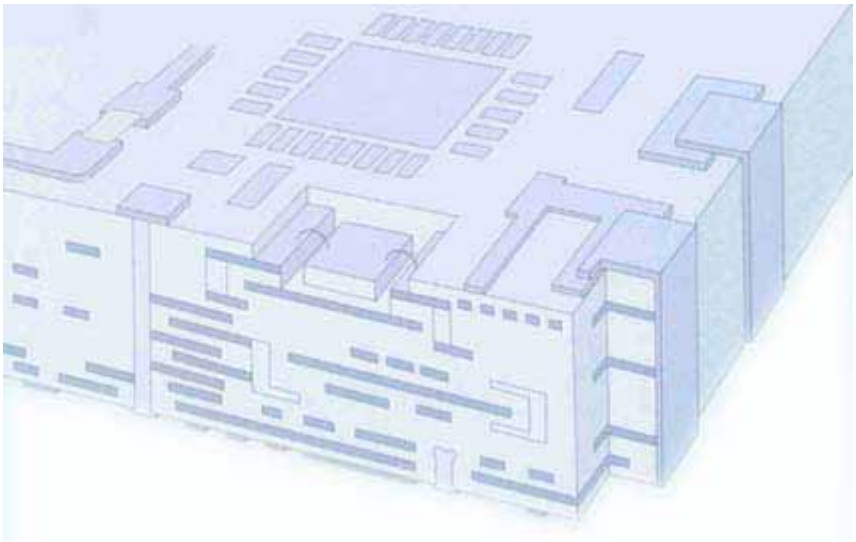
Properties	Alumina (9211) ceramic	Cordierite glass ceramic
Substrate color	White or dark	Red
Bulk density	3.6 gm/cc	2.6 gm/cc
Dielectric constant	9.5	5.0
Dielectric loss tangent	0.0005 @ 9.5GHz	0.0005 @ 9.5GHz
Dielectric resistivity	1 x 10^{15} ohms-cm (W)	1 x 10^{15} ohms-cm (W)
Thermal conductivity	19 W/m-k	5 W/m-k
Coefficient of thermal expansion	6.5 ppm/C	3.0 ppm/C
Conductor	Molybdenum	Copper
Conductor resistivity	10.0 µohms-cm	3.2 µohms-cm
Dimensional shrinkage tolerance	+/- 0.30%	+/- 0.15%
Camber/flatness	< 10.0 µm-cm	< 8.5 µm-cm
Flexural strength	420 MPa	190 MPa
Propagation delay	118 psec/cm	78 psec/cm
Characteristic Impedance (design range)	35-60 ohms	50-60 ohms
Line resistance (typical)	0.34 ohms/cm	0.22 ohms/cm
Via resistance (typical)	0.07 ohms/cm	0.05 ohms/cm
Capacitance (typical)	2.7 pF/cm	1.4 pF/cm

2.2.2.2 LTCC

The following description of LTCC technology is taken from the IMST web site at http://www.ltcc.de/index.htm. For more information and links to other relevant sites please go to their web pages.

OVERVIEW

The **L**ow **T**emperature **C**ofired **C**eramic (LTCC) technology can be defined as a way to produce multilayer circuits with the help of single tapes, which are to be used to apply conductive, dielectric and / or resistive pastes on. These single sheets have to be laminated together and fired in one step all. This saves time, money and reduces circuits dimensions. An other great advantage is that every single layer can be inspected (and in the case of inaccuracy or damage) replaced before firing; this prevents the need of manufacturing a whole new circuit.
Because of the low firing temperature of about 850°C it is possible to use the low resistive materials silver and gold instead of molybdenum and tungsten (which have to be used in conjunction with the HTCCs).



DESIGN RULES

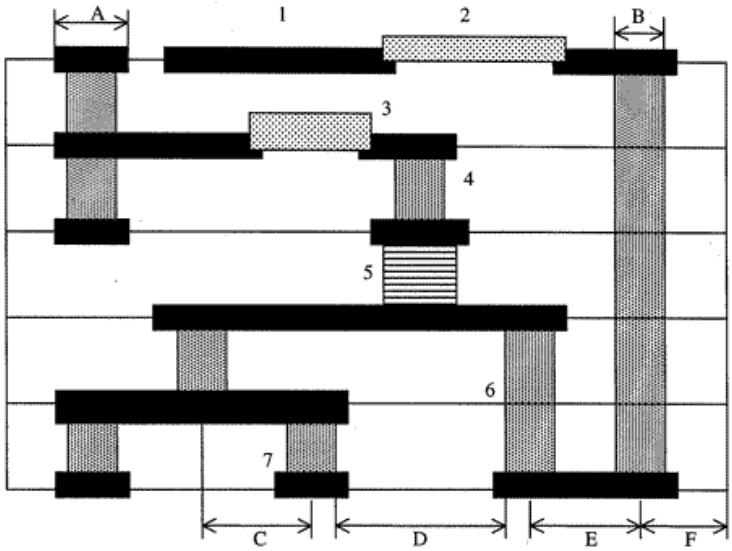
Because of the shrinking of the LTCC tapes during the firing it is very necessary to observe various design rules. This part is based on a few design guides published from the following manufacturers / processors:

- DuPont: LTCC-Technology Design And Layout Guideline Green Tape System (EKP,12.8.1998);
- CTS Microelectronics: Low-Temperature Cofired Ceramic Design And Layout Guidelines For The Fabrication Of Networks, Packages and Multichip Modules;
- National Semiconductor: Design Rules For Physical Layout Of Low Temperature Co-Fired Ceramic Modules (Version_8.1);
- Scrantom Engineering Inc.: Low Temperature Cofired Ceramic Design Guidelines (Rev. C);

- Siegert electronic GmbH: Design Rules For LTCC (Rev. C);
- Sorep-Erulec: General Design Guide For LTCC Substrates (8-jan-99).

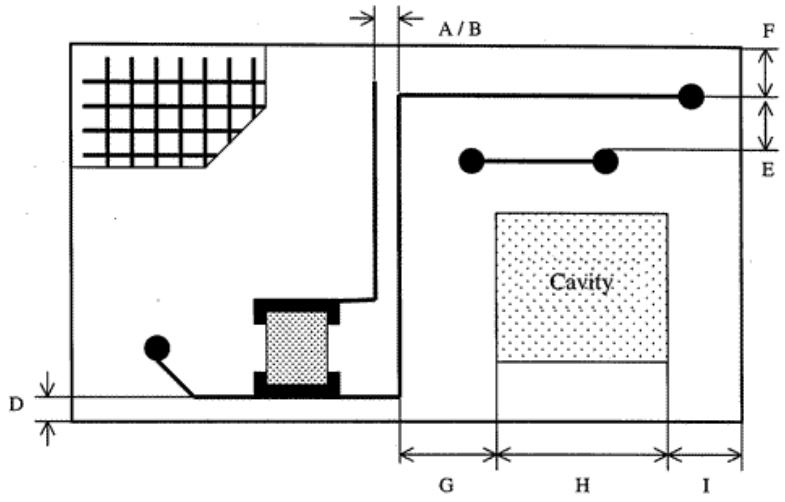
All called numbers are average values and ranges and may vary from one to the other system; these rules depend on both material and process properties. This paper doesn't intend to describe all known design rules; it should only give an idea about the possibilities of LTCCs.

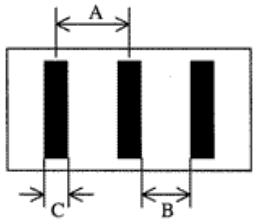
Terminology for Design Rules



1 : Top Side External Conductor
2 : Cofired or Postfired Surface Resistor
3 : Buried Resistor
4 : Buried Via
5 : Buried Capacitor
6 : Stacked Vias
7 : Blind Via

A : Via Cover Pad
B : Via Diameter
C : Via Stagger
D : Via Spacing
E : Via Pitch
F : Via Center To Part Edge





A : Line Pitch
B : Line Spacing
C : Line Width
D : Conductor To Part Edge / Edge To Feature
E : Via To Conductor Line Spacing
F : Via Center To Part Edge
G : Line To Cavity Wall Spacing
H : Cavity Size
I : Cavity Wall To Part Edge Spacing

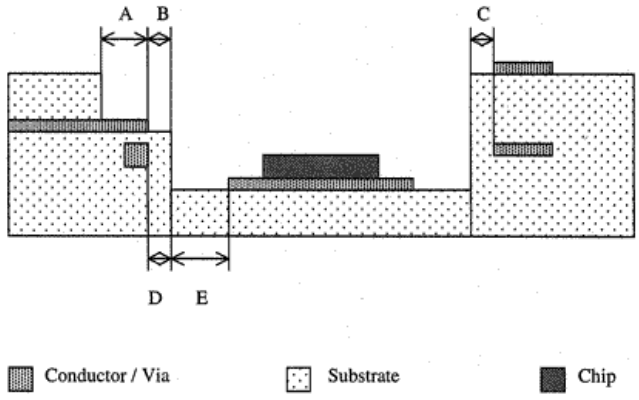
Table Of Main Values

	Standard	Possible
Edge To Feature in um	500	250
Line Width in um	200	100
Line Width in um (Fine Line Process)	50	50
Line Spacing in um	200	100
Line Spacing in um (Fine Line Process)	50	50
Line Pitch in um	400	200
Line To Cavity Wall Spacing in um	400	/
Via Diameter in um	250	100
Via Coverpad / Catchpad	2x via diameter	via diam. 25um
Via Spacing in um	200	175
Via Pitch in um	400	300
Via Stagger	1.5x via diameter	/
Via To Cavity Wall Spacing in um	400	/
Via Center To Part Edge in um	550	300
Via Geometry	Round + Rectangular	Round + Rectangular
Via Types	blind, buried, stacked	blind, buried, stacked
Thermal Via Coverage in %	15	30
Min. Resistor Dimensions in mm	1 x 1	0.5 x 0.5
Min. Resistor Overlap in um	300	200
Min. Width After Trimming in um	300	200
Tolerance After Trimming (Surface / Buried)	+/- 2% / +/- 25%	+/- 1% / x
Ground / Power Plane Coverage	50%	75%
Opening For Feed Through (length in um)	750	350
Max. Number Of Layers	*Depends on Thickness (10 - 50)*	*Depends on Thickness (10 - 50)*
Min. Number Of Layers	*Depends on Thickness (2 - 4)*	*Depends on Thickness (2 - 4)*
Circuit Shapes	Rectangular, special shapes possible	Rectangular, special shapes possible
Size Tolerance	+/- 0.5%	+/- 0.25%
Cavity's Shape	Rectangular, circular, special shapes possible	Rectangular, circular, special shapes possible
Min. Floor Thickness in um	450	200
Max. Cavity Depth in um	1500	2500
Min Cavity Size in um	1000	500
Max. Cavity Size in um	*Depends on layout*	*Depends on layout*
Cavity Wall To Part Edge Spacing in um	>1000	/
Bond Pad / Conductor Discoverage in um	750	/
Cavity Wall To Conductor Spacing in um	400	/

	Standard	Possible
Cavity Wall To Via Spacing in um	2.5x via size	/
Cavity Wall To Pad Spacing in um	250	/
Spacing Between Two Cavities in um	1270	/
Window's Shape	Rectangular, circular, special shapes possible	Rectangular, circular, special shapes possible
Window Depth in um	< 2000	> 2000
Min. Window Size (length in um)	1000	500
Max. Window Size (length in um)	*Depends on layout*	*Depends on layout*
Pitch Of BGA / LGA I/Os in mm	2.54	0.635
Wire Bonding Pitch in um	500	150
Solder Pad Pitch in um	400	250
Flip Chip Bonding Pitch in um	400	250

Cavities / Windows

Cavities are openings in the ceramic through a various number of layers with a bottom; windows are openings through the hole ceramic without a bottom.



A : Bond Pad / Conductor Discoverage

B : Cavity Wall To Bond Pad Spacing Conductor Spacing

C : Cavity Wall To Conductor spacing

D : Cavity Wall To Via Spacing

E : Cavity Wall To Die Pad / Bottom

	Standard	Possible
Cavity's Shape	Rectangular, circular, special shapes possible	Rectangular, circular, special shapes possible
Min. Floor Thickness in um	450	200
Max. Cavity Depth in um	1500	2500
Min Cavity Size in um	1000	500
Max. Cavity Size in um	*Depends on layout*	*Depends on layout*
Cavity Wall To Part Edge Spacing in um	> 1000	/
Cavity Wall To Bond Pad Spac. in um (B)	250	/
Bond Pad / Conductor Discover. in um (A)	750	/
Cavity Wall To Conductor Spac. in um (C)	400	/
Cavity Wall To Via Spacing in um (D)	2.5x via size	/
Cavity Wall To Pad Spacing in um (E)	250	/
Spacing Between Two Cavities in um	1270	/

Note:

- If cavities need to be processed it is advisable to use an isostatic press for lamination;
- Deep cavities need to have inlays during lamination.

	Standard	Possible
Window's Shape	Rectangular, circular, special shapes possible	Rectangular, circular, special shapes possible
Window Depth in um	< 2000	> 2000
Min. Window Size in um	1000	500
Max. Window Size in um	*Depends on layout*	*Depends on layout*

DESIGN TOOLS

Empire

EMPIRE™ is one of the leading 3D electromagnetic field simulators based on the powerful Finite Difference Time Domain Method. Its applicability covers the 3D-EM design and modelling of nearly all passive devices. Especially for multi-layered RF components and for antennas on LTCC. EMPIRE™ has been proven in practice in a huge number of applications. This experience is offered to design RF modules for customers applications.

Highlights are

- Accurate 3D modeling, utilizing a speed optimized FDTD kernel (Finite Difference Time Domain Algorithm)
- Easy-to-use interface
- Import / export of layout data supporting common standards
- Developed and supported by experienced RF design engineers
- Proven in practice within industrial and public projects
- Software and application support available

Updated frequently with latest developments in research and new features.

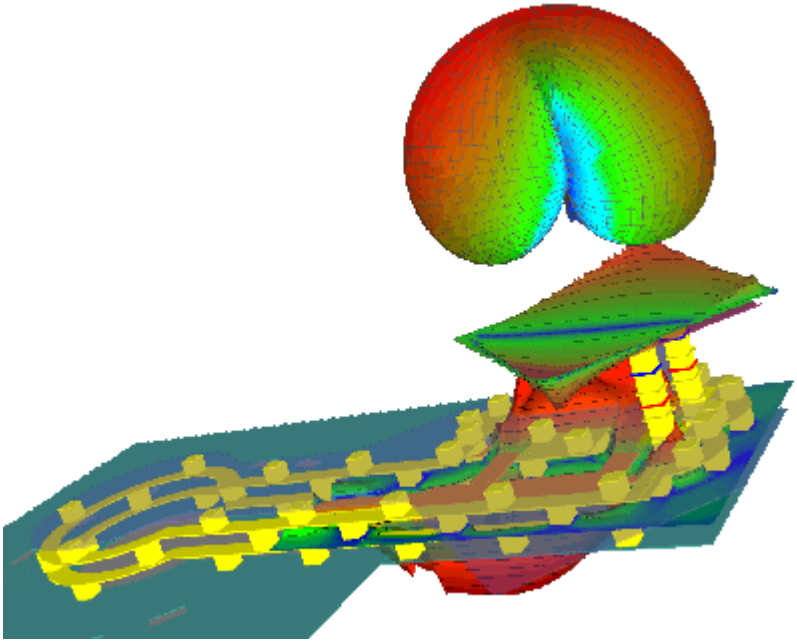


Figure 2.2-16: Illustration of far-field and E-field distribution of a circular polarzied antenna patch on multilayer LTCC simulated with EMPIRE, which is based on the 3D Finite Differences Time Domain method.

MultiLib

MultiLib™ is the new state-of-the-art model library, which includes all standard elements for analog high-frequency multi-layered circuit designs. As an add-on to Agilent‘s ADS™, MultiLib™ is very easy to use for the simulation, design, and layout of multi-layered RF circuits.

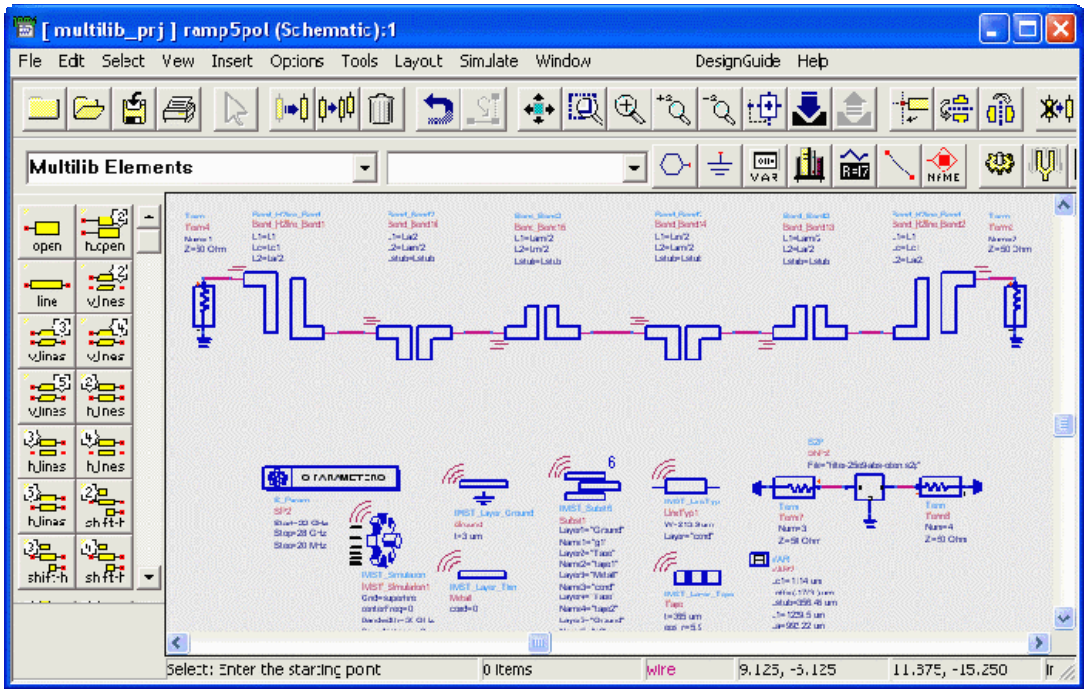


Figure 2.2-17: Filter schematic with MultiLib elements in Agilent‘s ADS™

MATERIAL SUPPLIERS

The following companies offer LTCC tapes for various applications.

DuPont
- 951: k = 7.8 (standard tapes: CT, AT, A2, AX)
- 943: k = 7.5 (low loss tape)

Ferro
- A6M: k = 5.9 (microwave tape)
- A6S: k = 5.9 (low cost microwave tape)

Heraeus
- HL2000: k = 7.3 (HERALOCK; near zero shrink)
- CT2000: k = 9.1
- CT700: k = 7.5 - 7.9
- CT800: k = 7.5 - 7.9 (zero shrink tape)

CeramTec
- Ceram*tape* GC: k = 7.9
- Ceram*tape* A (Alumina for constrained sintering)

ESL Electro-Science
41110-25C: k = 4.0 – 5.0 (transfer tape: zero shrink)
41010-25C: k = 7.2 – 8.2 (transfer tape: zero shrink)
41020-25C: k = 8.0 – 10.0 (transfer tape: zero shrink)
41110-70C: k = 4.3 – 4.7
41020-70C: k = 7 – 8

Kyocera
GL550: k = 5.6 - 5.7
GL660: k = 9.4 - 9.5

Nikko
Ag2: k = 7.8
Ag3: k = 7.1

Northrop Grumman
"Low K": k = 3.9

Samsung
TCL-6A: k = 6.3
TCL-7A: k = 6.8

2.2.3 Advanced Packaging: Wafer Level Packaging

The concept of chip-scale of chip-size packaging (CSP) was introduced in 1990's, and four categories of CSP were identified by 1998: flex interposer, rigid interposer, leadframe-based and wafer level [1]. In 1998, the flex-based CSPs were most widely used, but the wafer level CSPs were not near production [1]. However, the commercialization of the chip scale wafer level packaging or WLP was started in 2000 [1]. Today wafer level packaging technology is widely used.

The wafer level packaging is a technology, where, in addition to processing the device, all steps of IC packaging are performed at wafer level before dicing [3,4]. The following requirements has to be fullfilled: the footprint of the WLP is the same as of the die, the package is completed before dicing, and the packaged device should fit in to the standard surface-mount assembly process [3]. The WLP package can be tested after the packaging resulting in a known good package [3]. Wafer-level packages (WLPs) are interconnected to the board using solder balls like flip chips; now the underfilling is processed also in the wafer level [4,7]. There are different opinions on what is exactly the definition on wafer-level package, e.g., some count redistributed wiring flip-chip, while others insist greater physical protection. However, basic requirement has been agreed to be that the finished device should be mountable using standard surface-mount assembly techniques [2].

The benefits of the WLPs are that they are fabricated and tested in wafer level before dicing the wafer, thus their costs go down as the wafer size increases and the die shrinks. On the other hand all the dies are packaged, even though they are not good, because tests are done after packaging. One disadvantage of WLP is that interconnects are located under the die and very large I/O die requires very small solder balls on very tight pitch. Technically it is feasible to manufacture solder balls down to 50 µm or even smaller [5], but they require very high-density PWB (printed wiring board) to interconnect the I/O. This kind of microvia PWBs are very expensive. The tightest board pitch currently in use is 0.5 mm. [4]

All WLP technologies result in packaged area array chips, where all the interconnects are under the device. There are basically three different WLP technologies depending on processing steps [1,5]:

1) Redistribution technologies: redistribution is done in the initial process to achieve area array. Development of this technique is done by IZM-Berlin, Fujitsu, Oki, FCT, and Unitive. [5]
2) Encapsulated technologies: wafer is encapsulated in thin glass or silicon wafers. Development of this technique is done by Shellcase, Intarsia, and Chipscale. [1,5]
3) Flex tape technologies: film is attached to the surface of the wafer to provide the rerouting. Suppliers of this technique are Tessera and Amkor [5].

Of these three technologies the redistribution technologies are most widely used [1].

Redistribution technologies

The Ultra CSP redistribution technology is developed by FCT. Metallization of Al/NiV/Cu is used for redistribution and BCB (Benzocyclobutene) as the interlayer dielectric. Eutectic and high-lead solder balls are screen-printed or placed as preformed solder balls and Lead-free solutions are available. FCT redistribution technology has been licensed by ASE (Kaohsuing, Taiwan), SPIL (Taichung, Taiwan), California Micro Devices (Milpitas, California) and Amkor (Chandler, Arizona). [4,5]

The Super CSP is developed by Fujitsu. Redistribution to area array is achieved using metallization of Ti/Ni/Cu and PI (Polyimide) as dielectric. Copper posts are then plated (100 µm) on the area array pads, and Ni/Pd barrier layers are plated on top. Solder balls are aligned to the exposed Cu studs, and transferred and reflowed on the CSP. This technology is scaled up by Shinko (Nagano, Japan). [4,5]

The Xtreme CSP technology is developed by Unitive and it consists of products using Cu/BCB, solder or Al/BCB redistribution, a phased Cr/Cu or Ti/Ni UBM, and electroplated (up to 200 µm) or placed preformed (>250 µm) solder balls. This technology has been licensed by Dallas Semiconductor, Unitive Taiwan and Amkor. [4,5]

The chipCSP technology developed by Chipbond uses a Cu/BCB redistribution and solder plating technology. [4]

National Semiconductor has developed a WLP known as microSMD (surface mount device). The solder bump under bump metallization is deposited on a BCB repassivation layer. Similar low I/O redistribution wafer-level packaging technology has been commercialized by Dallas Semiconductor (One Wire), Atmel (dBGA), Xicor (X-BGA), Bourns and several others. [1]

Encapsulated technologies

In the Shellcase CSP technology the chip is sealed between glass plates. The peripheral pads on the die are extended into the dicing streets using Al/BCB interconnect. The face of the wafer is glued to a plate of glass and the wafer backside lapped down to 100 µm thickness (total thickness of the package is 0.3 to 0.5 mm). The backside of the wafer is sealed in glass and is partially sawn to expose the extended pads. The wafer is metallized and the area array leads are defined by lithography. Under bump metallisation is then deposited and bumps are attached. After that the die is tested and diced. [4]

The MicroSMT technology is used by Intarsia (licensed from Chipscale). It produces integrated passive componens on both silicon and glass. Silicon or glass is bonded to the active side of the silicon or glass wafer with epoxy to provide protection and structural support. The capping wafer is ground to form a parallel surface, and then the device wafer is ground to about 100 μm. Wet etching process is used to access bond pads on the device wafer. A proprietary conformal polymeric isolation is processed. Metallization, solder mask and solder ball attachment are following steps to complete the packaging. [5]

Flex tape technologies

Amkor has developed wsCSP technology, in which a redistribution pattern on Cu/PI flex tape is attached to the wafer with adhesive. Wirebonds are used to connect chip from the chip pads to the film. Liquid encapsulant protects the wire bonds and bond pads. Amkor has announced that it will not manufacture this package and subsequently has licensed the FCT and Unitive redistribution technologies for scaleup in Korea. Tessera (San Jose, California) has also studied the technical and commercial feasibility of such flex tape-based processes. [4]

Form Factor has developed a microspring technology MOST™, evolved from burn-in and test technology. "S"-shaped gold wires plated with nickel spring alloy are bonded to the bond pads forming microsprings. [5]

Wafer-level test

Wafer-level burn-in and test have to be carried out for low-cost wafer-level chip-scale packaging (WLCSP). FormFactor, Matsushita, Micronics Japan, and Gore/Motorola/Tokyo Electron have developed non-destructive probing technologies for wafer-level testing and burn-in of bumped wafers. [1]

Applications

The wafer level packaging technology is expected to remain for low pin counts, less than 100, and for small die sizes. Several types of memory are shipped in WLPs, e.g., EEPROM, flash, SRAM, and DRAM. Also, SDRAM for graphics, embedded and wireless applications are sampled by Micron. Multiple wafer-level diode products for ESD protection and high-speed signal line protection for digital cameras, mobile phones, and MP3 players etc. are shipped by Bourns and Littelfuse. Integrated passive devices for mobile phones and PDAs are shipped by AVX, California Micro Devices, Philips, STMicroelectronics and Telephus. Fairchild and Maxim are selling power management devices in WLP form factor, e.g., the Maxim battery management device. [1,7,8]

Wafer level packaging has been adopted for MEMS applications because packaging of MEMS devices is one of the major cost issues. MEMS devices have often a basic problem that the device has to interact with the environment without restrictions caused by the packaging that also protects the device from environment. Wafer level packaging can be used if the active sensor area is on the other side of the devices and interconnects are placed on the backside of the sensor. [1]

Schott Electronic Packaging has introduced the Schott OPTO-WLP technology for optical sensor applications, which is also a suitable technology for MEMS packaging. First, the sensitive structures are protected by a cover glass. A special adhesive wafer bonding process enables a selective coverage of the adhesive within the bond layer. After that, the backside or silicon side is thinned to about 100 μm depending on the application. Plasma etching is used to further process the silicon. Dielectric layers are used to provide electrical isolations for the redistribution process. BCB is used as dielectric and copper or aluminium connector. After redistribution the under bump metallization is processed and solder balls are placed. [1,9]

Suppliers for WLPs

Table 2.2-3 shows the merchant suppliers for wafer level packaging listed in reference [1]. Table 2.2-4 shows the institutes performing wafer level package research and development with component manufacturers [1].

Wafer level foundries	Technology	Location
ASE	Ultra CSP	Taiwan
Amkor	Ultra CSP Xtreme CSP	Korea
Chipbond		Taiwan
FlipChip International	Ultra CSP	Arizona
Fujitsu	Super CSP	Japan
Siliconware	Ultra CSP	Taiwan
STATS	Ultra CSP	Singapore
Unitive (Amkor)	Xtreme CSP	North Carolina
Captive Production		
Dallas Semiconductor (Maxim)		Texas
National Semiconductor	microSMD	Malaysia

Table 2.2-3: Merchant Wafer-Level Packaging [1].

Institute	Location
Fraunhofer-IZM	Berlin
MCNC-RDI	North Carolina
IMEC	Belgium

Table 2.2-4: Institutes performing wafer level packaging research and development with component manufacturers [1].

Achievable Frequencies and Losses of Wafer Level Packaging

Garchon et al. studied both theoretically and experimentally the electrical characteristics of high Q inductors and transmission lines in the wafer level packaging [10]. A peak Q-factor of 38 was obtained at 4.7 GHz for 1-nH inductor. Next to inductors coplanar waveguide (CPW) and thin film microstrip line (TFML) were realized. These transmission lines were measured to have losses of 0.2 dB/mm (CPW) and 0.12 dB/mm (TFML) at 25 GHz [10].

Park et al. studied RF-MEMS packaging with WLP techniques at frequencies up to 3 GHz [11]. The loss of the overall package was tested to be within 0.05 dB.

Polyakov et al. proposed a high-resistivity polycrystalline silicon (HRPS) as a low-cost and low-loss substrate for radio-frequency passive components in wafer-level packaging and integrated passive networks. They report inductor for 1 GHz having Q-value of 11, and coplanar waveguide having loss of 0.65 dB/cm at the frequency of 17 GHz [12].

Bakir et al. presented a high-density wafer level packaging technology, where the insertion loss of leads is less than 0.4 dB at the frequency range of 0.1– 45 GHz [13]. Worst-case insertion loss of the signal propagation into and out of the package is reported to be 1.15 dB at 45 GHz.

Wang et al. presented a RF filter which is hermetically sealed with wafer level packaging [14]. The filter has passband at 1930-1990 GHz and the insertion loss in the passband is less than 2 dB. The broadband attenuation outside the passband is better than 35 dB.

Seki et al. reported a RF-MEMS switch with an insertion loss of 0.5 dB and an isolation of 30 dB up to 10 GHz [15]. The switch was with Chip Scale Packaging (CSP) structure utilizing wafer level packaging technology.

Majumder et al. reported a broadband ohmic RF-MEMS switch which is hermetically sealed with wafer level packaging [16]. DC on-resistance of the switch is less than 1 Ohm with an actuation voltage of 80 V. RF characteristics of a 4-contact microswitch at 2 GHz are an insertion loss of 0.32 dB and isolation of 33 dB. For an 8-contact switch insertion loss of 0.27 dB and isolation of 12 dB are reported [16].

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2.2.3.1 Packaging solutions dedicated to MEMS

Packaging needs to be considered as a part of a MEMS components since it allows to use the MEMS functionality within specification during the life time of the subsystems it uses it. More specifically packaging for MEMS enables : environmental protection, mechanical protection, hermeticity (if needed), electrical interconnects, heat dissipation, handling during process and mounting.

In is indeed even more important for RF MEMS as packaging has a strong impact on the performance of the device itself. It contributes to about half of the insertion loss budget (at frequency over 10 GHz) of the RF MEMS component.

Packaging can be achieved following different techniques that are described in the following paragraphs.

2.2.3.1.1 Wafer bonding techniques

Bonding method	Temperature °C	Hermeticity	Reliability	Bond strength MPa	Comments
		Surface bonding			
anodic bonding	medium, 200–500	yes	good	>30	requires flat surface, high voltages
fusion bonding	very high, 700–1400	yes	good	>20	requires surface preparation, flat surface
surface activated bonding	very low, RT*–200	yes	not certain	>10	requires flat surface, surface preparation
		Metallic interlayer			
eutectic bonding	medium, 180–400	yes	not certain	20	particle insensitive
thermo-compression bonding	medium, 350–500	not certain	not certain	10	very high pressure required
solder bonding	low, 180–300	yes	not certain		particle insensitive
		Insulating interlayer			
adhesive bonding	low, RT–300	no	not certain	10–25	very particle insensitive, very versatile
glass-frit bonding	med./high, >400	yes	good		particle insensitive, versatile

*room temperature

Figure 18 : Overall assessment of all wafer bonding techniques

We have sorted in the above table, different wafer bonding techniques according to their operation mode and resulting characteristics. It is shown that for RF MEMS using HR Si substrate anodic bonding, wafer fusion bonding and glass frit bonding are the one that offer the most promising results. They are also based on existing know-how in high volume market of MEMS sensors (accelerometers, gyros,…) where reliability and cost are but at a very high level. The technologies using metallic interlayer (eutectic bonding, thermo-compression or solder bonding) are attractive but suffer of some potential reliability problems. These problems could be generated by intermetallic creation, surface wettability or pollution issues due to flux or other processing effects. The above packaging technologies applied to RF MEMS case are illustrated in the figure below. It shows that RF interconnects and bias management of the RF MEMS can be either implemented by through wafer interconnects and/or buried feed-through assuming that sealing of the cavity would not alter the switche reliability.

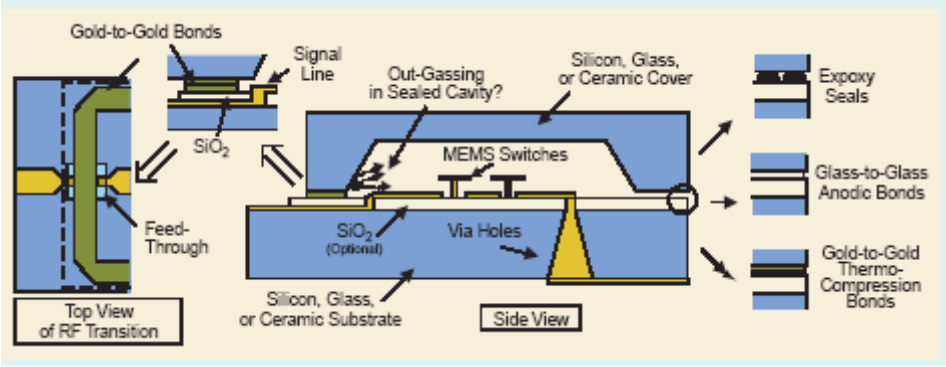

Figure 19 : illustration of possible packaging and RF feedthrough technologies applicable to RF MEMS

The problem with electrical feedthrough is that standard MEMS components require dc-50 kHz signals that can easily pass underneath the glass layer (anodic bonding) or use thin nitride or oxide layer to isolate the input/output lines from the gold-seal ring (thermo-compression bonding). These designs can be pushed to 6 GHz using narrow lines around the seal ring and a short input matching network. However, for 6-100 GHz operation, it is

best to use RF transitions based on via holes (wideband designs) or on electromagnetic coupling through the wafer (20-30% bandwidth). Alpha Inc. developed a via-hole transition covering dc-40 GHz and having an insertion loss of -0.1 dB at 20 GHz. RF transitions are, therefore, not the major problem in RF MEMS packaging. There is currently a large effort to develop wafer-scale packaging techniques that are compatible with MEMS switches (low-temperature hermetic glass bonding, minimal outgassing, gold-to-gold bonding with localized heating, etc.). Perhaps the only mistake in this field is that most RF MEMS switches available today were developed independent of the package. This necessitates the development of packaging techniques that must be compatible with an already mature RF MEMS switch technology at the wafer level. To take that as goal for future industrialisation or technology selection, to further develop and/or use RF MEMS switches that are considered as a single unit together with the package. This will allow perfect compatibility and limited reliability impact among the two areas.

2.2.3.1.2 Wafer level sealing approach (using surface micromachining)

Surface-micromachining leads to very compact and thin micro shells requiring just a bit more space than the actual devices to be package. The traditional sealing by dielectric shell procedure by LPCVD process is illustrated in the figure below. This approach was validated but has the disadvantage of high temperature process (>500 °C) that could be incompatible with some RF MEMS devices. Recently, a lower temperature approach (250 °C) have been demonstrated using metal. The shell is formed by Ni electroplating onto a photoresist layer, which is then removed by KOH etchant. Sealing is done by solder reflow in vacuum using solder bumps printed on the shell.

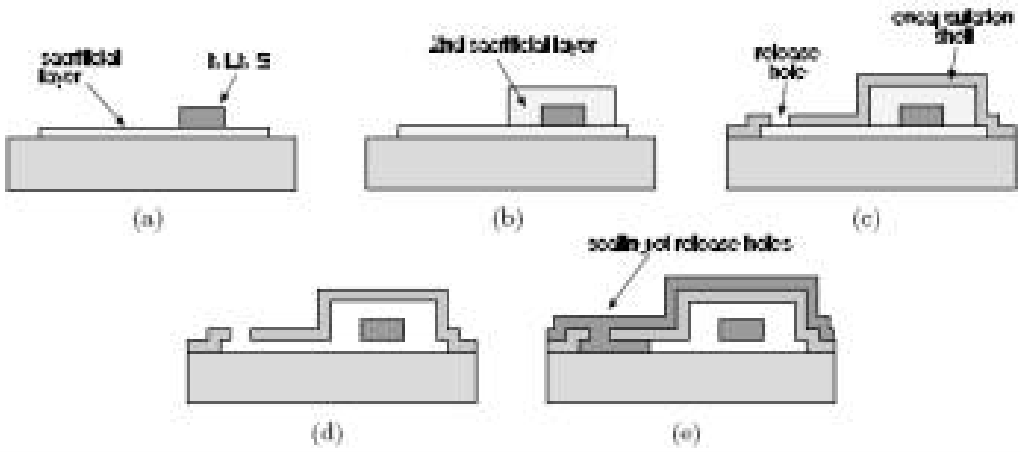

Figure 20 : illustration of wafer level sealing

This method is very attractive because it allows an improved packaging partitioning, limiting the interconnect constraints that are induced by the packaging constraints (sealing rings,…). Contamination should be also reduced because the sealing of the RF MEMS device is done as part of the MEMS process

2.2.3.2 Anodic Bonding

Anodic bonding process (or field assisted glass-silicon sealing) is used to hermetically join glass and silicon without the use of adhesives. The bonding is achieved by placing the

wafers together (a surface roughness of less than 0.1 μm is needed to allow the surfaces to mate closely) and heating them to a proper temperature (well below softening of glass, typically 300-500 °C) when the alkali-metal ions in the glass become mobile. A high dc voltage of the order of a few hundred volts is applied across the glass and silicon wafers (silicon positive respect to glass) and the alcali cations migrate from the interface resulting in a depletion layer with high electric field strength. The electrostatic attraction get the silicon and glass in very close contact. An anodic reaction occurs in the interface when the current flow of oxygen anions from the glass to silicon takes place. This reaction accomplishes the anodic bonding joining the glass and silicon wafers permanently together with a chemical bond. [1,2]

The benefits of anodic bonding include the following [1]:

- *Relatively low bonding temperature gives more design flexibility*
- *Bond is stress free and thermally matched; mechanical dimensions stable*
- *Flat assembly*
- *No measurable flow of the glass occurs, hence enabling sealing around previously machined grooves, cavities etc. without any loss of dimensional tolerances*
- *Since glass is an electrical insulator, parasitic capacitances are kept small*
- *Hermetic seals. The sealing process can readily be performed in vacuum, allowing hermetically sealed reference cavities to be formed (or the sealing in of special gas mixtures)*
- *Glass transparency at optical wavelengths enables simple, but highly accurate, alignment of pre-patterned glass and silicon wafers. This transparency can also be exploited via optical addressing, and to 'see' inside micro-fluidic devices*
- *High yield process. Tolerant to particle contamination and wafer warp (the electrostatic field generates a high clamping force which overcomes these surface irregularities)*
- *Low cost wafer scale process for first order packaging can be done at chip level if required*
- *Multi-layer stacks allow an easy route to complex 3-D microstructures*
- *High strength bond - higher than the fracture strength of glass*

Applications of anodic bonding

Anodic bonding has been used in applications of MST, MEMS or microengineering, more specifically in fabrication of pressure sensors, accelerometers, micropumps and other fluid handling devices. Anodic bonding can be used as a first order packaging of silicon microstuctures to isolate package induced stresses. The sensitive microstructure bonded to a relatively thick (~1mm) glass base can be mounted on PCB's or other substrates having a thermal expansion mismatch with silicon. Thus, the high stress regions occurs in the glass instead of in the microstructure. Sealed cavities can be used for MEMS devices, e.g., capacitive and optically addressable pressure sensors. AML has a process for hermetically sealed leadthrough between internal electrodes and external bond pads.

SUPPLIERS OF ANODIC BONDING

Applied Microengineering Ltd (AML), http://www.aml.co.uk

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2.3 POSSIBLE ANTENNA APPLICATION

2.3.1 Active Integrated Antennas

The active integrated antenna concept allows construction of very compact transmit and receive elements, [1,2]. Transmit elements can be highly stable, [3], easily modulated, [4], but have got high out of band radiation, [5,6], primarily because its hard to fit filters into an integrated antenna. Linearity is also a problem, [7]. Due to the difficulty of integrating filters duplex, simultaneous transmit receive action is also hard to achieve.

In the light of these difficulties it is possible that the opportunities offered by packaging technologies can help. In particular, multi-chip modules, multi-layer construction, LTCC and micromachining, may allow better screening and the introduction of filters, whilst still resulting in low cost

2.3.1.1 Multi-Chip Modules

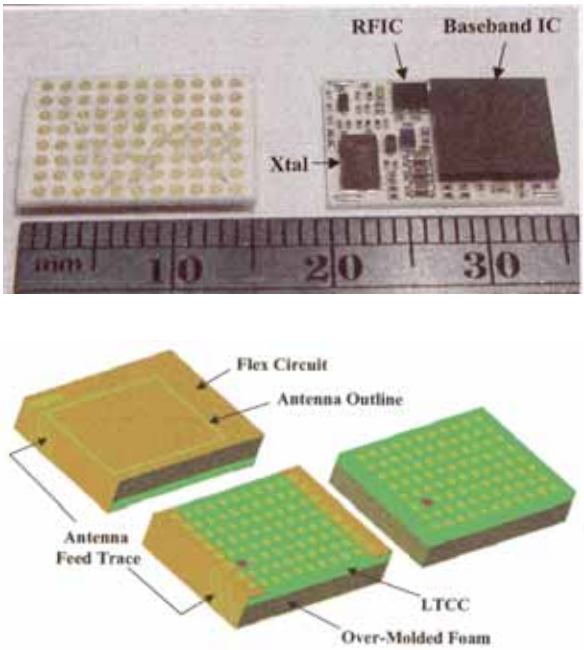

Figure 2.3-1: Multi-chip module for Bluetooth applications
(Courtesy of E-tenna Corp)

Multi-chip modules (MCM) is a technique that is now widely adopted. Some of the large surface mount packages inside PCs are not single chips, but multiple chips wired together in an MCM package. Figure 2.3-1 shows an MCM package for a Bluetooth application. The module is constructed on a carrier, which is a multilayer low temperature cofired ceramic, LTCC, assembly. Multiple chips, such as the RF MMIC, crystal and baseband chip, are mounted on this carrier. The bottom of the package has a lot of solder bumps to allow solder mounting onto a printed circuit board. The flex film slot antenna is soldered on bumps at the edge and wrapped around the whole module. It thus forms a complete communications package, including antenna.

2.3.1.2 Multi-Layer Modules

A more compact or coherent package can be obtained using multi-layered concepts throughout the whole assembly. Table 2.3-1, [8], shows the performance of different materials used for multi-layered packages, teflon (low, dielectric constant, plastic based), polyimide (used for thin layers on printed circuit boards) and ceramic. By and large, ceramic performs well in most of those, apart from the fact the antenna will be narrow band.

Figure 2.3-2 shows a ceramic polyimide combination. In the ceramic layers, patch antennas, vias, filters and ground planes, can be made. So good shielding between the parts of the

transceiver can be achieved, and filters will be relatively small. The polyimide provides connection to the MMIC and DC supplies. The connection to the MMIC is one of the most crucial issues in the whole assembly.

If wide band antennas or antennas covering big areas, such as arrays, are needed, then a Teflon, ceramic, polyimide combination may be used, as shown in Figure 2.3-2. An area of difficulty is the gluing of Teflon to ceramic and its integrity over large temperature changes.

	Teflon	Polyimide	Ceramic
Antenna Size	Large	Large	Small
RF Performance	Good	Good	Excellent
Thermal Radiation	Fair	Fair	Excellent
Easy Fabrication / Antenna	Good	Fair	Good
Easy Fabrication / Filter	Good	Fair	Good
Easy Fabrication / RF Circuit	Fair	Excellent	Good
Easy Fabrication / Connection	Fair	Good	Good

Table 2.3-1: Comparison of the Performance of Materials used in Multi-Layer Packaging, [8]

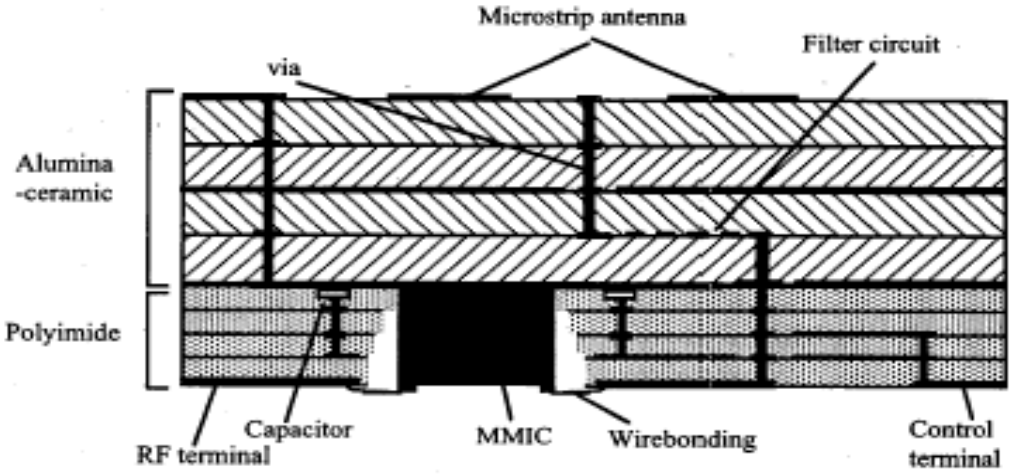

Figure 2.3-2: Typical Ceramic, Polyimide Multi-Layer Package, [8]

It is concluded that this approach will allow very good performance of integrated antennas, but is neither cheap (yet), or simple. However it should also realised that this sort of technology, particularly multi layer ceramic and polyimide, are being used already, particularly in very fast PC processor chips. Table 2.3-2 gives the relative permittivity, ε_r , of various packaging materials. It is important to know how big the antenna going to be on each of these materials. For example, an air-spaced, 900MHz GSM antenna, will occupy 8.3cm^2, which is probably too big to make on a chip.

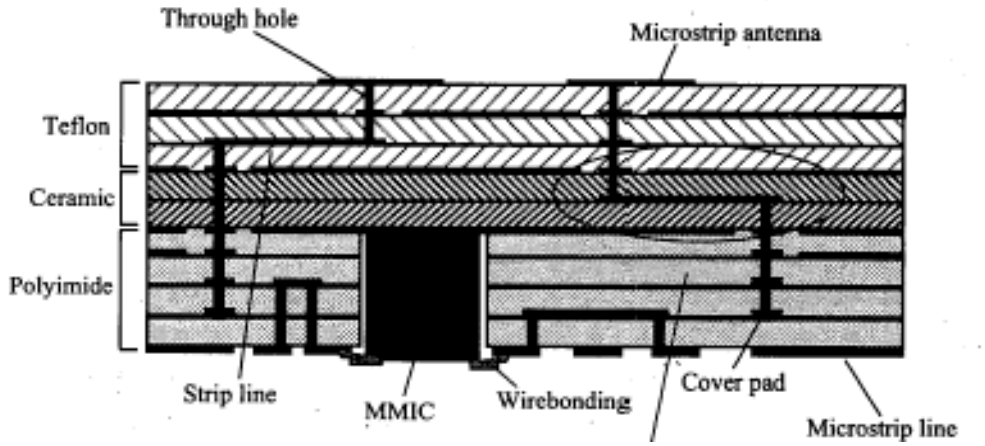

Figure 2.3-3: Typical Teflon, Ceramic, Polyimide Multi-Layer Package, [8]

	ε_r		ε_r
Teflon	2.1	Low temp cofired ceramic	4.8
Kapton	3.6	Low K thick film dielectric	5.2
Valox	3.7	Beryllia ceramic	6.5-6.9
FR-4 Epoxy glass	4.8	Alumina ceramic	8.8-10.1

Table 2.3-2: Relative Permittivity, ε_r , of Various Packaging Materials, [9]

For alumina the area will be about 2.8cm^2, which might allow one of these packages. However, the antenna will be narrow band. If this is acceptable then there are a variety of configurations that could be used. Figure 2.3-4shows one, in which the patch antenna is made as part of the lead frame, [10].

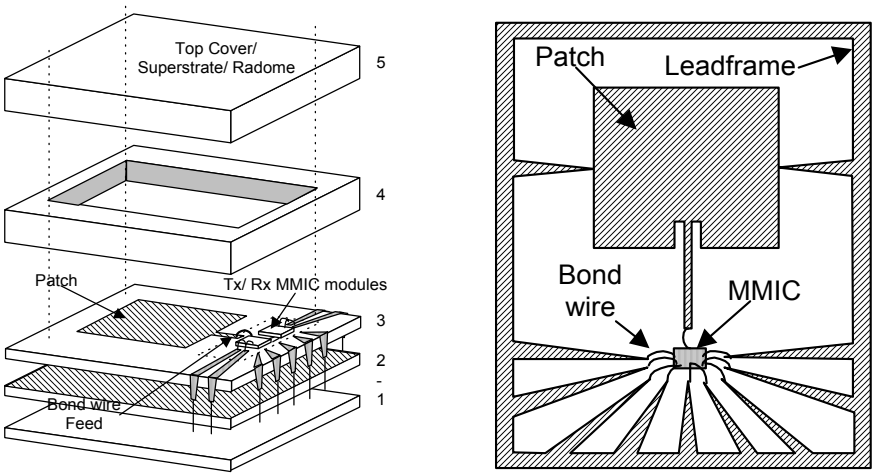

Figure 2.3-4: Chip Carrier Integrated Antenna Package, [10]
(Lead frame shown on right)

Other concepts are shown in Figure 2.3-5, using multi layering in ceramic to allow the incorporation of filters.

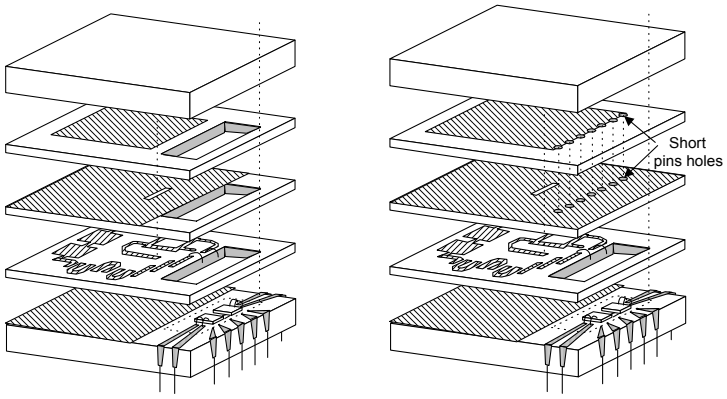

Figure 2.3-5: Alternative Chip Carrier Integrated Antenna Package Configurations, [10]

Another possibility is to use some device on the MMIC to excite a metal lid on the top of the package. Such metal lids on top of packages are used for grounding and protection. But in this architecture it becomes the antenna. This concept he been demonstrated at 5.8GHz, with a GaAs MMIC shorted H shaped patch 4x2mm in size, [11]. This is about is about 20th of a wavelength and consequently the gain was -10dBi. With a parasitic placed a couple of millimetres above it, the gain was about 3dBi.

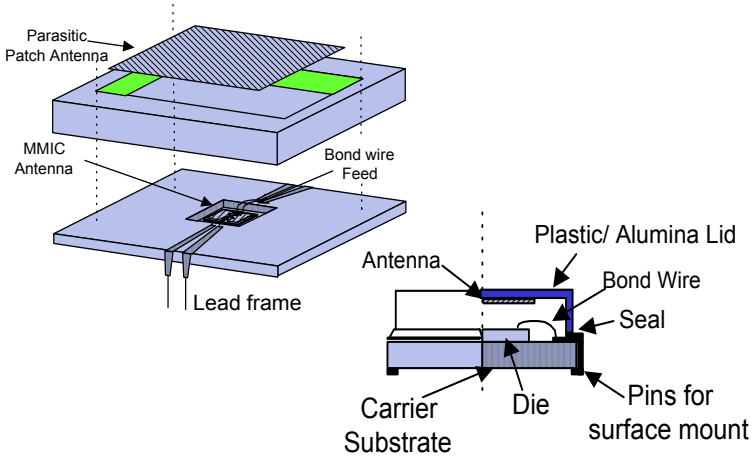

Figure 2.3-6: Chip Carrier Integrated Antenna with Parasitic on Top of Package, [10]

Figure 2.3-7 shows an alternative configuration, [12]. A MMIC with a millimetres antenna is placed in a multi layer ceramic assembly. The patch antenna couples into the layered patch array located above it.

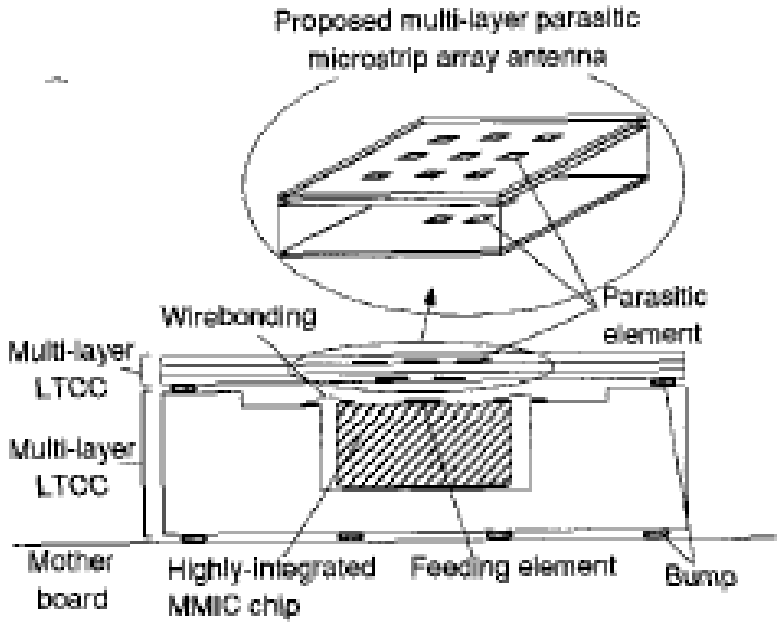

Figure 2.3-7: Array-MMIC Coupling Arrangement, [12]

2.3.1.3 LTCC

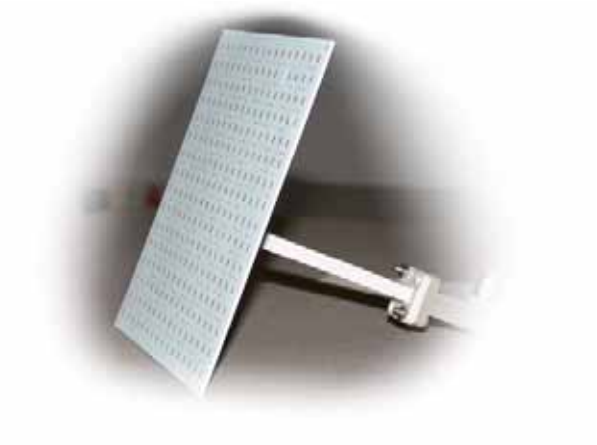

Figure 2.3-8: LTCC Array, [13]

Good antennas can be made from LTCC, and one example is shown in Fig 8, [13]. Here the conventional microstrip lines in the feed network are replaced by waveguides, formed in the LTCC multi-layer. The losses are reduced by more than half.

Small antenna and front-end modules are also being demonstrated using this technology.

2.3.1.4 Micromached Packaging

Antennas can also be integrated using electromagnetic bandgap materials. Figure 2.3-9, [14], shows a wood pile material that is being investigated as a medium into which sub-millimetric antennas and circuits can be implemented. The work has been initiated by the

European Space Agency who are interested in frequencies above 300GHz for earth resource observation from space using radiometers.

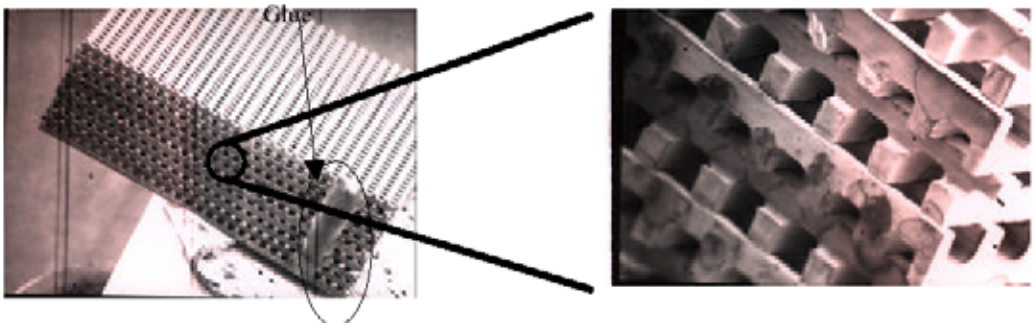

Figure 2.3-9: Wood Pile Electromagnetic Bandgap Material for Sub Millimetric Wave Integrated Antennas, [14]

2.3.1.5 MMIC Integration

Fig 10 shows a patch antenna with FET oscillators on GaAs MMIC for operation at 30GHz, [4]. This will cost between 500 and 1000 UKP for a university to have this made using the Europractice foundry service. Also, much of the chip is occupied by a passive device.

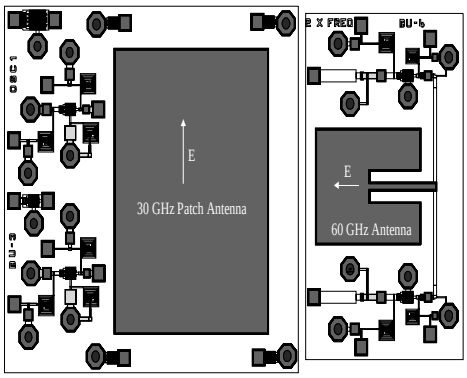

Figure 2.3-10: Patch Antenna with FET Oscillators on GaAs MMIC for Operation at 30GHz, [4]

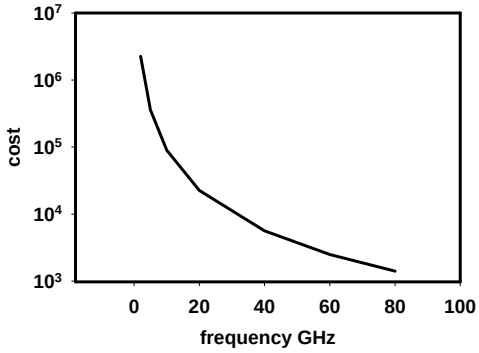

Figure 2.3-11: Cost of Integrated Antennas on MMICS.

(note – no units on cost axis; graph is for illustrative purposes only)

Figure 2.3-11 shows in diagrammatic form the relationship between the cost of an integrated antenna on a MMIC chip and frequency. At low frequency the antennas are big so cost is high. At high frequencies cost reduces. It is concluded that it is uneconomic to put the antenna on the chip except at higher frequencies, unless very low area antennas are used.

Figure 2.3-12 shows an example where a low area antenna, a loop, is used on a silicon-germanium MMIC, [15]. Underneath the slot a trench has been cut out to improve the efficiency. It is clear that this antenna uses a much smaller area than for example the patch antenna shown in Fig 10. So it is concluded that it is important to find an efficient antenna that minimises the occupied space on the chip.

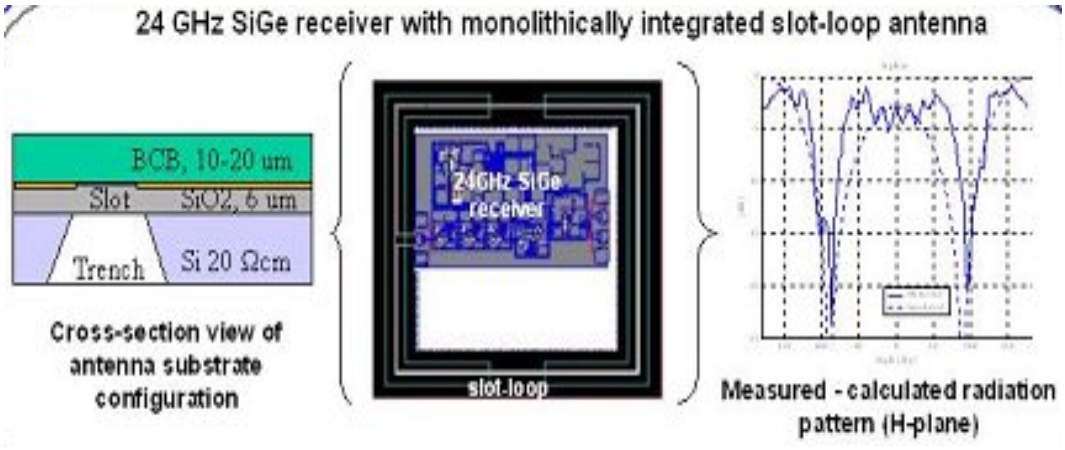

Figure 2.3-12: Micromachined Loop Slot Antenna on SiGe MMIC, [15]

Figure 2.3-13 shows an integrated antenna at 76GHz for a Doppler radar module, [16]. The antenna is a split patch which appears to be fed in a balanced way. At this frequency the antenna is relatively small compared to the circuit elements and for this simple application, where direct down conversion, or rather the extraction of the baseband Doppler signal, is easily done, this type of integrated approach looks promising.

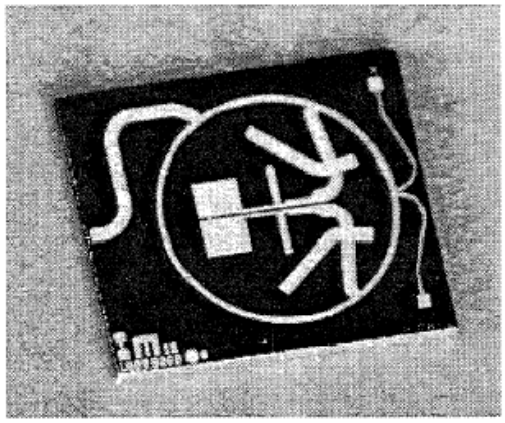

Figure 2.3-13: Integrated 76GHz Doppler Module, [16]

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2.3.2 Other Cases

A cooperation project of the two groups of Prof. Brand at the University of Erlangen and of Prof. Hartnagel at the Technical University Darmstadt, funded by the German Science foundation DFG used one dipole matrix for the fundamental frequency for a particular wave orientation and a second matrix shortly behind this, where its dipoles are for a harmonic frequency with an orientation of 90 degrees with respect to the first matrix dipoles. The two types of dipoles are then each connected up by GaAs Schottky diodes. Illumination by the fundamental wave was done by a horn antenna together with a polarizer, and a similar antenna was used to detect the harmonic signal. Since this arrangement was basically not a guided-wave system, the overall efficiency was very low, but sufficiently large for easy measurements. The matrix was a monolithic realization on a GaAs wafer with typically 4 x 4 elements.

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CHAPTER 3

MATERIAL MACHINING

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3. BENCHMARKING MANUFACTURING FACILITIES: MATERIAL MACHINING

3.1 INTRODUCTION

Historically, radio-frequency (RF) systems began with wires, valves and wire antennas. Such systems were physically extremely large and cumbersome. Fortunately, the trend has been towards increasing miniaturisation of devices and systems. A key part in this trend has been the improvements in manufacturing methods at smaller and smaller scales. Another aspect has been the growth of the number of materials available with different properties, allowing a wide variety of approaches to the miniaturisation problem. The following pages will describe some of the materials and technologies currently available for manufacturing, as well as examining potential applications to antennas.

3.2 TECHNOLOGICAL ASPECTS

3.2.1 Cast Ceramics

3.2.1.1 Overview

Ceramics are defined as man-made solid objects formed by non-metallic and inorganic raw materials that are baked at high temperatures. The traditional porcelain is composed of three naturally occurring minerals: pure white clay, silica, and feldspar [1].

Electronic ceramics is the fastest growing field in ceramics today. Ceramics have a wide range of electrical properties including insulating, semi-conducting, superconducting, piezoelectric and magnetic. Therefore, many kinds of capacitors, insulators, substrates, integrated circuit packages, piezo-electrics, magnets and superconductors are made from ceramics. Ceramics are critical to products such as cell phones, computers, television, and other consumer electronic products [2].

The following four types of ceramic are important electronic materials, and have wide usage.

3.2.1.2 Powder Pressed Ceramics

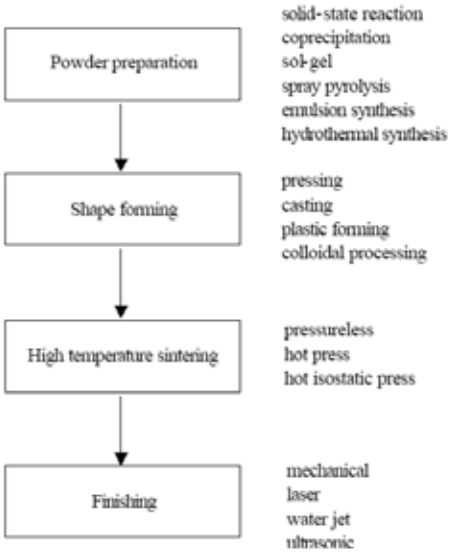


Figure 3.2.1: Powder processing route [3].

Traditionally, a powder compact is made by dry powder pressing, which is accomplished by placing the powder into a die and applying pressure to achieve compaction [3].

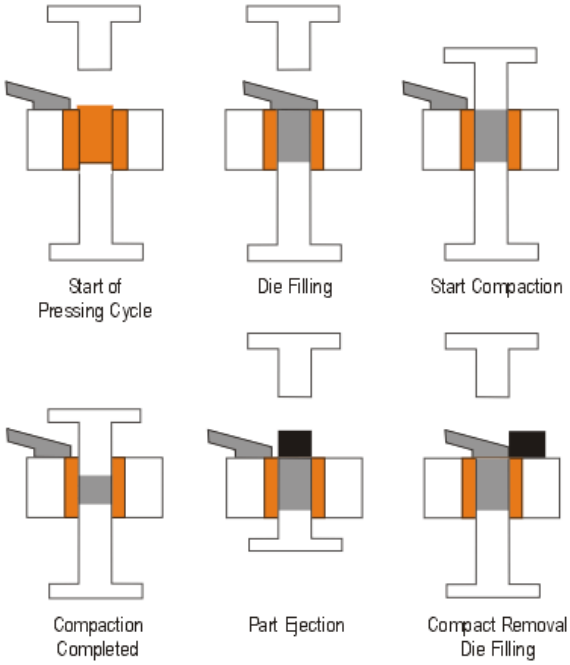


Figure 3.2.2: A typical uniaxial compaction cycle [4].

Powder pressed ceramic materials with high relative permittivity, high Q and good temperature stability are useful as dielectric resonators for microwave applications. They are an attractive, low cost alternative to metallic resonant cavities where they have the advantage of size reduction without reduction in performance [5].

Dielectric resonator materials have ε_r, values in the range 10-100. The discontinuity of the relative permittivity at the resonator surface allows a standing electromagnetic wave to be supported in its interior. A small radiating field from the resonator is usefully employed as a means of coupling, for instance, to a microstrip line on a circuit board or probes within a cavity [5].

The parameters of several typical powder pressed ceramics are listed in the appendix.

3.2.1.3 Castable Ceramics

Castable ceramics, ceramic refractories in which raw materials and hydraulic –setting cement (or chemical binder) are mixed. They are mixed with water, formed by casting and used to line furnaces, kilns, etc. Castable Ceramics will achieve optimum strength after heat-treating.

3.2.1.3.1 Technical Advantages **[6]**

- Feasibility for micro-fabrication with sub-micron dimensional tolerance
- Simple, one-step processing even for complex 3D geometries that would require multiple-step processing with other technologies/materials.
- Significantly lower processing costs and production times for complex geometries.
- Scalability to large volume production with very high component production rates.
- Excellent thermal cycling, thermal shock properties
- Continuous use temperature stability up to 1000^{o}C in air
- Component surface areas can be tailored to be over 100 m^2/g
- High surface are allows catalyst deposition with no wash coat.
- Flexural strengths as high as 80 MPa.

3.2.1.3.2 Applications [6]

- Alternative to silicon for high-T MEMS devices and micro-reactors;
- Micromachined sensors, substrates for optical switches, fibre-optic connectors, custom micro-reactors.

A lot of research has been done after this kind of material was manufactured. It shows castable ceramics have different electric parameters at different frequency and temperature.

TABLE I
MEASURED MATERIALS AND MANUFACTURERS

Material		Manufacturer
1.	Epoxy-LMB 1386, HY 951	CIBA-GEIGY
2.	Teflon-Vergussmasse, CHS-Type 1542	Carl Huth & Söhne
2a.	(2) plus 1/8 volume Eccospheres FTF-15	Emerson & Cuming, Inc.
2b.	(2) plus 1/4 volume Eccospheres FTF-15	Emerson & Cuming, Inc.
3.	Scotchcast 830	3M Co.
4.	Epoxy-LMB 1386, LMB 1387, DY 067 (mixed by weight)	CIBA-GEIGY
4a.	(4) plus 1/8 volume Eccospheres FTF-15	
4b.	(4) plus 1/4 volume Eccospheres FTF-15	
5.	Epoxy-LMB 1386, LMB 1387, DY 067 (mixed by volume)	CIBA-GEIGY
6.	Epoxy-Araldit CY 220, HY 951	CIBA-GEIGY
7.	Epoxy-Araldit F, HY 951	CIBA-GEIGY
8.	Eccofoam SIL	Emerson & Cuming, Inc.
9.	Epoxy-Araldit CY 209, HY 951	CIBA-GEIGY
10.	Epoxy-Araldit D, HY 956	CIBA-GEIGY
10a.	Epoxy Araldit D, HY 956 plus 17 % Eccospheres	CIBA-GEIGY
10b.	Epoxy-Araldit D, HY 956 plus 20 % Quartzmeal	
10c.	Epoxy-Araldit D, HY 956 plus 44 % Quartzmeal	
11.	Paraffin 52^{0} - 54^{0}	Merck
12.	Solid Teflon	Dupont

TABLE II
MEASURED AND PUBLISHED DIELECTRIC CONSTANTS AND LOSS TANGENTS

Material	300 °K		77 °K		Published (300 °K)	
	ε'	tan δ	ε'	tan δ	ε'	tan δ
1	4.33	n.m.				
2	3.00	0.019	2.92	0.0048		0.0021/1 kHz
2a	2.77	0.021				
2b	2.61	0.019				
3 •	3.03	0.021	2.92	0.0051	3.8 / 50 Hz	0.008
4	4.38	0.011				
4a	2.96	0.008				
4b	2.67	n.m.				
5	4.55	0.011	4.45	0.006		
6	2.97	0.025	2.89	0.0042	4.3 / 50 Hz	0.003
7	3.08	0.034	2.90	0.0043	4.1 / 50 Hz	0.003
8	2.91	0.026	2.87	0.010	1.4 / 10 GHz	< 0.01
9	2.96	0.023	2.87	0.0041	4.3 / 50 Hz	0.007
10	2.99	0.024	2.90	0.0039	4.1 / 50 Hz	0.016
10a	2.06	0.012	2.04	0.0028		
10b	3.05	0.017	2.98	0.0035		
10c	4.38	0.013			4.5 / 50 Hz	0.038
11	2.27	0.0003			2.3 / 25 GHz	0.0003
12	1.96	0.0005	1.96	< 0.0003	2.08/25 GHz	0.0006

Figure 3.2.3: Tables from [7].

Figure 3.2.3 shows the difference of dielectric constant and loss tangent at 22GHz and at 77°K comparing with at low frequency and room temperature.

3.2.1.4 Viscous plastic processing (VPP)

Viscous plastic processing (VPP) is a technique that has been developed to produce ceramics with improved properties by eliminating microstructure defects. A major cause of these flaws is the agglomeration, which occurs spontaneously in fine powders such as those used to produce ceramics. By carefully controlling the mixing conditions, VPP breaks down these agglomerates [4].

The doughs produced can be processed using a range of polymer forming techniques, which extend the options for both simple and complex shapes. These techniques have been applied to an extensive range of materials, including advanced refractory ceramics and tile bodies [4].

In VPP, ceramic powders are mixed into a viscous polymer solution under very high shear conditions, such as using a two-roll milling technique. The process is appropriate for most ceramic powders [4].

3.2.1.4.1 Advantages of the VPP Route [4]

Advantages of VPP over other more conventional processing routes include:

- Enhanced material consistency;
- Easier green handling;
- Increased strength;
- Improved creep resistance;
- Increased fracture toughness;
- Superior surface finish;
- Rapid processing;
- Environmentally friendly systems.

Viscous plastic processing can result in products of much greater flexural strength than is achieved by powder pressing (Figure 3.2.4).

Material	Powder Pressed (MPa)	VPP & Extrusion (MPa)
Titania	190	760
Alumina	290	980
Silicon Carbide	425	1087
Mullite/Alumina (kiln furniture)	7.1	18.4
Zirconia HSY-3	690	995
Tile Body	35	44

Figure 3.2.4: Strength comparison of pressed and VPP manufactured components [4].

The VPP procedure is shown in Figure 3.2.5.

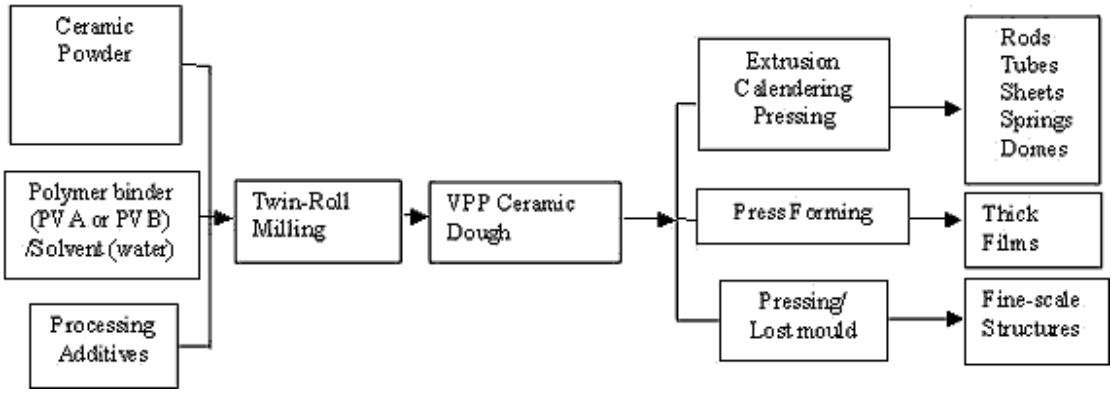


Figure 3.2.5: VPP Procedure from [8].

The fabrication routes involve producing a homogeneous and formable ceramic dough using a Viscous Polymer Processing technique, with various subsequent shape-forming operations to produce devices with sizes ranging from tens of millimetres to tens of microns [8].

- High shear mixing
- Ceramic powder, polymer binder and solvent
- Simple, usually 3-part, system
- De-agglomerated mix created
- High solids loading:
  - 50-60 vol.%
- Plastically formable green state

$$\dot{\gamma} = \frac{R}{g}(\omega_1 - \omega_2)$$

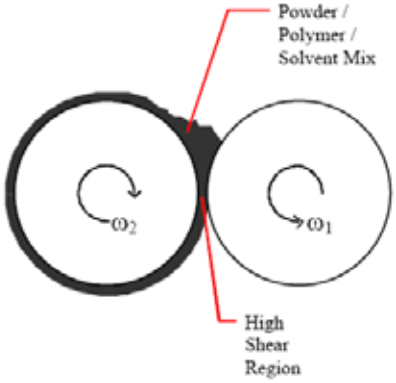


Figure 3.2.6: Twin-Roll Milling from [9].

3.2.1.5 Piezo-electric Ceramics

Piezoelectricity is a phenomenon that occurs in a certain class of anisotropic crystals subjected to mechanical deformation. When a mechanical pressure is applied to such materials, the crystalline structure produces a charge proportional to the strain. Conversely, when an electric field is applied, the crystalline structure changes shape, producing dimensional changes in the material [3].

Piezoelectricity is a property of certain classes of crystalline materials including natural crystals of Quartz, Rochelle Salt and Tourmaline plus manufactured ceramics such as Barium Titanate and Lead Zirconate Titanates (PZT) [5].

The piezoelectric effect for a given item depends on the type of piezoelectric material and the mechanical and electrical axes of operation can be precisely orientated within the shape of the ceramic. These axes are set during "poling", the process that induces piezoelectric properties in the ceramic. The orientation of the dc poling field determines the orientation of the mechanical and electrical axes [5].

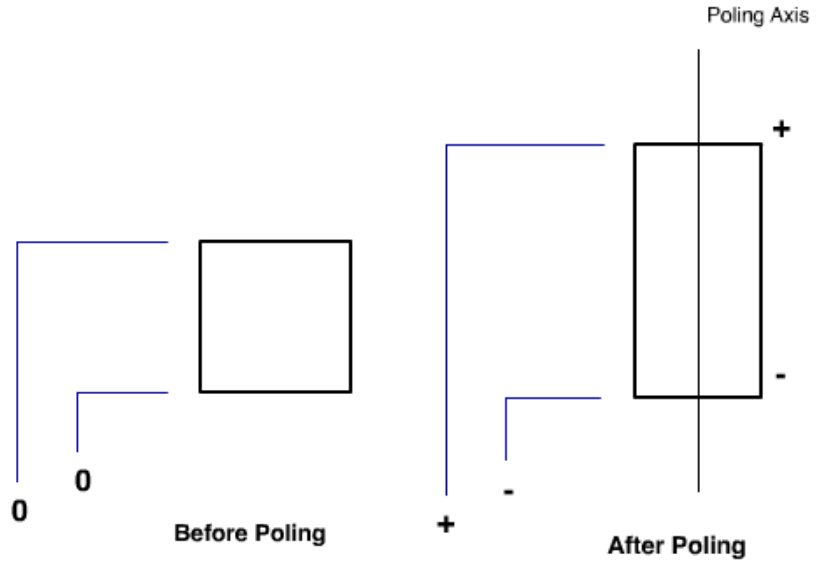


Figure 3.2.7: Piezoelectric Actions from [5].

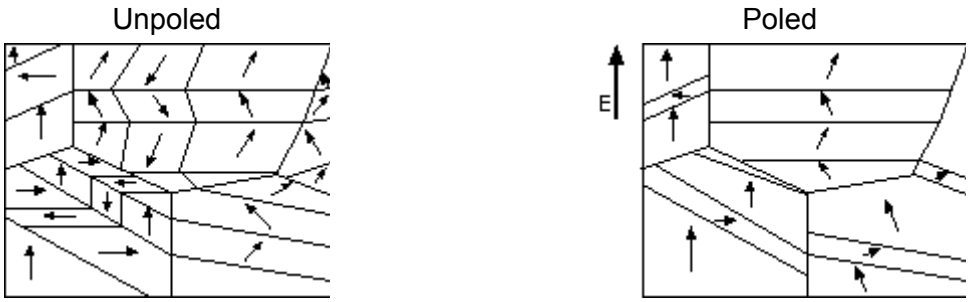


Figure 3.2.8: Poling from [5].

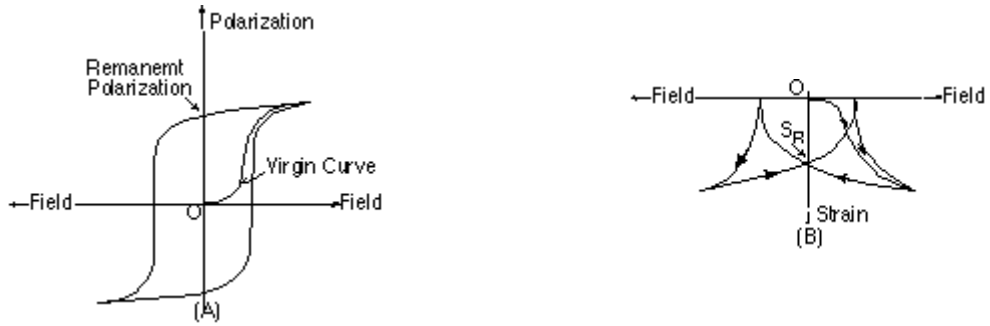


Figure 3.2.9: Hysteresis from [5].

When the crystalline structure of a material has no centre of symmetry, it is non-centro-symmetric. A single crystal with this structure has anisotropic characteristics: the properties of the material differ according to the direction of measurement. Piezoelectricity is an anisotropic characteristic. The non-centro-symmetric crystalline structure provides a net electric dipole moment within the crystal unit cell. Any dipoles aligned in the same direction will arrange themselves into regions called domains.

Piezoelectric ceramics are ferroelectric materials. These materials have non-centro-symmetric unit cells below a certain temperature and a centro-symmetric structure above that temperature. That temperature is the Curie temperature. Above the Curie temperature, these ceramics have a centro-symmetric structure and have no piezoelectric characteristics. Below the Curie temperature, these ceramics have a non-centro-symmetric structure [5].

3.2.1.5.1 Typical Arrangements

3.2.1.5.1.1 Unimorph®

The magnitude of piezoelectric forces, actions and voltages is relatively small. The maximum extension of a single element is in the order of fractions of a micron. Amplification is often required and can be achieved by various arrangements of the piezo ceramic such as Unimorph, Bimorph and Stacks.

A Unimorph is made by bonding a thin piece of piezo-ceramic to an inactive substrate. Driving the piezo-ceramic will lead to deformation of the entire structure. Transducer Products Division has expertise in making various high specification Unimorphs for Hydrophones, Sensors and Actuators.

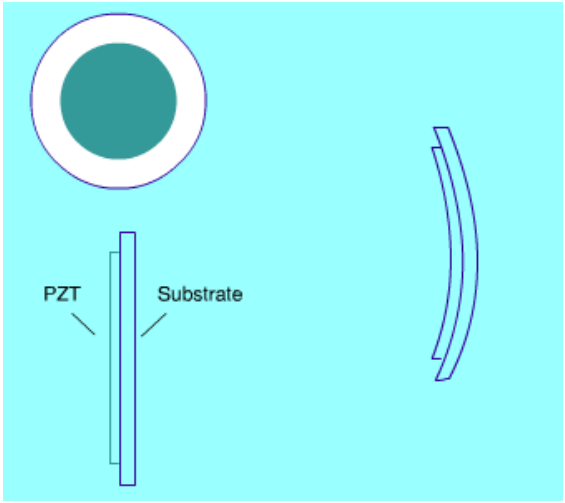


Figure 3.2.10: from [5].

3.2.1.5.1.2 Bimorphs®

A Bimorph is made by bonding two pieces of piezo-ceramic together so that differential changes in length of the two pieces can produce relatively large movements. This element consists of two transverse expander plates secured together face to face in such a manner that a voltage applied to the electrodes causes the plates to deform in opposite directions, resulting in a bending action. The displacement of the Bimorph in response to an applied voltage is many times greater than the corresponding displacement of a single plate, typically in excess of 10µm per volt. Thus Bimorphs have, in effect, 'built-in' levers to provide or require much greater motion but less force than single plates.

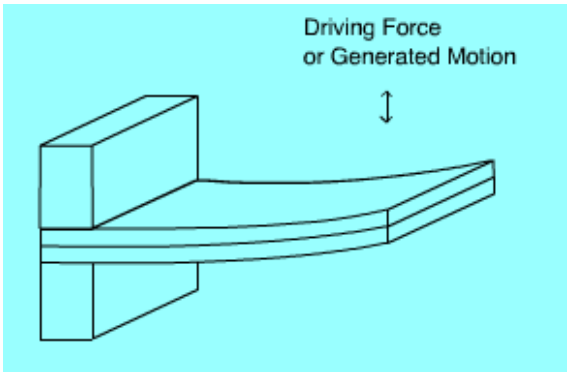


Figure 3.2.11: from [5].

3.2.1.5.1.3 Actuator Stacks

Stacks are several piezoelectric elements connected mechanically in series and electrically in parallel. The displacement of each transducer element adds to the total displacement. The displacement of the whole stack assembly is equal to the sum of the individual displacements. Stacks are generally required for applications requiring large displacements (typically between 5 and 180µm).

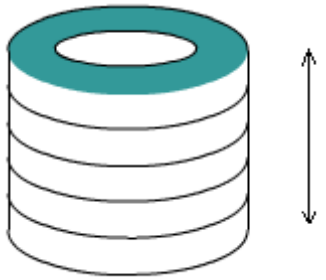


Figure 3.2.12: from [5].

3.2.1.5.1.4 Sandwich Transducers

It is difficult to make single blocks of ceramic resonating below about 100 KHz. Instead a composite half wave resonator is used consisting of two or more piezo-ceramic rings sandwiched between metal layers. This arrangement can achieve low frequencies at high drive levels.

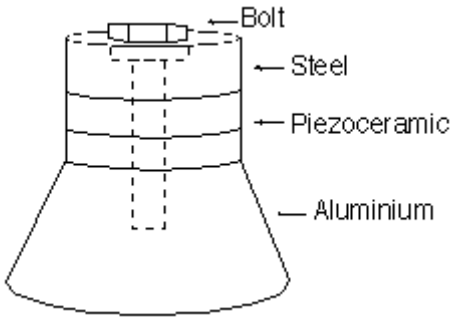


Figure 3.2.13: from [5].

3.2.1.5.2 Properties Definitions

The piezoelectric properties are described by a system of symbols and notations, identifying compliance, electromechanical coupling, etc. [5].

Property	Definition	MKS Units
Electro Mechanical Coupling Coefficient		
k	$\sqrt{\frac{\text{mechanical energy stored}}{\text{electrical energy applied}}}$ or...	-
	$\sqrt{\frac{\text{electrical energy stored}}{\text{mechanical energy applied}}}$	-
Piezoelectric Constants		
d	$\frac{\text{strain developed}}{\text{applied field}}$	m / V
	$\frac{\text{short circuit charge density}}{\text{applied stress}}$	C / N
g	$\frac{\text{open circuit field}}{\text{applied stress}}$	V / N
	$\frac{\text{strain developed}}{\text{applied charge density}}$	m^2 / C
Relative Dielectric Constant		
K	$\frac{\text{(permittivity of material)}}{\text{(permittivity of space)}}$	-
Modulus of Elasticity		
Y	$\frac{\text{stress}}{\text{strain}}$	Nm^{-2}
Density		
ρ	$\frac{\text{mass}}{\text{volume}}$	kg/m^3
Frequency Constant		
N	Controlling Dimension x Resonant Frequency	Hz m

Typical properties of several kinds of Piezo-ceramics are listed in the appendix [5].

3.2.1.5.3 Limitations

Each piezoelectric material has a particular operating limit for temperature, voltage, mechanical stress and power. The particular chemical composition of the material determines the limits. Operating a material outside of these limitations may cause partial or total depolarization of the material, and a diminishing or loss of piezoelectric properties [5].

3.2.1.5.3.1 Temperature

As the operating temperature increases, piezoelectric performance of a material decreases, until complete and permanent depolarization occurs at the material's Curie temperature.

The Curie point is the absolute maximum exposure temperature for any piezoelectric ceramic. Each ceramic has its own Curie point. When the ceramic element is heated above the Curie point, all piezoelectric properties are lost. In practice, the operating temperature must be substantially below the Curie point.

The material's temperature limitation decreases with greater continuous operation or exposure. At elevated temperatures, the ageing process accelerates, piezoelectric performance decreases and the maximum safe stress level is reduced [5].

3.2.1.5.3.2 Voltage

A piezoelectric ceramic can be depolarized by a strong electric field with polarity opposite to the original poling voltage.

The limit on the field strength is dependent on the type of material, the duration of the application, and the operating temperature. The typical operating limit is between 500V/mm and 1000V/mm for continuous application.

It should be noted that alternating fields can have the same effect during the half-cycle opposite to the poling direction [5].

3.2.1.5.3.3 Mechanical

High mechanical stress can depolarize a piezoelectric ceramic. The limit on the applied stress is dependent on the type of ceramic material, and duration of the applied stress. For dynamic stress (impact ignition) the limit is less severe; materials with higher energy output (high g constant) can be used.

For impact applications, the material behaves quasi-statically (non-linear) for pulse durations of a few milliseconds or more. When the pulse duration approaches a microsecond, the piezoelectric effect becomes linear, due to the short application time compared to the relaxation time of the domains [5].

3.2.1.5.3.4 Power

The acoustic power handling capacity of a radiating transducer is limited by the following factors:

1. Dynamic mechanical strength of the ceramic;
2. Reduction in efficiency due to dielectric losses;
3. Reduction in efficiency due to mechanical losses;
4. Depolarization of the ceramic due to electric field;
5. Depolarization of the ceramic due to temperature rise;
6. Instability resulting from the positive feedback between dielectric losses and internal heating (2 and 5) [5].

Power limitations of several kinds of Piezo-ceramics are listed in the appendix [5].

3.2.1.6 Ceramic Material Research and Processing Facilities in the University of Birmingham

3.2.1.6.1 Research [8]

The research areas under investigation include the synthesis, processing, fabrication and characterisation of functional and structural ceramic materials, components and devices. Three research groups work on a range of fundamental and industrial projects. They are the Functional Materials Group, Ceramics Forming Group and Ceramic Composite Group, comprising approximately 30 staff, research workers and students.

3.2.1.6.1.1 Research Topics of the Functional Materials Group

- Piezoelectric Materials and Devices;
- Ferroelectric Materials and Thick Films;
- Microwave Dielectric Materials and Characterisation Techniques;
- High Temperature Superconductors (HTS);
- Improved Processing of Ceramic Materials.

3.2.1.6.1.2 Research Topics of the Ceramics Forming Group

- Anisotropic Magnets by Paste Forming;
- Interactions of Formulation, Rheology and Extrudate properties;
- Advanced Trickle Bed Technology for the Fine Chemicals and Petroleum Industries;
- Extrusion of Ceramic Tubes with Controlled Bends;
- Signal Processing for On-line Control of Paste Extrusion.

3.2.1.6.2 Facilities [8]

The IRC is equipped with state-of-the-art facilities for synthesis, processing, fabrication and characterisation of ceramic powders, materials, components and devices. Some of the equipment is listed below.

3.2.1.6.2.1 Powder Synthesis and Characterisation

- Netzsch Dilatometer for 1600°C with atmosphere control;
- Netzsch Dilatometer for 2000°C for vacuum/inert atmosphere work;
- Edwards Freeze Drier;
- Ball Mills and High Energy Vibro-Mill for particle comminution;
- Laser Diffraction Particle Size Analysers – Coulter and Sympatec.

3.2.1.6.2.2 Processing, Fabrication and Sintering

- 2-Roll Mills;
- 3-Roll Mill;
- 50-ton Press;
- Screen Printer;
- Large range of ovens, muffle furnaces and tube furnaces with temperature capabilities to 1700°C;
- 2-roll Calender;
- Laminar Flow powder handling and processing areas 100kN and 200kN Instron testing machines (used for instrumented pressing and extrusion work).

3.2.1.6.2.3 Materials and Device Characterisation

- Electromagnetic Characterisation from 100MHz–20GHz via HP 4914A Impedance / Gain Phase Analyser HP 8720A Vector Network Analyser;
- Wide range of test cavities for microwave materials measurements at normal and cryogenic temperatures. High power microwave amplifiers available for 1-2GHz and 8-12GHz frequency ranges;
- Computer controlled electromagnetic measurements from -70 to +200°C;
- Piezoelectric sensor and actuator device characterisation with computer control;
- Surface roughness characterisation (Talysurf);
- High voltage electrical supplies and heated oil bath for poling of piezoelectric materials;
- Wide range of DC voltage and current supplies with micro- and nano-voltmeters for DC characterisation at normal and cryogenic temperatures;
- Optical Microscope with Digital Camera;
- 3-point and 4-point mechanical property measurements;
- Accutom 50 for precision cutting and surface grinding.

3.2.1.6.2.4 Others from Ceramics Forming Group

- Rosand Capillary Rheometer;
- Carrimed Controlled Stress Rheometer for flow, creep and oscillatory measurements of fluids and pastes at 20–90°C;
- Load Frames;
- Werner and Pfleiderer Mixers with counter-rotating masticator blades and heating, cooling and vacuum facilities;
- Micromeritics Instruments for porosity, surface area, pore size and chemisorption measurements;
- Small Furnaces for temperatures up to 1600°C;
- Battenfeld Wax Injection Moulder;
- Manumould Injection Moulder capable of moulding ceramic, metal and plastic components;
- Extrumix, a double lobe, sigma blade mixer with screw attachment, which improves mixing and discharges the paste by extrusion. 5-litre capacity;
- Attrition Mill with 1440 ml vessel;
- Haake Rheocord Twin and Single Screw Extruders with various feeders, heating and cooling facility, four pressure transducers along the barrel for the single screw (the units of the co-rotating twin screws can be re-assembled as needed);
- Olympus Microscope with camera;
- Controlled Environment Drying Oven, where various temperatures and humidities can be maintained over long periods;
- Two Reciprocating Mixers with a variety of mixer plates, heating and cooling.

3.2.2 Metal Micromachining

3.2.2.1 Overview

The following is an extract from a report by researchers at the University of Birmingham. It is intended to provide an example of the role that can be played by metal micromachining in antenna design.

3.2.2.2 Antennas and Beamformers

3.2.2.2.1 Dimensional Measurements of Machined Structures

The electroformed coupler specimen (nominal 50um layer version) was measured using the surface profiler and the thickness recorded was an average of 33um, as shown in Figure 3.2.14 and Figure 3.2.15 below. This result indicates that the thickness of the pieces is below the design target. However, the other dimensions of the specimen generally match the designed values.

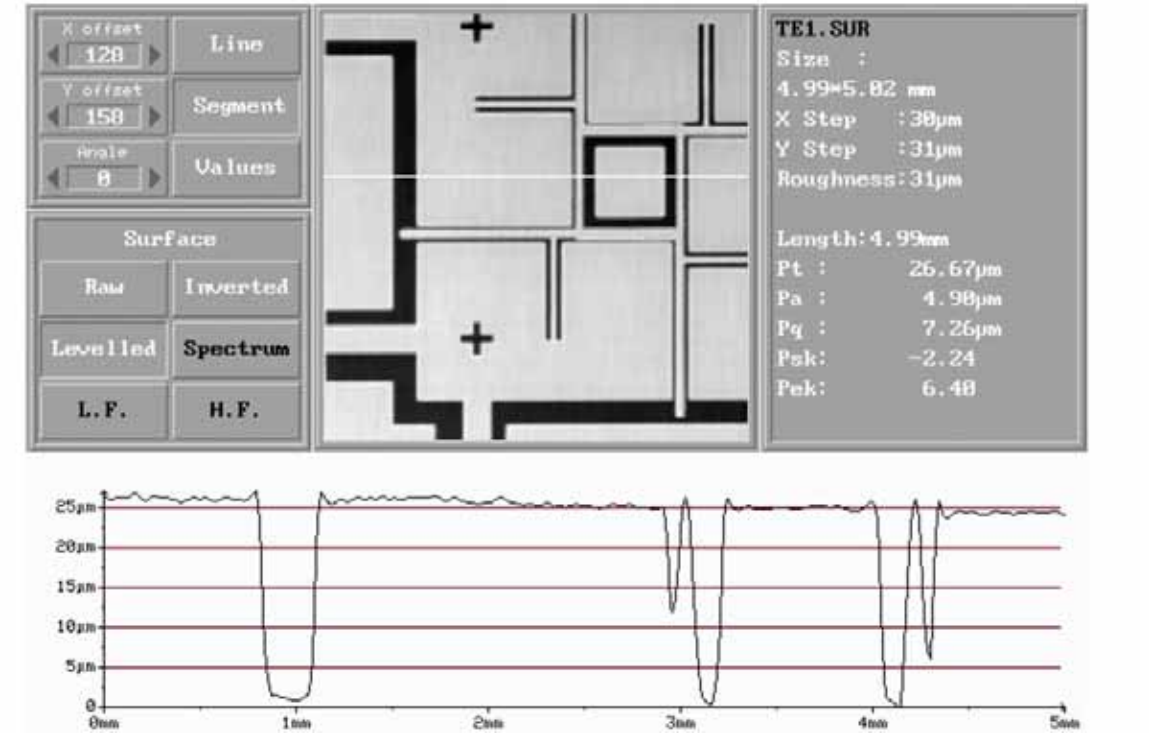


Figure 3.2.14: Horizontal Profile of the electroformed centre piece

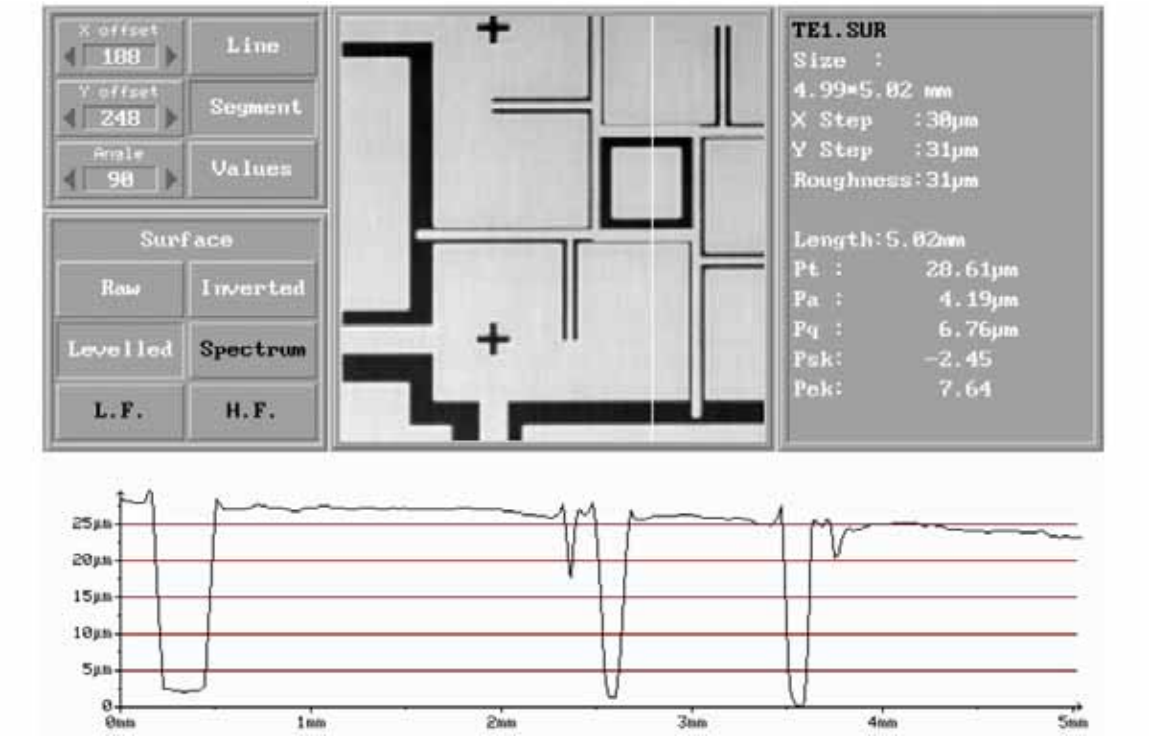


Figure 3.2.15: Vertical Profile of the electroformed centre piece

The thickness of the 100um, chemically etched coupler specimen was also measured by the same technique. The result showed a good agreement with the average thickness of 100um. This is shown in Figure 3.2.16 and Figure 3.2.17.

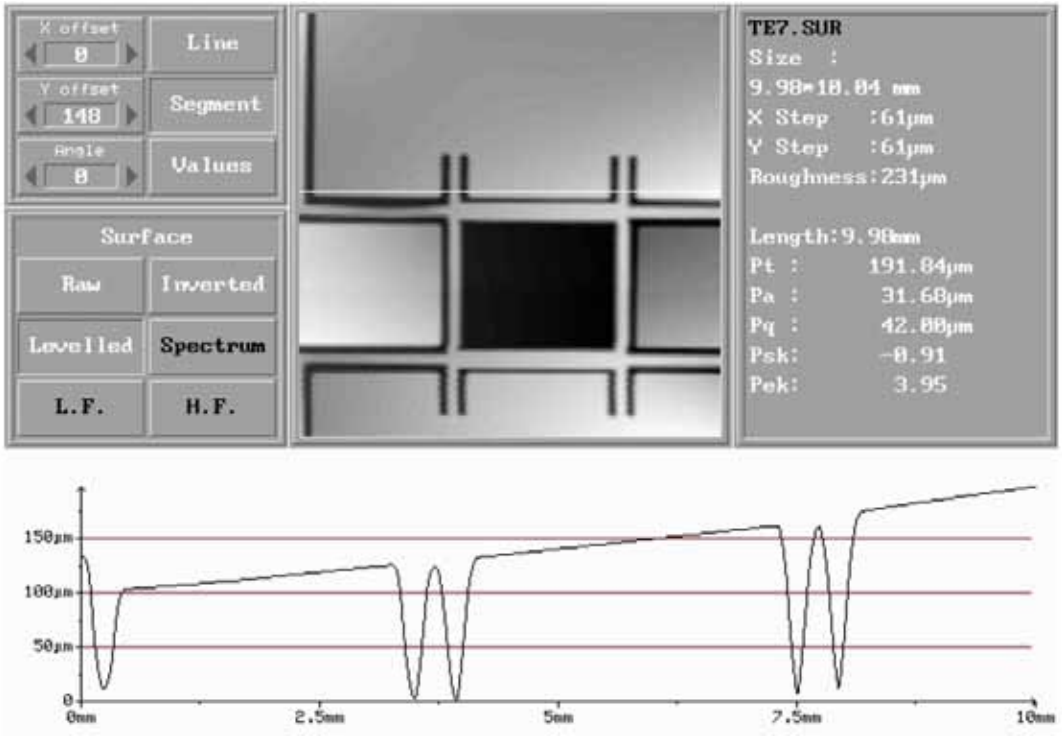


Figure 3.2.16: Horizontal Profile A of chemically etched centre piece

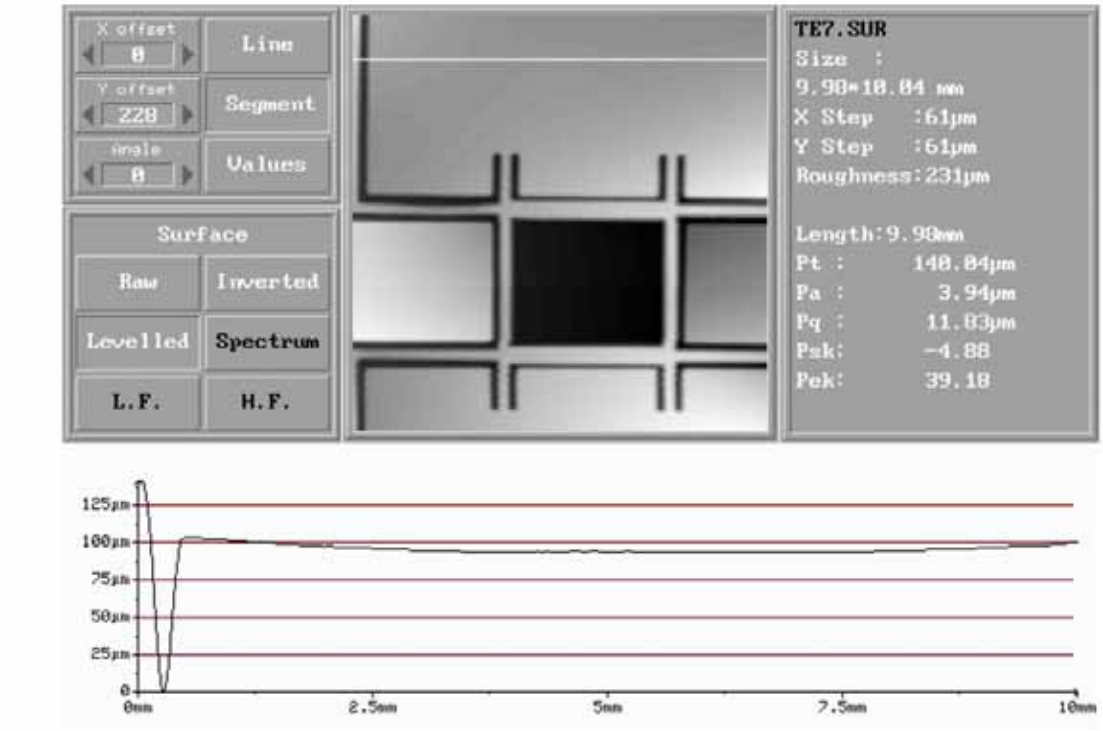


Figure 3.2.17: Horizontal Profile B of chemically etched centre piece

Figure 3.2.16 above shows the thickness reading of 125 ± 25 um, which is because of the thin film copper sheet being curved at the open edge. The result is correct at 100um ±10um with reference to Figure 3.2.17, where the copper sheet is held flat by the inner plate.

Table 3.2.1 gives a comparison result for some of the designed values and actual measurements for both approaches.

50um electroformed piece	Designed Values	Measured Values
Channel gap	0.200mm	0.219 ± 0.01mm
50Ω line width	0.086mm	0.079 ± 0.01mm
35.5Ω line width	0.120mm	0.084 ± 0.01mm
¼λ stub length	1.190mm	1.190 ± 0.01mm
¼λ stub width	0.050mm	0.041 ± 0.01mm

Table 3.2.1: Measurement of electroformed pieces

100um chemically etched piece	Designed Values	Measured Values
Channel Gap	0.700mm	0.700 ± 0.01mm
88Ω line width	0.170mm	0.175 ± 0.01mm
66Ω line width	0.340mm	0.346 ± 0.01mm
¾λ line length	3.750mm	3.796 ± 0.01mm
¼λ stub length	1.190mm	1.193 ± 0.01mm

Table 3.2.2: Measurement of chemically etched sample

The overall measurement satisfies the design requirement. A ±0.01mm error was estimated in the measured results, as the measurement is taken under a microscope by human eyes. The result indicates that both fabrication methods may be suitable for this application, although further work is needed on the electroforming technique to control the layer thickness.

3.2.2.2.2 mm-wave Measurements on Beamformer Elements

Two nominally identical 63-64 GHz crossovers and one separate branchline coupler were built from conventionally machined upper and lower layers, and chemically etched centre layers. Both were tested at Jodrell Bank.

Crossover A: The through port S31 shows average –6dB loss over the 60-65GHz Band. S11 return loss is matched at 63.5GHz. Some of the excess loss in the through port is believed to arise from loss and mismatch in the connectors. In this test, the inner conductors of the connectors were not soldered nor glued to the inner conductor layer of the squarax line. The contact was simply made and maintained by mechanical pressure.

Crossover B: Similar characteristics were observed. However, the through loss is better than that of crossover A at –4dB. And the S11 is –16dB at 62.5–63GHz.

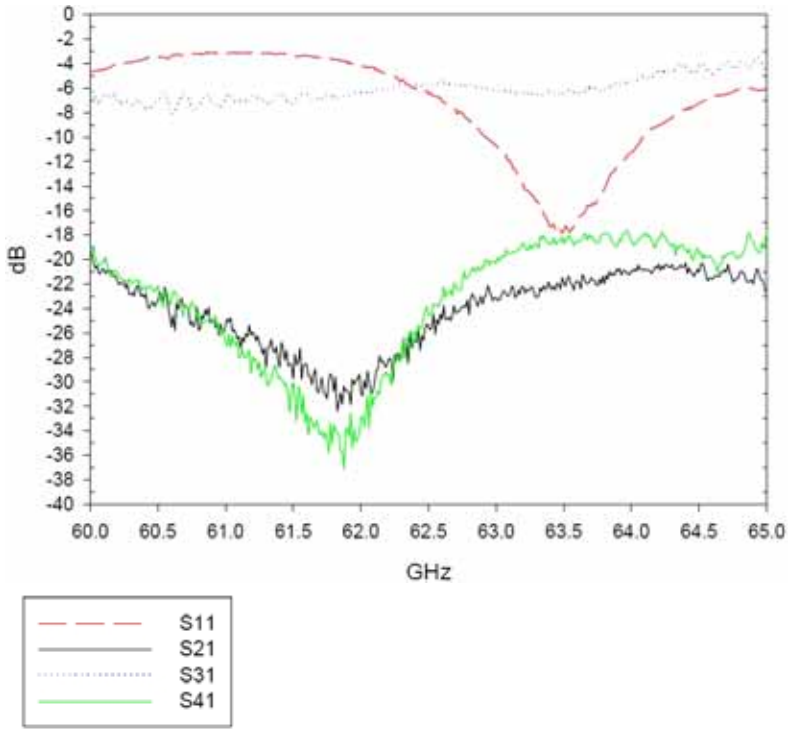


Figure 3.2.18: Crossover A. Measured Characteristics

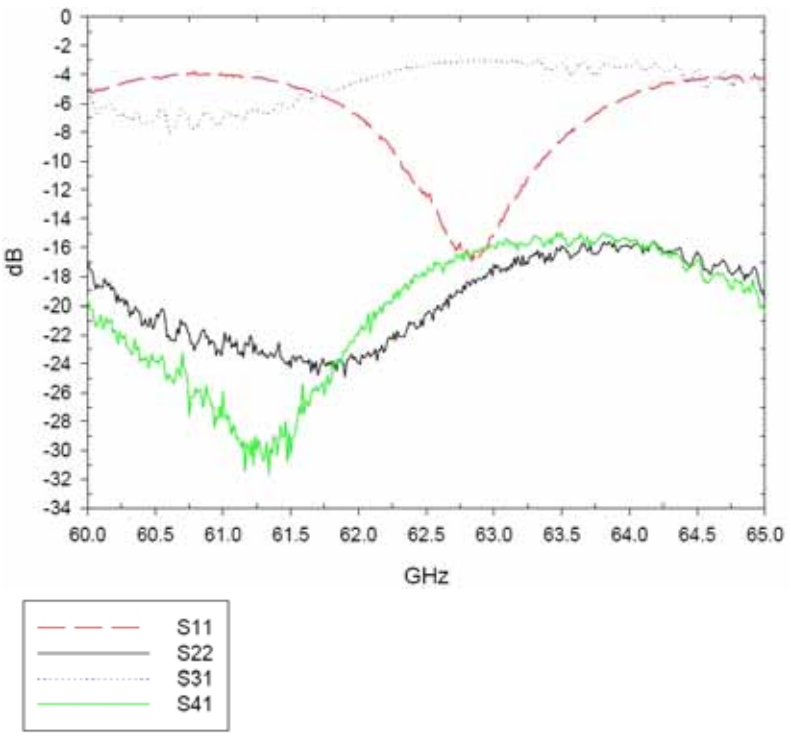


Figure 3.2.19: Crossover B. Measured Characteristics

Figure 3.2.20 shows the simulated result of the crossover design in the same format, showing low loss and a very good match on all ports.

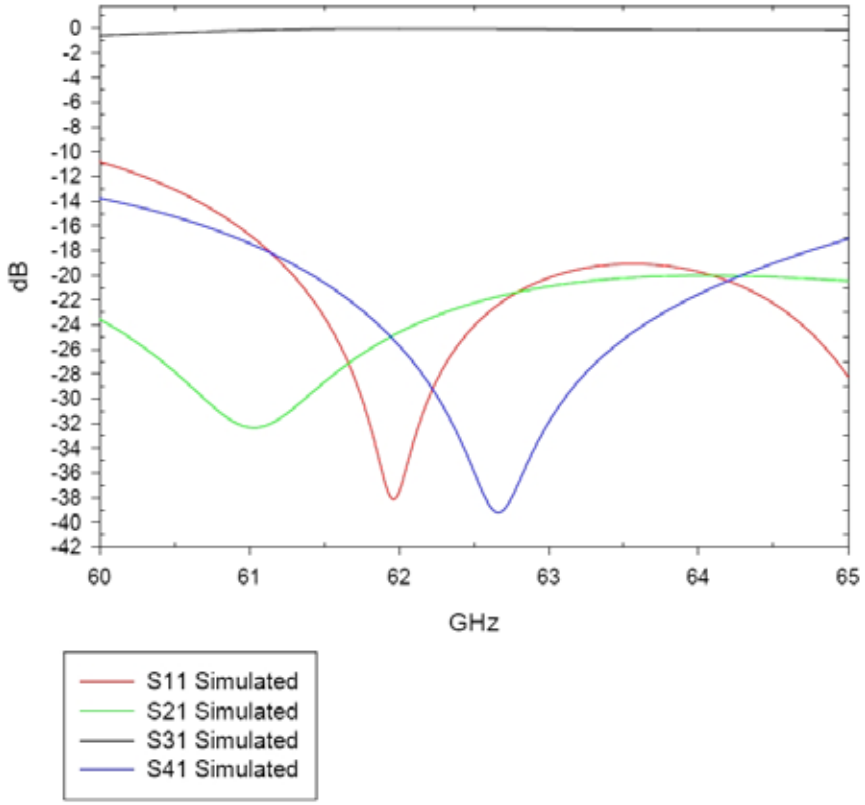


Figure 3.2.20: Crossover Simulation Results

3.2.2.2.2.1 Comparison between measured and simulated crossover results

The return loss for each of the ports of both Crossover A and B are compared with the simulated results in Figure 3.2.21 to Figure 3.2.24. They show a resonant match approximately 1 to 1.5 GHz above the expected resonant match, and all give a reasonable match, at least –10dB at 63GHz.

The S21 and S41 parameters give good isolation between the ports too. The through loss is higher, at –6dB at least and is very different from expected 0dB. We believe the manufacturing tolerance and the connectors have caused the loss.

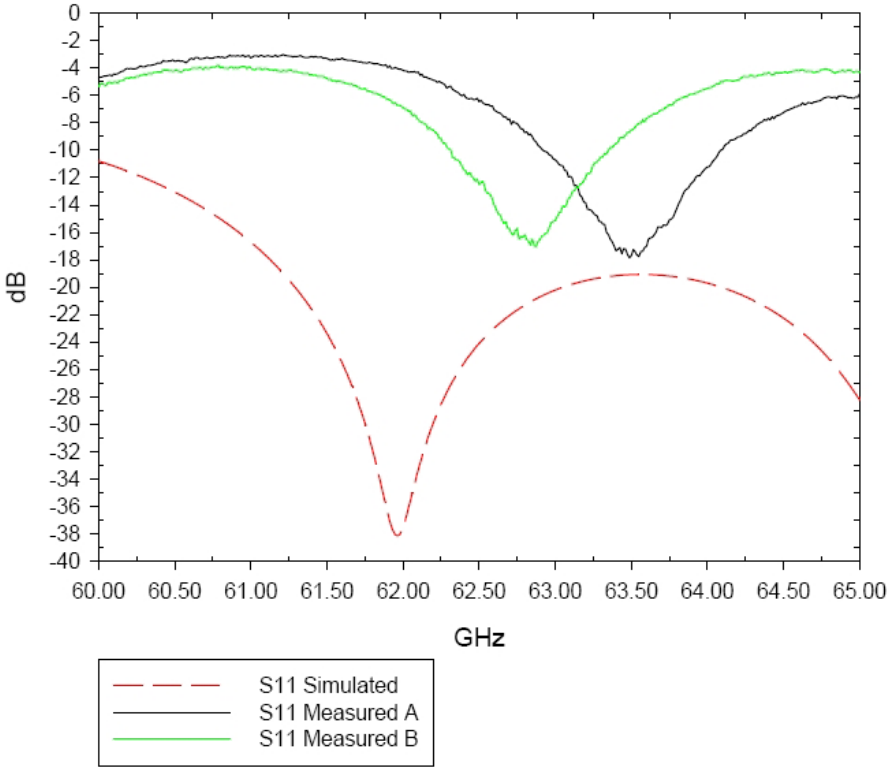


Figure 3.2.21: S11 Comparison

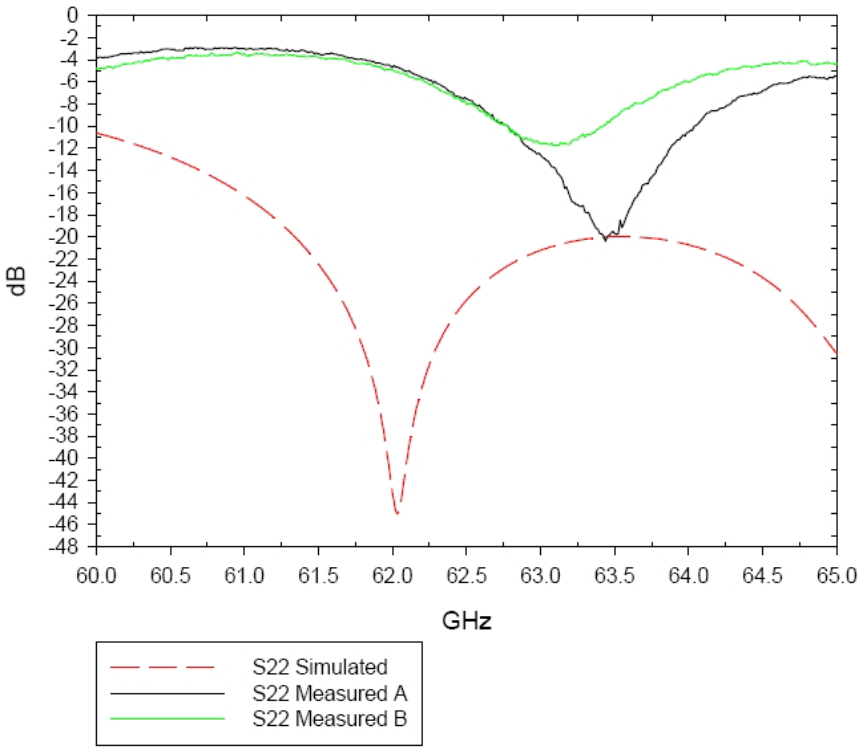


Figure 3.2.22: S22 Comparison

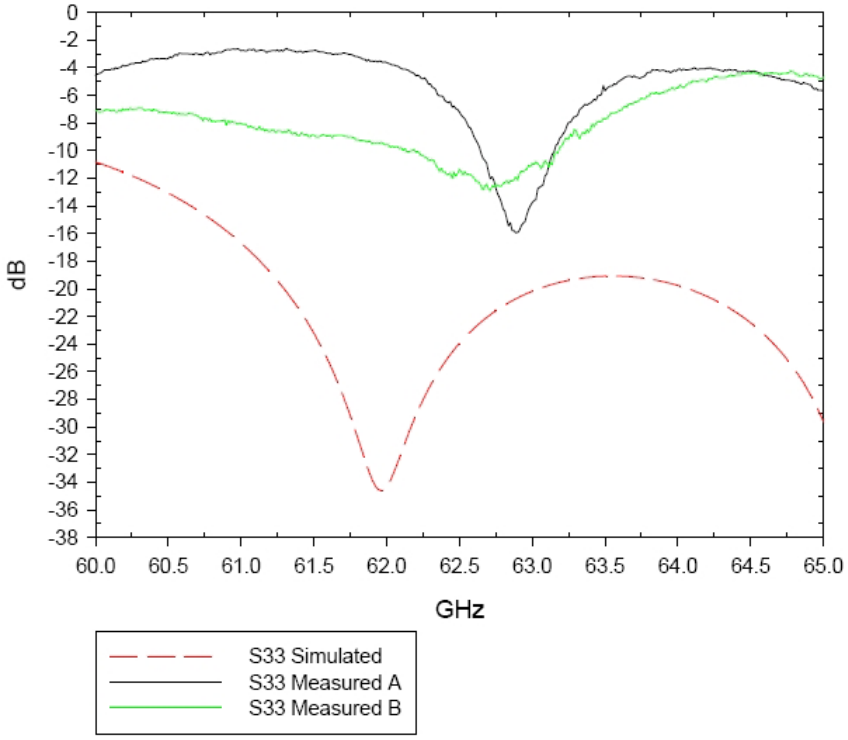


Figure 3.2.23: S33 Comparison

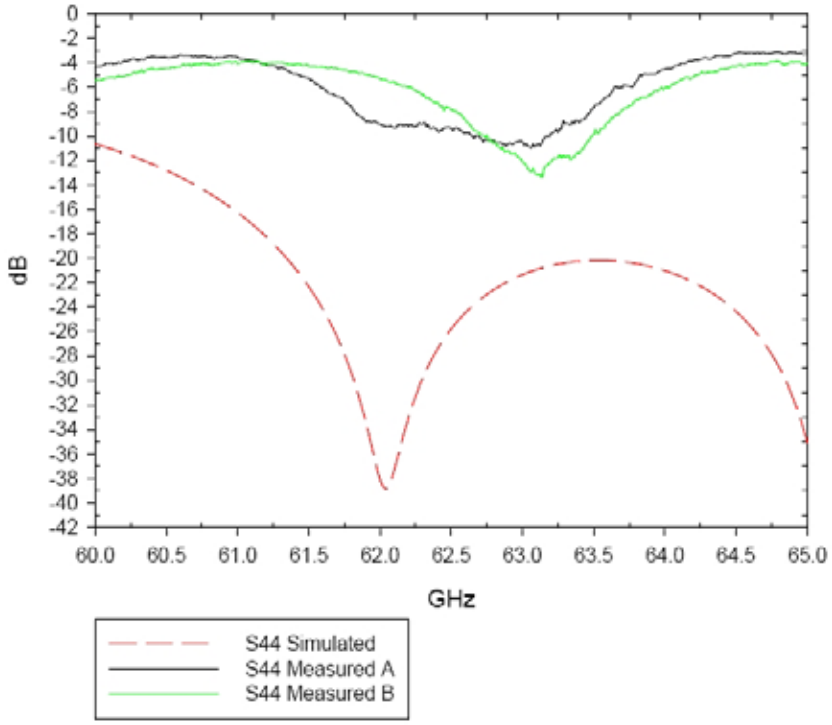


Figure 3.2.24: S44 Comparison

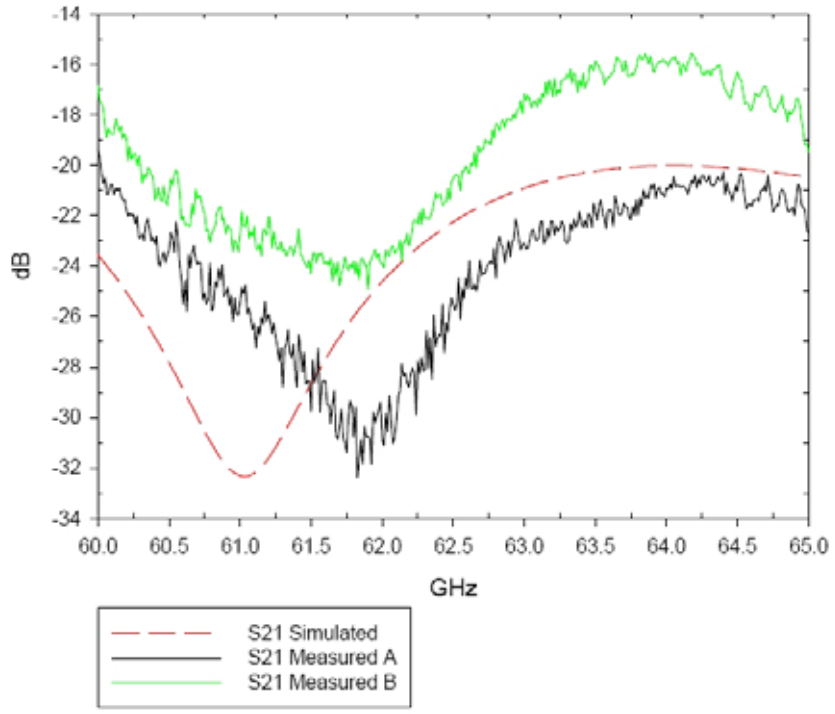


Figure 3.2.25: S21 Isolation Comparison

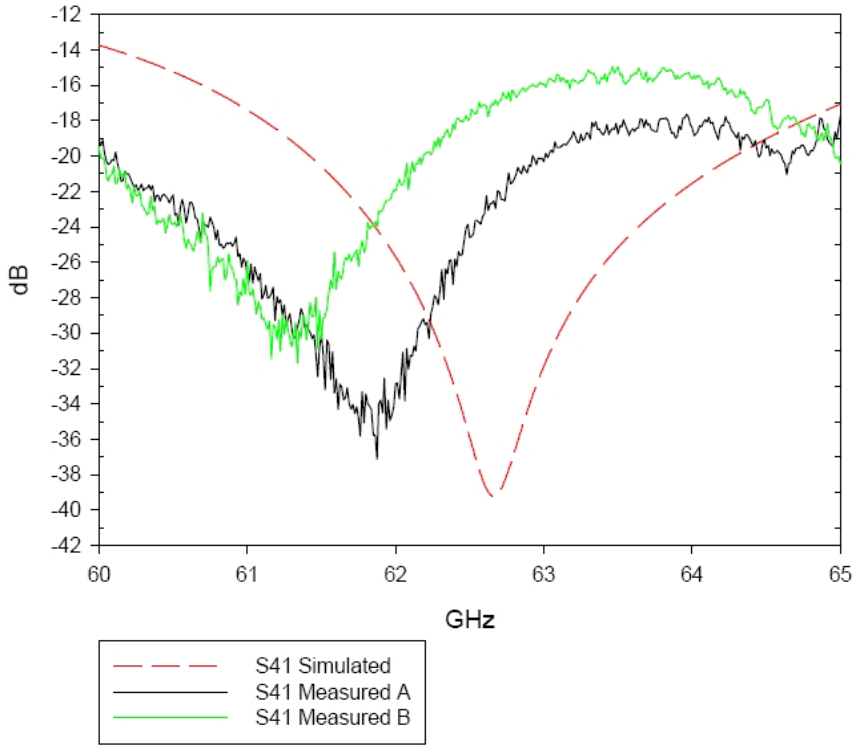


Figure 3.2.26: S41 Isolation Comparison

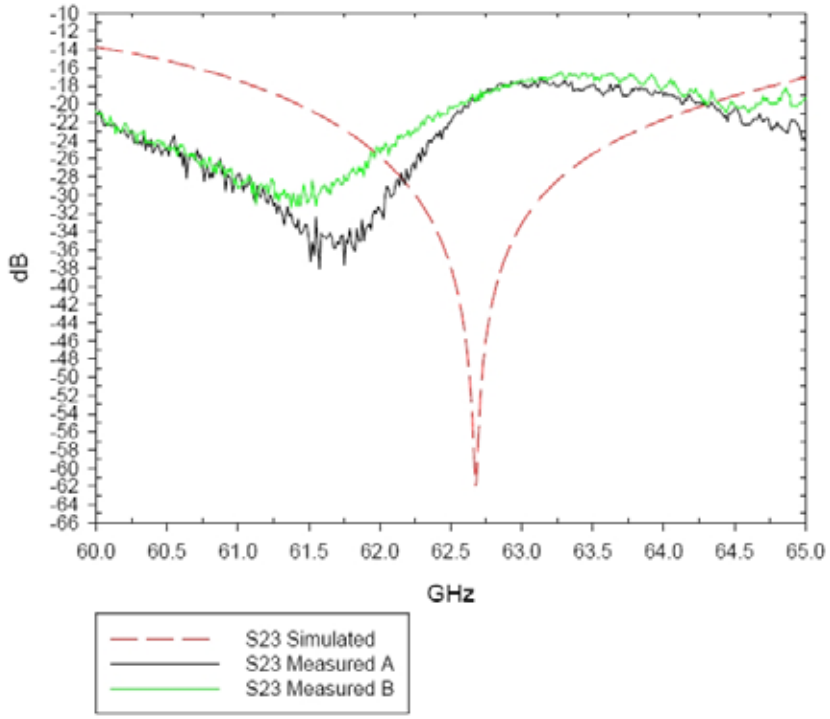


Figure 3.2.27: S23 Isolation Comparison

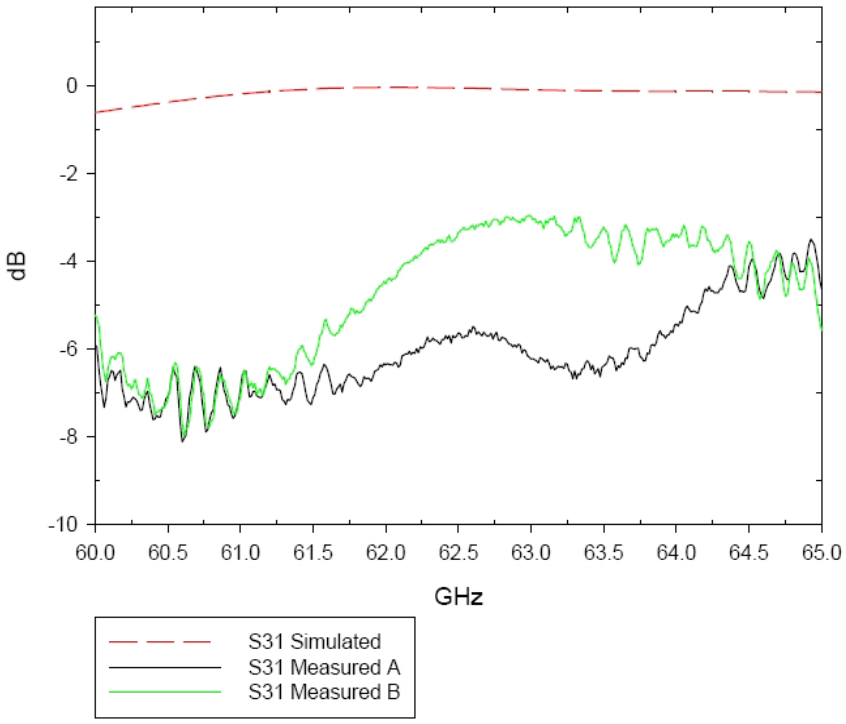


Figure 3.2.28: S31 Through-loss Comparison

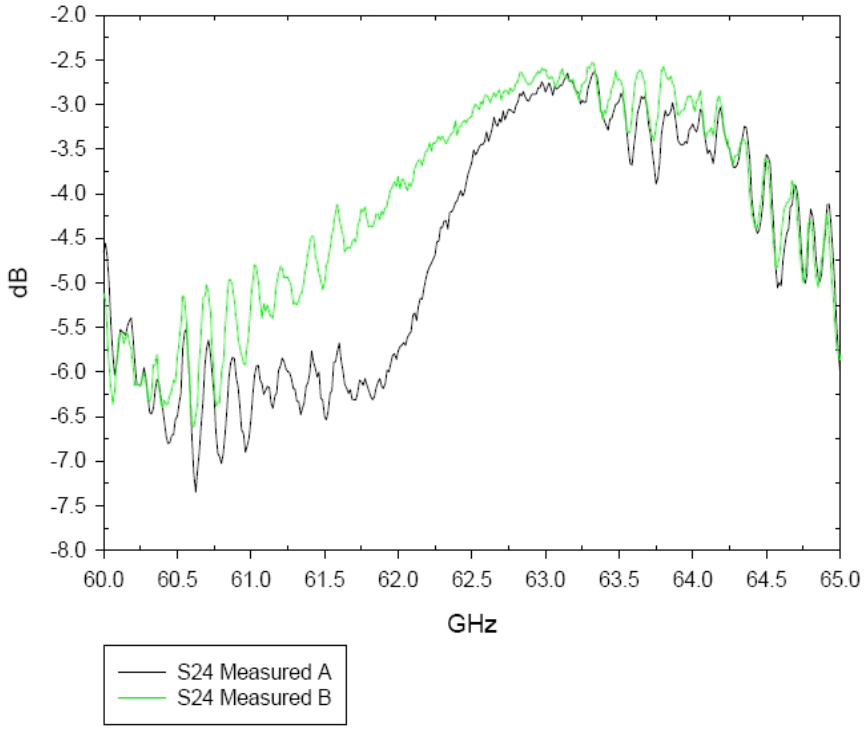


Figure 3.2.29: S24 Through-loss Comparison

3.2.2.2.2.2 Branchline Coupler Measurements

The S-parameters of the standalone coupler were also measured. The measured results are shown in Figure 3.2.30. The device shows the expected characteristics of a quadrature coupler over the 61–62 GHz range, with an excess loss of 2 to 3 dB. The deviation from the design frequency was expected because of known fabrication errors.

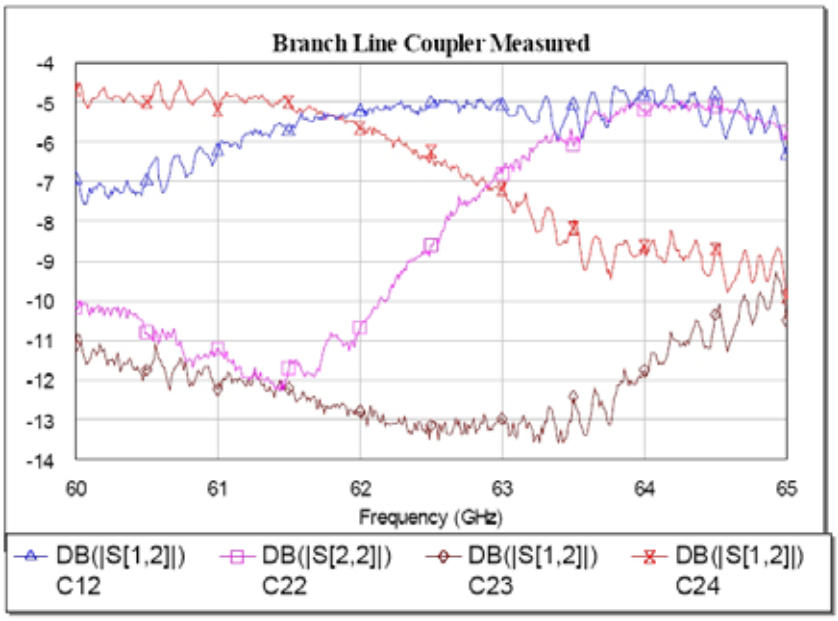


Figure 3.2.30: Branchline Coupler Measurements

3.2.2.2.2.3 Silicon Micromachined Structures

Further efforts have been made to produce the layers required for the multiplayer squarax beamformer components using etched silicon wafers. This work has shown that very high dimensional accuracy can be achieved in practice. The processes required for metalising the layers and bonding them together still need to be developed.

3.2.2.2.2.4 Layered Air Spaced Antenna Structures

Simulations and experimental measurements on scaled models of air spaced antennas have been carried out, in order to develop antenna structures that can be directly integrated with the squarax beamformer structures. The antenna designs investigated are air spaced patch antennas. Two variants of this concept have been studied. The first is a half wavelength air spaced patch antenna in which the centre conductor is supported by thin beams at the short circuit point at the centre of the patch, as illustrated in Figure 3.2.31. The second is a shorted quarter wavelength patch, in which the short circuit a quarter wavelength from the radiating edge of the antenna provides a natural means of physical support for the centre conductor, as illustrated in Figure 3.2.32.

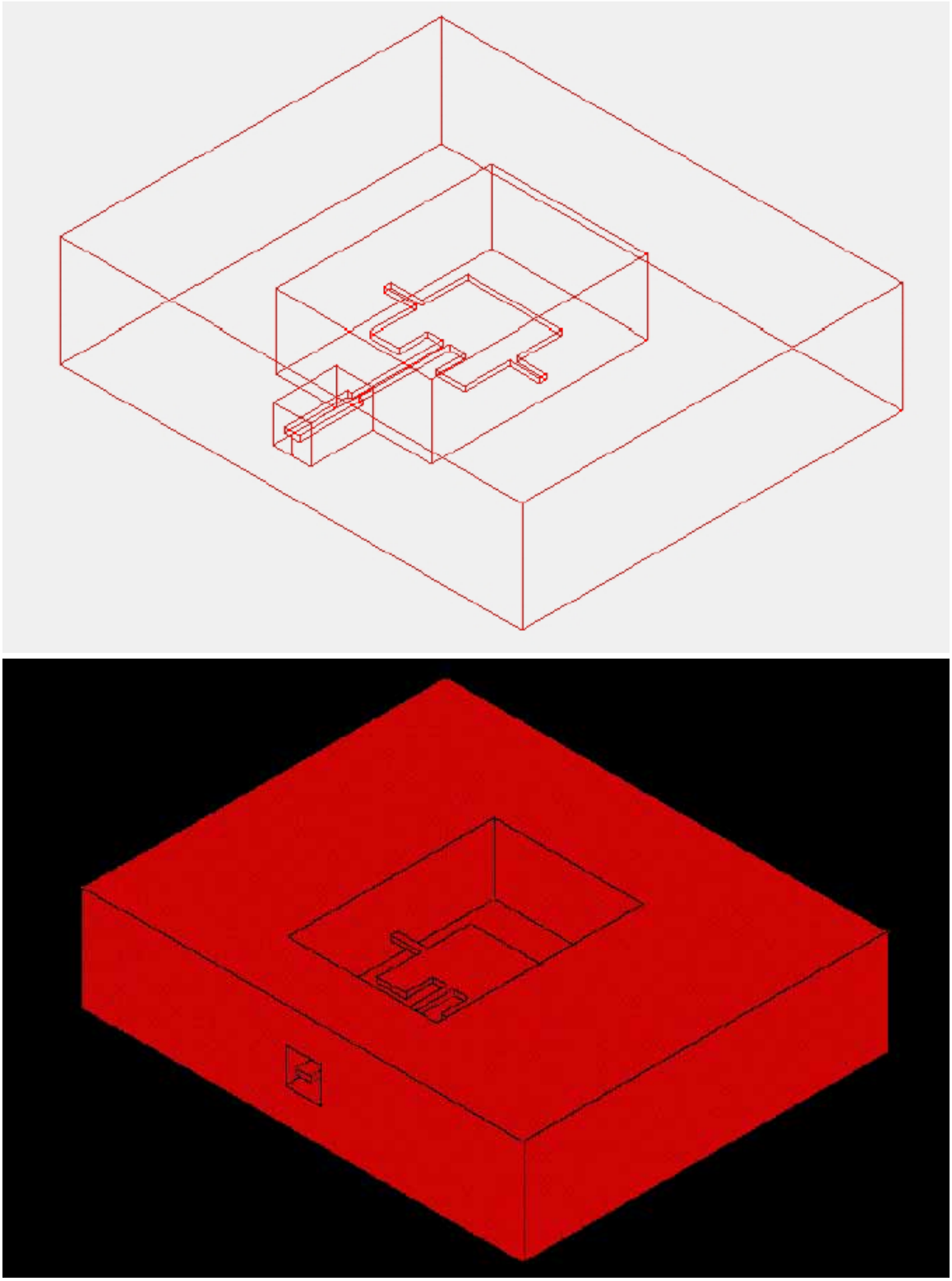


Figure 3.2.31: 3-D Views of the Half Wavelength Patch Antenna

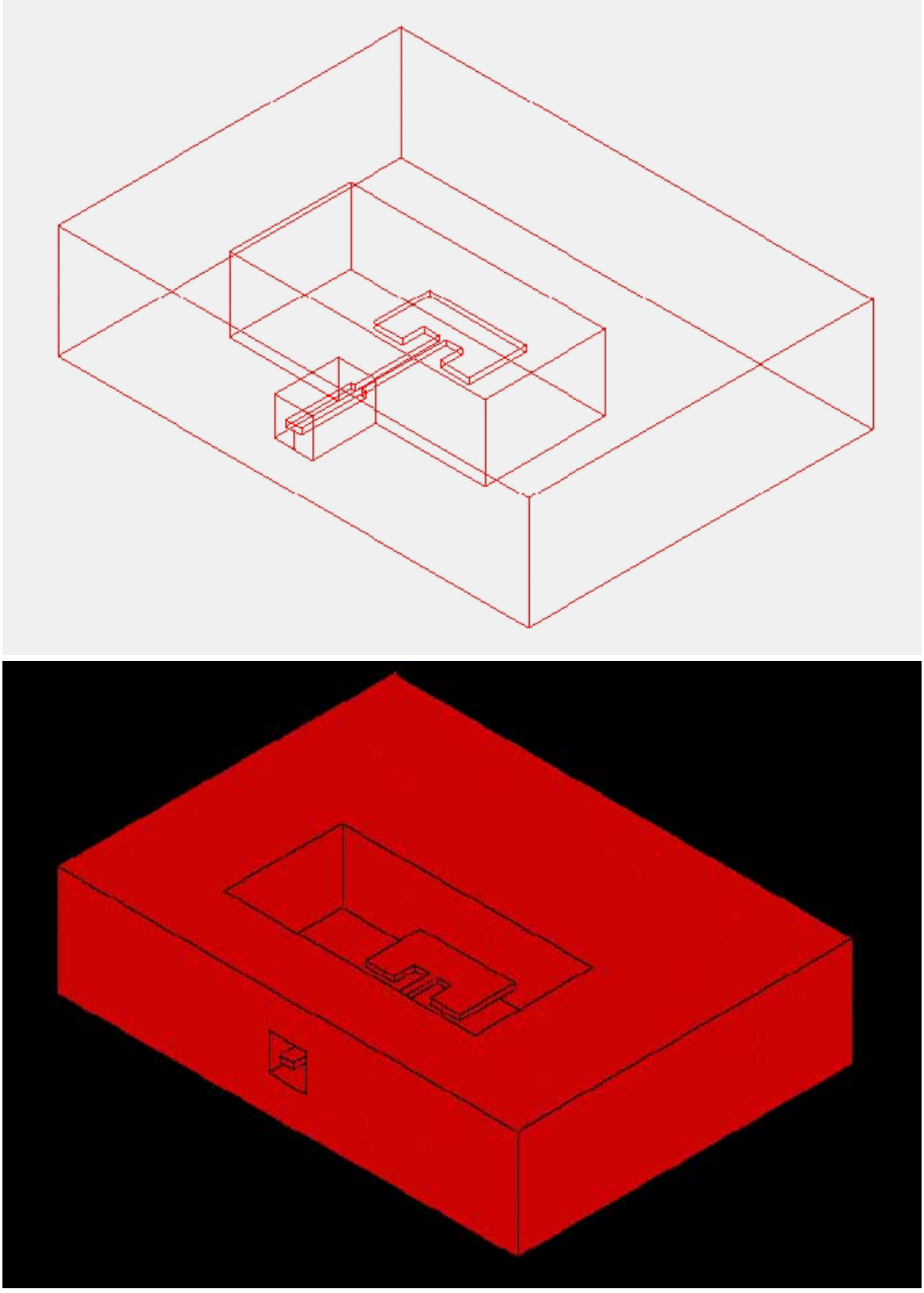


Figure 3.2.32: 3-D Views of the Shorted Quarter Wavelength Patch Antenna

3.2.2.2.2.5 Measured Results for the Half Wavelength Air Spaced Patch Antenna

Figure 3.2.33 shows the measured and simulated antenna patterns for the halfwave air spaced patch at 6.3GHz, showing good agreement between measurement and simulation, except for a frequency offset, from 6.3 GHz in the simulation to 6.5 GHz in the measurement. The patterns for the practical antenna were measured at the frequency that gave the best input-return-loss.

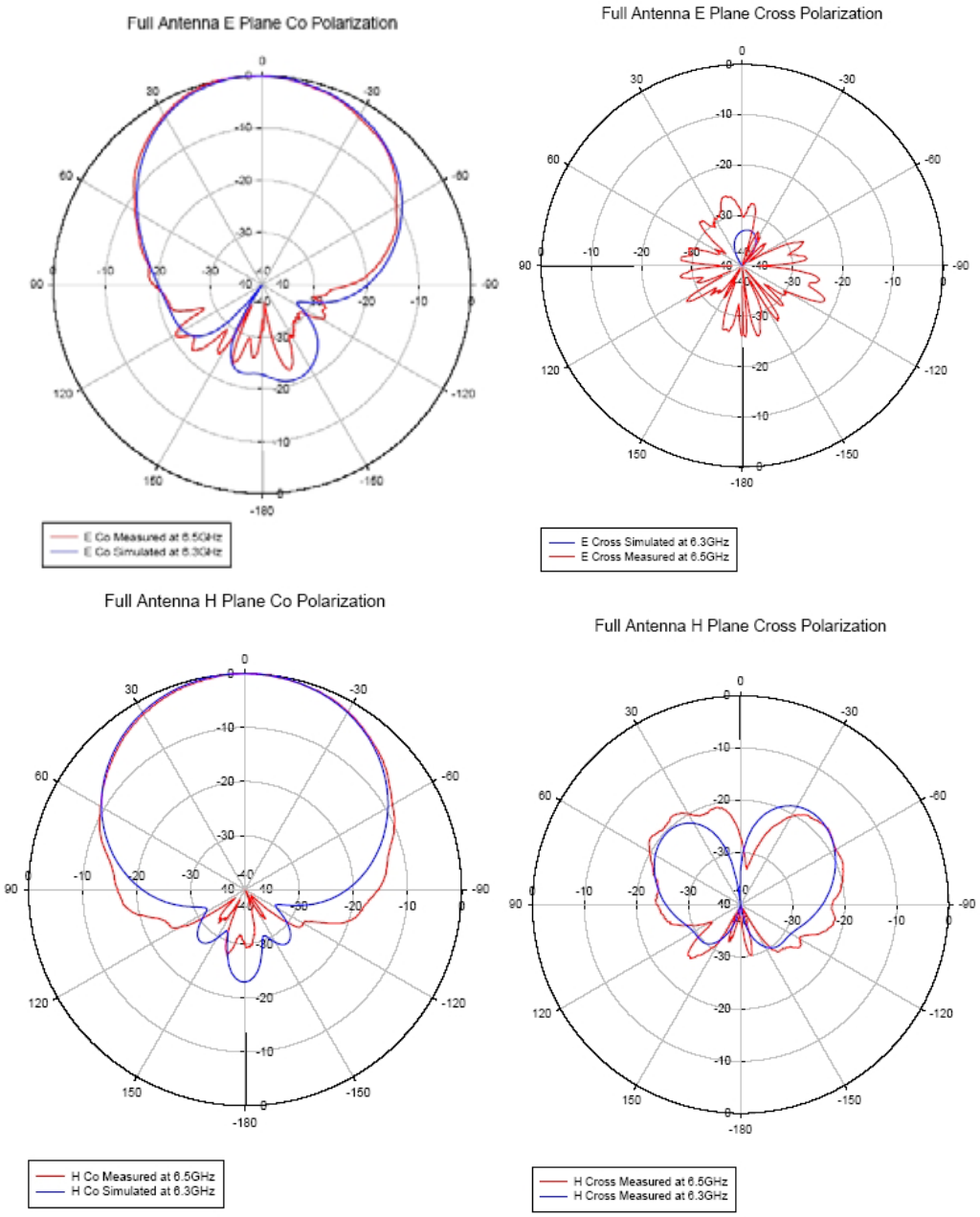


Figure 3.2.33: Measured and Simulated Antenna Patterns for Air Spaced λ/2 Patch

The E Plane Co Polarization pattern result agrees well with the simulation. The E Plane Cross Polarization pattern was expected to show very low cross polarization isolation, at around -34dB. The measurement result shows somewhat lower isolation, at a maximum –22dB, but this is still a good level of isolation. The H Plane Co Polar pattern shows good agreement with the simulation, except in the shape and level of the backlobes. The H Plane Cross Polar pattern shows good agreement in shape and level, with good levels of isolation.

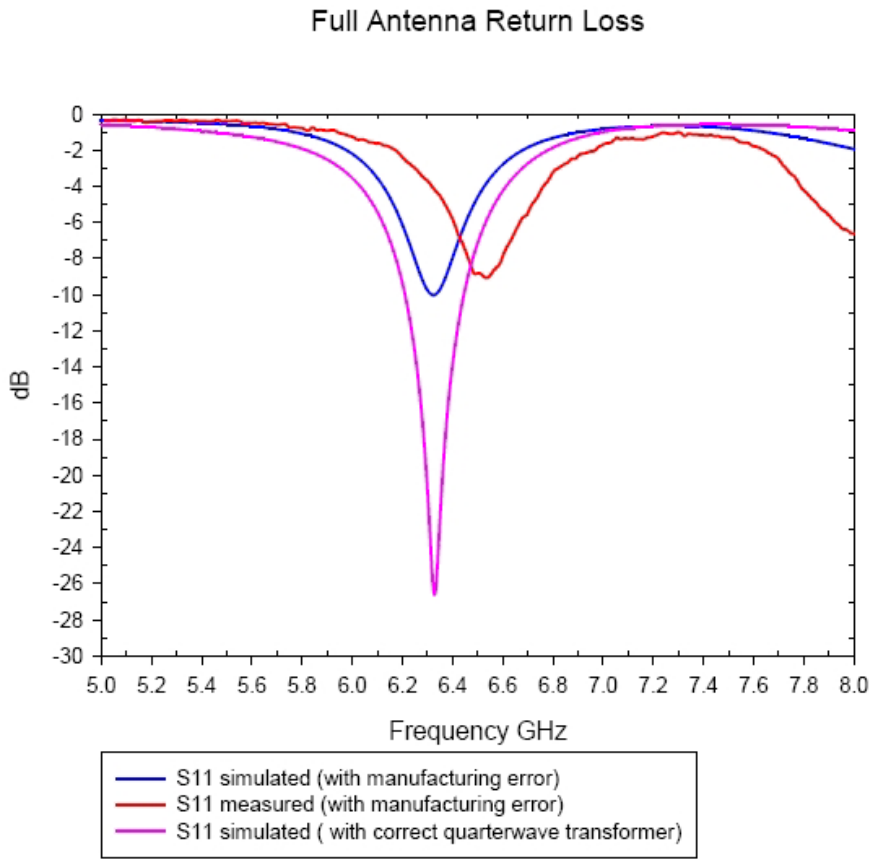


Figure 3.2.34: Measured and Simulated Return Losses of the Air Spaced Half Wavelength Patch Antenna

The return losses in both simulation and measurement agree very closely, although there is a slight offset in frequency. A dimensional error came to light after the unit was assembled and measured. Figure 3.2.34 shows simulated results for the ideal dimensions and the actual dimensions. The error was in the length of the transmission line transformer section, hence it is reasonable to believe that if the transformer length within the square coaxial line section is corrected, the return loss would be improved from –10dB to at least –20dB, as suggested by the simulations. The antenna pattern simulations used the actual fabricated antenna dimensions.

3.2.2.2.2.6 Measured Results for the Shorted Quarterwave Air Spaced Patch Antenna

Figure 3.2.35 shows the measured and simulated radiation patterns for the shorted quarterwave air spaced patch antenna, showing generally good agreement and without the frequency offset which arose in the half wavelength version.

The measured polar plot for E Plane Co Polarization agrees well with the simulation. The simulated polar plot for E Plane Cross Polarization shows absolutely no cross polarization radiation pattern. In the measurement, the cross polarization was very low with a maximum at about –20dB. The measured polar plot for H Plane Co Polarization agrees well with the simulation, but with two backlobes rather than only one backlobe seen in the simulation result. The polar plot for E Plane Cross Polarization agrees well the simulation, showing relatively high levels away from boresight. It is suspected that the high levels of cross polarisation radiation seen here are related to the wall thickness, possibly through the mechanism of a cavity mode.

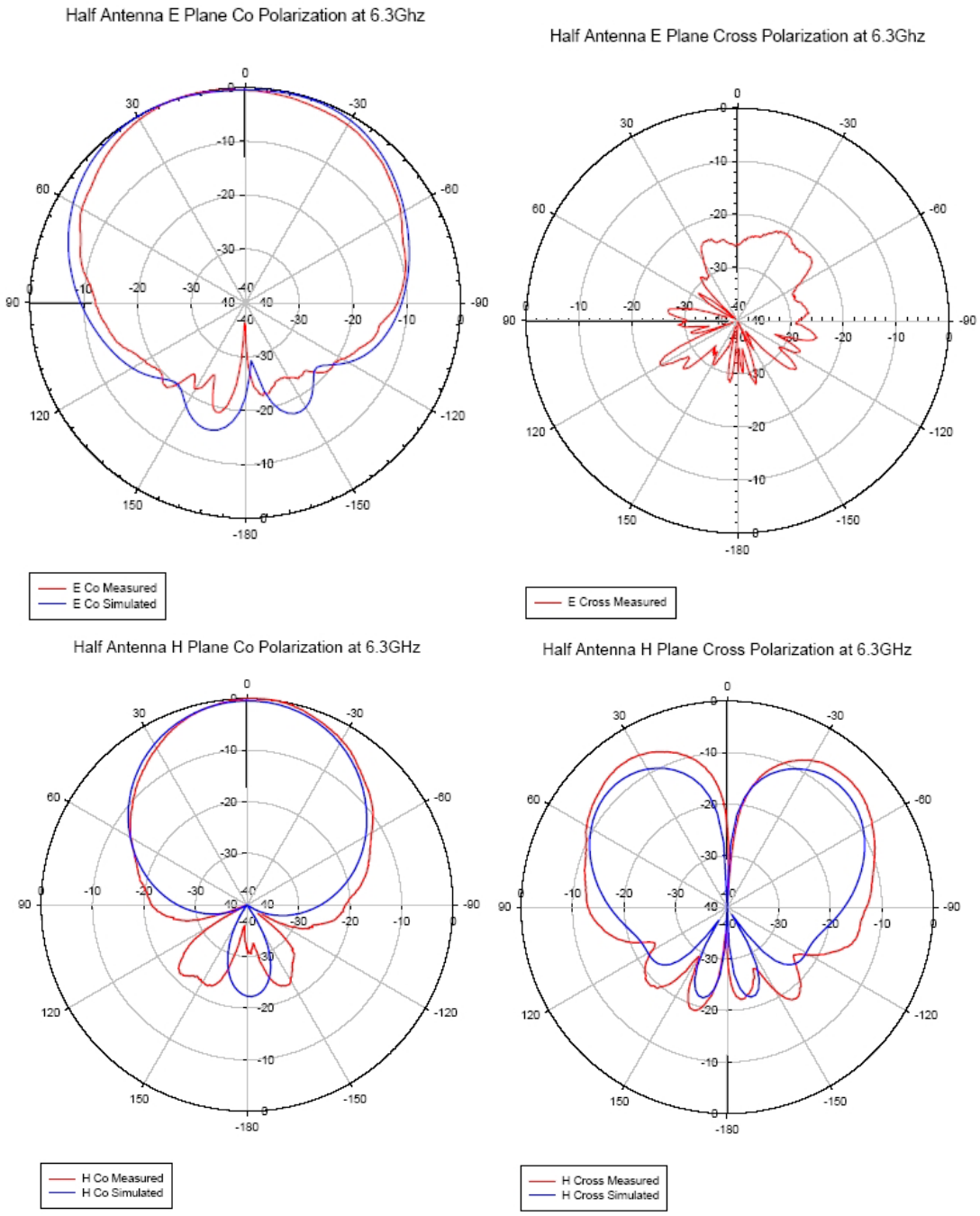


Figure 3.2.35: Measured and Simulated Antenna Patterns for Air Spaced λ/4 Patch

The measured and simulated input return losses of the quarterwave air spaced patch antenna are shown in Figure 3.2.36. The expected return loss was at least 20dB in the original design. However, the top layer wall was increased to 10mm to facilitate the mounting of the input SMA connector. As shown in the simulation, this causes the return loss to become poorer, at around 10dB measured. This can be improved in future designs, either by avoiding the use of flanged connectors requiring thick top layers, or by re-optimising the transformer to account for the changed impedance.

The return loss of the shorted quarterwave patch, S11, agrees well in both simulation and measurement.

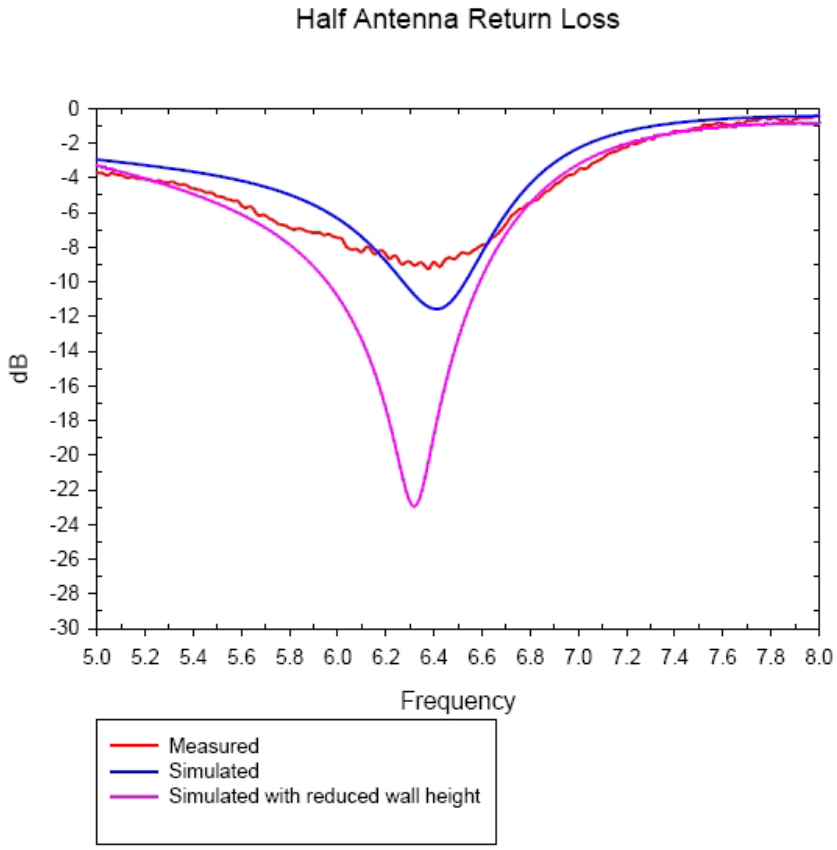


Figure 3.2.36: Input Return Loss of λ/4 Air Spaced Patch

3.2.2.2.3 Conclusions

The work on passive beamformer components has shown the potential for making low-cost components using multiplayer fabrication of squarax transmission line sections. Crossovers and couplers have been built at 63 GHz using chemically etched centre layers. Electroforming has been shown to produce layers with a smaller minimum feature size, but there is still a need to control the electroformed layer thickness. Etching of the required structures from silicon wafers has been shown to be possible, although further process steps still need to be developed to allow metalisation and bonding together of the layers. Suitable antenna structures have been designed for direct integration with beamformers in this multilayer construction technology. Scale models of the antennas have been built and demonstrated at 6.3 GHz. The centre conductor thickness in the scaled models was 1 mm. For 63 GHz operation, this would scale to 0.1 mm, the same thickness that was used in the mm-wave beamformer measurements, and compatible with silicon etching or (subject to further process development) electroforming. In the mm wave experimental work, a key limitation has been the cost, insertion loss and poor repeatability of the V-connectors used to introduce the signals into the squarax medium, and the difficulty and high level of skill required in assembling the interconnections. A better approach, both for future experimental investigations and eventual systems implementations, may be to use waveguide interfaces in place of coaxial connections. It should be possible to produce the waveguide to squarax transition in the same multilayer fabrication technology.

3.2.3 Laser Micromachining

3.2.3.1 Overview

Laser ablation can be used to accomplish subtractive and additive deposition and machining processing in a manner similar to silicon micro machining (see Section 3.2.4), although little evidence of its widespread use is to be found in industry or the academic literature.

The subtractive processes cover direct machining of both metals and non-metals to achieve sculptured shapes, hole drilling, device scribing, profiling and dicing, and for feature trimming and calibration. Of these applications, the most common use of laser ablation for micro-machining processes has been for precise trimming and calibration of micro-machined devices fabricated using wet chemical processing. Two examples of post micro-machining, mechanical calibration are given in [15], one in which the depth of a channel is controlled to 170nm in a 100µm deep channel (equivalent to 0.17%) and in the second the two tines of a tuning fork sensor are precisely balanced. In other micro-machining applications, in the wider electronics industry, laser trimming is routinely used to achieve high tolerance resistor values.

Laser machining processes, like traditional mechanical machining methods, result in some machining debris, which is re-cast back onto the device surface. In Figure 3.2.37, a micro-machined switch circuit, diced using laser ablation shows significant evidence re-cast debris. However, unlike traditional methods, the debris is not easily removed. For devices with moving parts, there is a possibility that this debris will migrate and contaminate the actuated parts, leading to failure. The formation and the re-casting of surface debris is most prevalent in so-called nano-second (pulse length) lasers.

These lasers machine by both plasma and heating/melting effects. It is the heating effect that produces the re-cast surface debris. In the so-called femto-second laser machining, only the plasma machining element occurs (i.e. no melting). The plasma-machined material is readily removed away from the device and is thus not re-cast onto the surface [16].

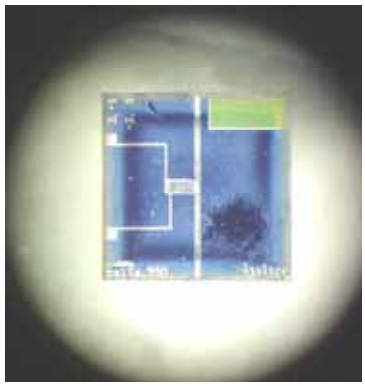


Figure 3.2.37: Micro-machined switch diced by laser ablation and showing re-cast debris.

For devices that include free-standing features, laser-dicing offers an advantage over more traditional dicing methods such as sawing, as no liquid coolants, which can lead to 'stick down' due to viscous forces, are used. As a result, laser-dicing techniques are likely to be developed for micro-machining applications.

Additive processes use laser ablation of target materials to deposit layers of metals and dielectrics onto host wafers in a similar manner to sputtering. This technique has been used for the fabrication of thin films in other areas of electronics, e.g. in the deposition of thin film, high temperature superconductors. However, to date there is no substantive evidence that the technique has been used for additive micro-machining applications.

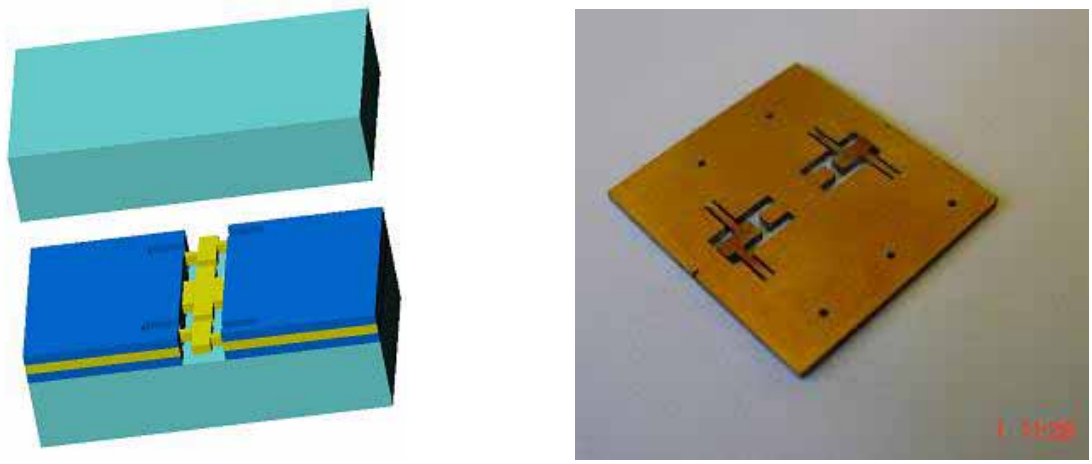
3.2.3.2 Laser Micromachining at the University of Birmingham

The Emerging Devices Technology Group at Birmingham has successfully demonstrated the potential for laser micromachining in making a 2-pole Chebychev 9 GHz band pass filter, with 70% fractional [17]. The filter was made using multilayer air-spaced square cross section coaxial lines. The individual planar layers making up the structure were produced from conventionally machined thin metal sheets.

The same transmission line techniques have been shown by simulation to be compatible with higher frequency filter designs, using a laser machined central layer of 700 micron thickness (as illustrated in Figure 3.2.38, with a simulated response shown in Figure 3.2.39). Sample micromachined parts have been produced by a third party contractor and shown to meet the required dimensional specifications for a mm-wave version of the filter, although initial RF measurements appear to show higher-than-expected insertion, possibly due to deterioration of the edges in the laser machining process. Further investigation of this issue is required.

The laser processes available includes laser drilling and laser cutting, which can produce features down to 2 μm in size in materials up to 1.5 mm thick. A number of laser micromachining systems are available for drilling of accurate, small holes (typically 5-200 microns diameter), very accurate cutting (kerf widths down 5 microns) and 2.5D milling of microfeatures. With the appropriate choice of laser, these systems can be used to machine most materials (metals, ceramics, polymers, diamond etc.).

The multilayer air-spaced squareax approach is also suitable for direct integration with a range of antenna structures, including patches and slots. The antenna concepts have been demonstrated with conventional machining at low frequency [18]. Further development work on multilayer air spaced beamformer networks and antennas is underway in the Miltrans project (with BAE Systems, Qinetiq and Panorama Antennas) to produce related designs at 63 GHz. Present indications, however, are that chemical etching is equally capable of achieving the required tolerances for this band at lower cost. The situation may, however, be different for higher frequency applications, where the dimensional capabilities of chemical etching are unlikely to be adequate.



(a) (b)

Figure 3.2.38: (a) 28 GHz Multilayer Squarex Filter Concept.
(b) Laser Machined Central Layer.

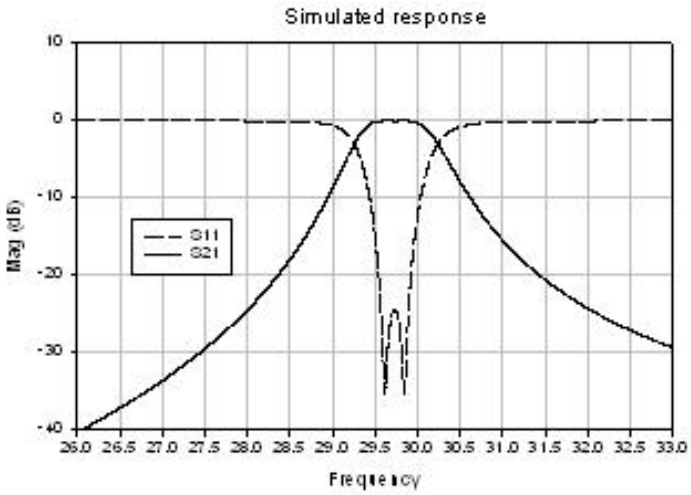


Figure 3.2.39: Simulated response of 28 GHz filter.

3.2.4 Silicon Micromachining

3.2.4.1 Overview

Micro-machining techniques for UHF, microwave and millimetric applications have been demonstrated on an variety of substrate/wafer[1] materials e.g. alumina, quartz, glasses, silicon carbide, diamond, gallium arsenide, silicon etc. The vast majority of RF applications over the past decade have used silicon.

Silicon and, to a lesser extent, gallium arsenide have been favoured, as the perception was that the established low-cost batch processing technologies used in the semiconductor industry would easily be flowed across to the new micro-system technologies (MST). Furthermore, it was believed that MST could be piggy-backed onto the established semiconductor foundry processes. This has not proved to be the case, particularly for RF applications. The structures required are many orders larger and include moving mechanics. Also, the preferred conductor material, namely gold, is excluded from semiconductor foundries owing to the potential for contamination. The solution has been to develop batch semiconductor technologies for MST in independent clean room facilities to suit the RF applications.

As micro-machined RF devices to date have been, and are likely to remain, predominantly silicon-based, silicon machining techniques will be considered. There are two categories of micro-machining for RF devices and distributed element structures: subtractive and additive. Both technologies start with a silicon wafer.

In the subtractive process devices and structures are machined into the bulk of the silicon wafer. The bulk machining process tends to provide 'piece parts', which are then processed further by additive processing or by assembly with other parts. By contrast, in the additive process, structures are fabricated by first 'adding' multi-layers of insulator, conductor and structural materials. To create free-standing structures, sacrificial layers will be included. Structures and conductor patterns are 'machined' by selective etching processes.

One key requirement of on-chip antennas is small size, due to the high cost of wafer space. Therefore, because of the fundamental limitations in antenna directivity mandated by the small size of integrated antennas, the radiation efficiency is one of the most important figures of merit for such antennas. Thus, an important objective of the research on monolithic antennas is to maximize the radiation efficiency of small antennas, for instance by using micromachining methods compatible with the active circuits integrated on commercial, low resistivity Silicon (Si) substrates.

Several fabrication technological processes are available, such as:

- *Silicon Bulk Micromachining*

  Bulk micromachining refers to processes where parts of the bulk of the semiconductor substrate are selectively removed by etching processes. Two major techniques are used for bulk micromachining of Si substrates: (chemical) wet etching and dry etching.

[1] Substrate and wafer have the same meaning, substrate being used by RF engineers, while wafer is used by process engineers.

In chemical wet etching, the surface of the Si wafer is masked by a durable mask (such as Silicon Nitride), with openings where a liquid is allowed to etch the substrate. Wet etching can either be isotropic, where the etching progresses with the same rate in all directions, or anisotropic where the etch rate in certain directions is restricted by the (111) crystal planes in Silicon. The anisotropic etch leaves slanted walls of etched cavities if a Si wafer with the standard crystal orientation (100) is used. Anisotropic etching is a standard Silicon micromachining process. Several kinds of etchants are available: KOH (with eventually isopropyl alcohol, IPA, to increase the selectivity Si/SiO_2), EDP (with SiO_2, Si_3N_4, Au, Cr, Ag, Cu or Ta mask layers), and TMAH that presents the advantage to be compatible with IC technologies. For GaAs substrates, the principle is similar, but the etchants are different (H_2O_2 combined with acids, for instance).

Dry etching is performed in an evacuated chamber where plasma is generated and used to etch the Si substrate. The wafer is masked by photoresist and patterned with photolithographic techniques to enable selective etching. In the commonly used Deep Reactive Ion Etching (DRIE), the wafer is exposed to an alternating sequence of an etchant and a passivant. By the alternation between etching and passivation of the substrate, the sidewalls of the etched holes are protected, thereby enabling high aspect ratio structures to be manufactured.

- *Membrane technology*

  Thin membranes of high quality dielectric materials offer a way of integrating high quality transmission line structures and antennas on semiconductor substrates. By suspending the conductors on membranes in air, an effective dielectric constant close to one can be achieved. Low losses are also obtained since the Si/GaAs substrate is removed in the vicinity of the transmission lines or antenna conductors. A low temperature membrane process, compatible with pre-processed semiconductor wafers, is also obtained by combining the spin-on Benzocyclobutane (BCB) dielectric process with bulk micromachining. The BCB membrane is released by backside etching of the wafer, using wet etching methods such as KOH or DRIE.

3.2.4.2 Physical attributes and electrical properties of silicon wafers for micro-machined RF applications

Precisely controlled wafer fabrication methods have been developed for the semiconductor industry over many years. The result is that the dimensional control of silicon wafers is higher than that the microwave community are used to from conventional microwave integrated circuit (MIC) substrates such as alumina. In most RF applications, the RF signal propagates through the silicon wafer material at some point. To achieve acceptable loss, the silicon material must have a high resistivity, which maps to a low loss tangent [10]. Recent commercial products [11] claim silicon resistivities of up to 30KΩ cm. However, these values are for a few selected wafers, which would be available only in small quantities and at a high premium price. A more realistic commercial specification is 10KΩ cm, which corresponds to a loss tangent of 0.0016. Fine features and front-to-back side alignment dictates the use of double sided polished (DSP) wafers.

3.2.4.3 Subtractive processing

Micro-system devices are commonly fabricated in bulk silicon by machining directly into the wafer. A common method has been to use bulk chemical etching techniques but more recently deep reactive ion etching (DRIE) has been shown to offer advantages to RF applications.

Bulk etching relies on the properties of silicon wafers cut along different orientations of the crystal. These cuts provide a number of different machining opportunities. A common cut, identified as the (100) orientation, will preferentially etch along one crystal plane and yields a sloping profile. It is limited to orthogonal patterns. By appropriate masking, shaped structures are produced e.g. movable armatures for RF switches or membrane supported low loss conductors.

The DRIE process uses two-stage etch-and-passivation chemistry to machine deep sections with essentially vertical walls. The process has another advantage, in that the machining is not constrained to orthogonal patterns. Complex shapes, peninsular features, membranes and thin cross-section support ribs can be fabricated.

Thin (typically 1µm thick silicon nitride) membranes have been used at millimetric frequencies to eliminate the dominant dielectric losses and increase physical size of antenna feed networks and antennas. Reference [12] uses the bulk etching approach and makes brief reference to a 20GHz receiver front end while a more recent publication [13] describes a 45GHz antenna application. The antenna shown in Figure 3.2.40 is an end fire, Yagi-Uda design. Significantly, the fabrication uses the DRIE process to achieve the membrane and an extremely thin (50µm) front-end support to minimise the field pattern distortion.

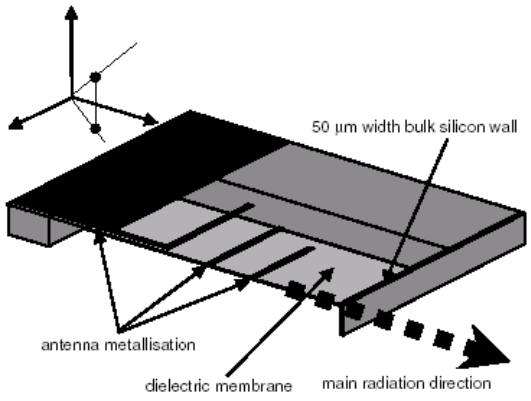


Figure 3.2.40: Membrane Supported Antenna (taken from reference [4]).

Within BAE Systems, bulk etched membrane structures have been applied to low-loss resonators and filters for the 10GHz band, Figure 3.2.41.

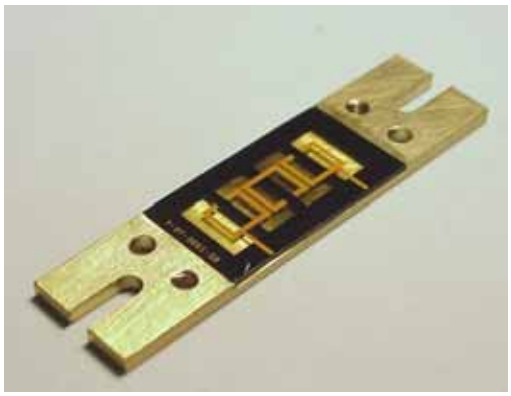


Figure 3.2.41: Membrane Supported Filter.

Studies to apply the technology to low-loss antenna feeds for a 60 GHz automotive application have been carried out. By comparison, the path loss is significantly lower than the more conventional 'soft-board' microstrip approach. Figure 3.2.42 shows a proposed demonstrator 4×4 Butler matrix. In practice, additional support ribs would be required to support the large area membrane. For the soft-board solution, the matrix was based on a 3dB branch-guide hybrid.

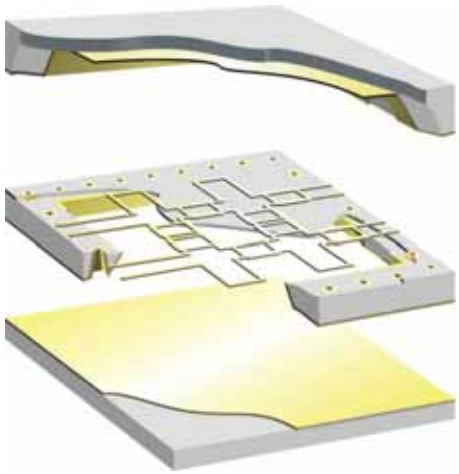


Figure 3.2.42: Proposed Membrane Supported 4 x 4 Butler Matrix.

Owing to the high frequency and material dielectric constant, a three-quarter-wavelength design was used. The effective dielectric constant of the membrane configuration is close to unity, hence the wavelength is longer and a conventional quarter-wavelength design can be implemented, resulting in broader bandwidth. Tandem coupled hybrids offer further bandwidth advantage. However, to implement the design will require developments to the air-bridge technology used in the semiconductor and MIC industries.

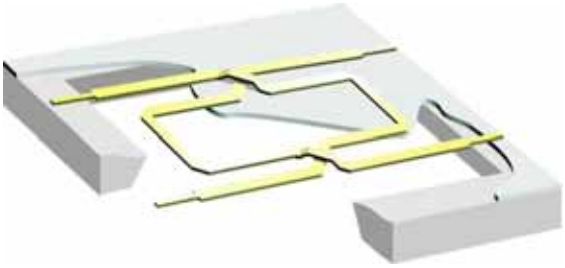


Figure 3.2.43: Proposed Broadband 3dB Hybrid.

3.2.4.4 Additive processing

This is the most widely used process for fabricating RF MEMS devices. It is a complementary process to conventional MIC processing but achieves much higher levels of complexity. Starting with a polished silicon wafer, layers of dielectric, metal and structural materials are deposited using chemical/thermal, evaporation and sputtering processing. Etch-back and pattern-plating processes define the required circuitry and 3D structures e.g. electro-mechanical switches. Etch-back techniques utilise either wet chemical or dry ion etch processes, which give greater scope for innovative structures. A multiplicity of deposition and etching processes have been developed and are in common usage. In many cases, the differences for a specific process type are only subtle but they can have a profound effect on the processing flow and resultant material parameters. This wide range of available machining techniques can itself be a limiting factor, as all processes cannot be covered in a single fabrication centre. MEMS designs then tend to become process specific.

The additive techniques have generally been used for components other than antenna feeds and antennas e.g. switches, phase shifters. A recent publication [14] reported on an application of MST to switched matrices for scanned arrays; switches (MST) and interconnects (LTCC) Figure 3.1.4.5. It is easy to imagine that the matrix could be integrated using an all MST approached and scaled to the millimetric band.

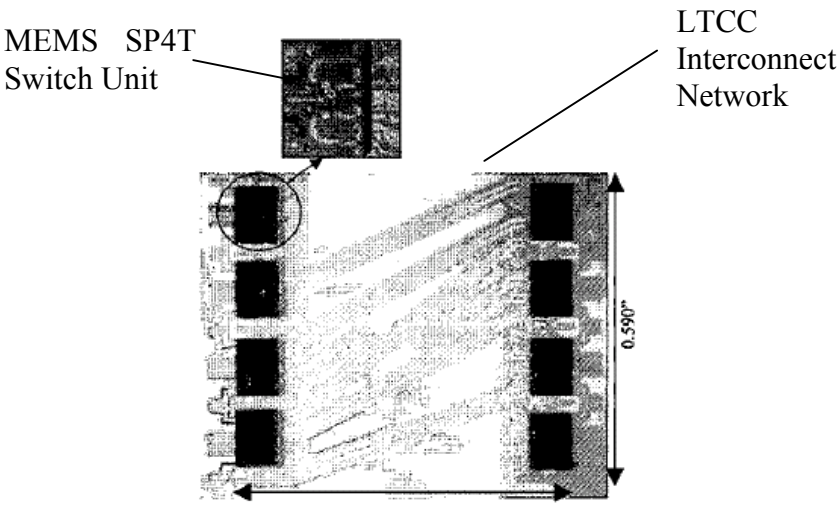
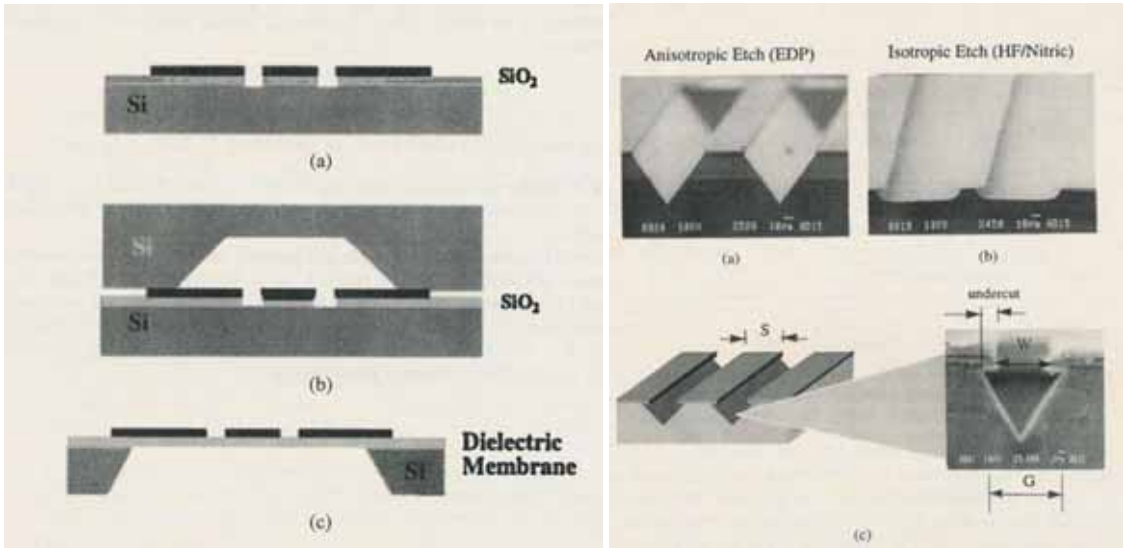


Figure 3.2.44: MEMS/LTCC 4 X 4 Switch Matrix (Taken from reference [14]).

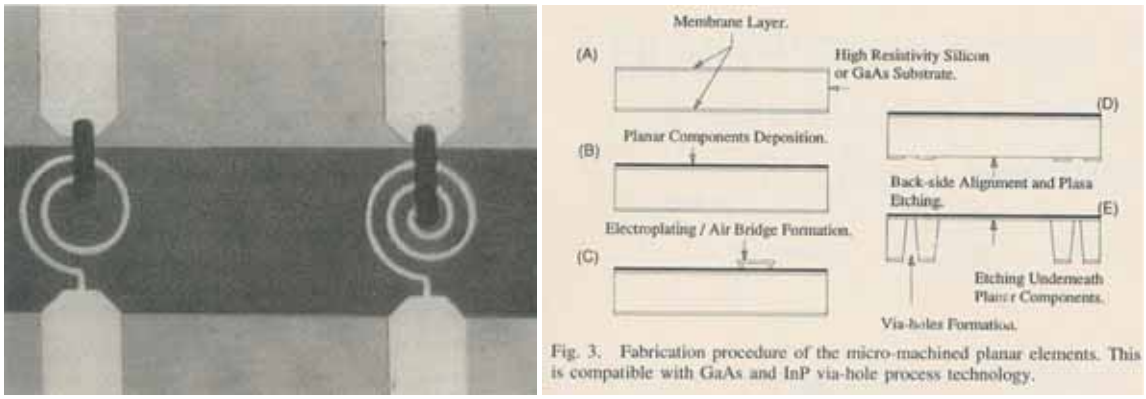
3.2.4.5 Some applications of membrane and Silicon bulk technologies

Micromachining techniques are used for the fabrication of (i) low loss transmission lines in microstrip or coplanar waveguide technologies (see Figure 3.2.45, taken from [19]), (ii) lumped elements (e.g. Figure 3.2.46, [20]), micromachined filters (e.g. Figure 3.2.47, [21]; see also [40]), diplexers [41], oscillators, and many more.



(i) (ii)

Figure 3.2.45: (i) Micromachined finite ground coplanar (FGC) waveguides (500µm-thick Si substrate with $SiO_2/Si_3N_4/SiO_2$ 1.5µm-thick membrane). Electro-plated Cr/Au metal patterns are obtained by lift-off process. Measured effective permittivity equals 4 at 110 GHz [19]. (ii) FGC filters fabricated by EDP etching, HF/Nitric etching [19].



(i) (ii)

Figure 3.2.46: (i) Inductors fabricated on a three-layer 1.2µm-hick membrane [20]. (ii) Fabrication procedure for the micromachined planar elements [20].

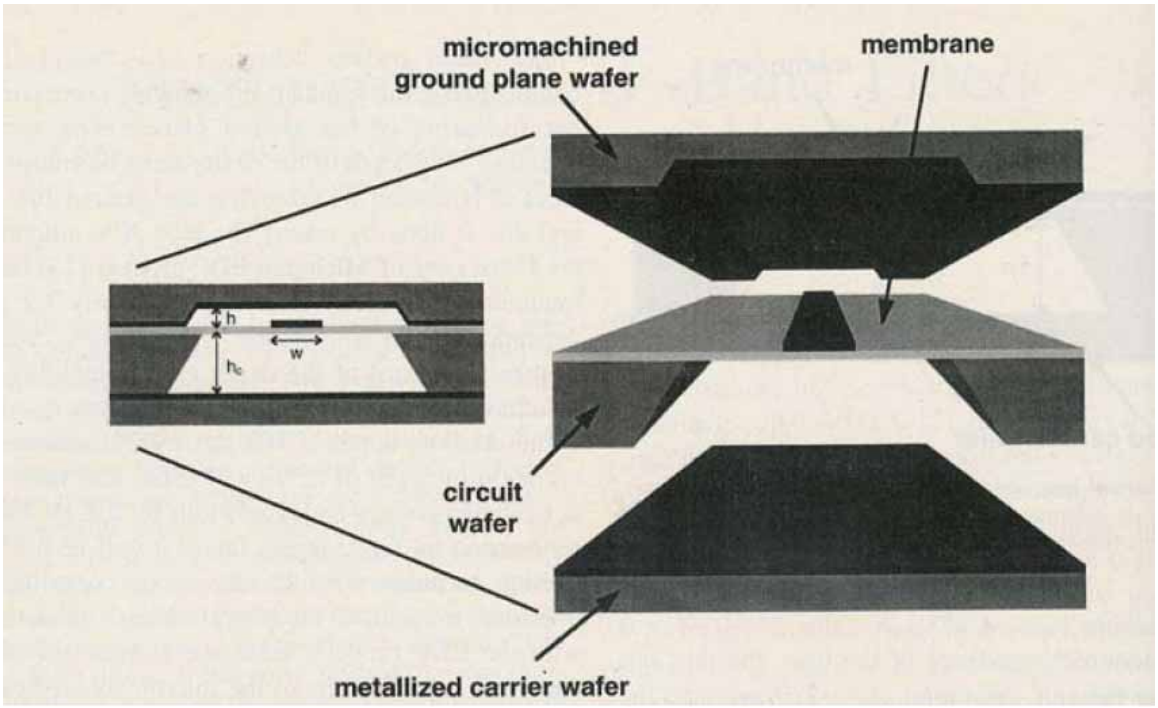


Figure 3.2.47: Micromachined W-band filters [21].

In the antenna field, a plethora of radiating structures with interesting performance have been proposed from millimetre wave to sub-millimetre wave frequencies. Among those, we can quote:

- Integrated antennas with plane (Figure 3.2.48, [22]) or parabolic (Figure 3.2.49, [23]) reflectors, and corner cube antennas [24];
- Integrated horns [25] and arrays (Figure 3.2.50 and Figure 3.2.51, [26]);
- Slot loop antennas built on micromachined membrane Si substrates [27], or integrated with active devices using high resistivity Silicon and bulk micromachining [28];
- Improved characteristics can be obtained using surface micromachining technology and BCB process on Si wafer [29][30];
- Passive patch antennas and arrays fabricated on GaAs or Si substrates ([32] to [35]). Conductive losses in the Silicon lead to poor efficiency, thus requiring the use of high resistivity wafers, which is generally not compatible with standard SiGe bipolar and CMOS processes.

  A solution to these problems is offered by micromachining methods. The lossy Silicon can be removed by back side etching of the substrate (although much less popular, front side etching has been also reported), thereby creating a cavity under the patch, or by depositing a low permittivity, low loss dielectric such as BCB to the top of the wafer and realizing the patch on top of this layer.

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Membrane technology enables to decrease the effective dielectric constant [35] of the substrate, and thus to reduce significantly the surface wave losses and improve the bandwidth. Figure 3.2.48 shows a K-band microstrip patch antenna fabricated on a Silicon membrane obtained by EDP etching. To neglect fringing field effects, the distance separating the edges of the patch and the bulk material should be (at least) equal to twice the substrate thickness. Two examples of aperture-coupled microstrip patch antennas are given in Figure 3.2.49 and Figure 3.2.50. By combining Silicon micromachining techniques and aperture feed, a highly efficient patch antenna can be made by stacking two Silicon substrates on each other [32], [33]. A thick wafer is selected for the upper wafer to obtain good radiation characteristics where a cavity is opened underneath the patch. A thinner wafer is selected for the transmission lines, thus reducing the risk for substrate modes.

The radiation efficiency of printed antennas can also be improved by drilling holes in the host Duroid 6010 medium, as shown in Figure 3.2.51 ([36], [37], [42]); or by synthesizing an Electromagnetic Bandgap (EBG) substrate (Figure 3.2.56) from bulk Si or GaAs materials [38][39]. If the EBG substrate is properly designed (spatial periodicity of the periodic lattice and hole dimensions), substrates modes cannot propagate, which results in a great increase of the antenna efficiency.

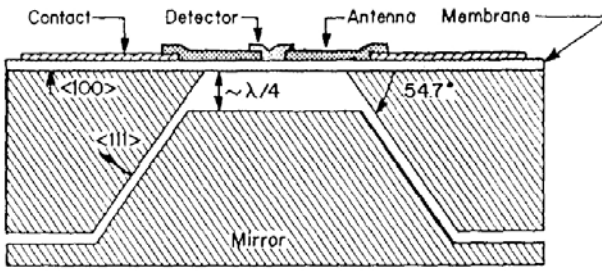


Figure 3.2.48: Integrated Antenna with a plane reflector [22].

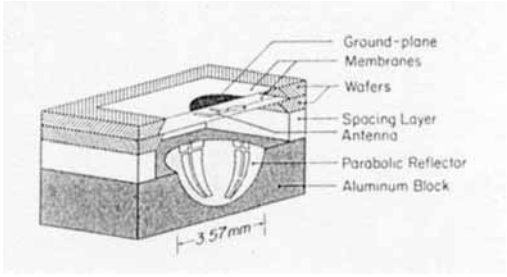


Figure 3.2.49: Integrated Antenna with a parabolic reflector [23].

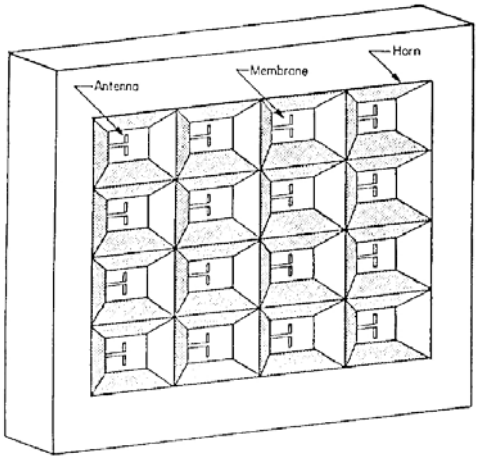


Figure 3.2.50: Monolithic millimetre wave two dimensional horn imaging arrays [26].

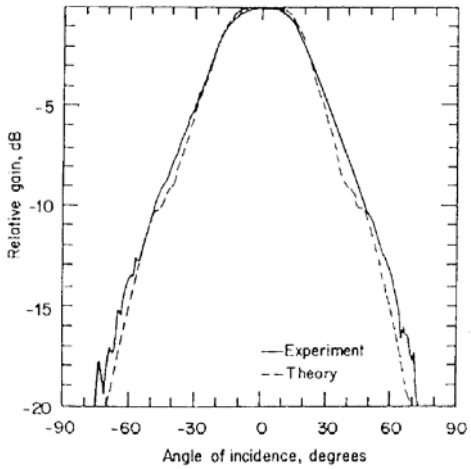


Figure 3.2.51: Measured and computed H-plane of the 9×9 integrated horn array [26].

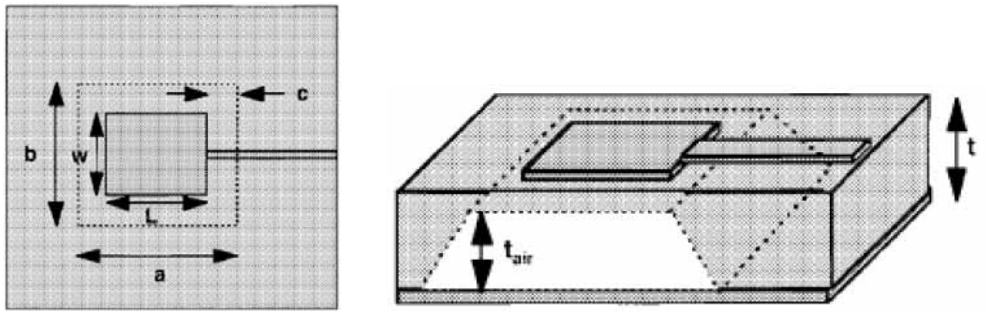


Figure 3.2.52: Micromachined rectangular microstrip patch antennas. The silicon material is removed laterally underneath the patch antenna to produce a cavity that consists of a mixture of air and substrate with equal or unequal thicknesses [35].

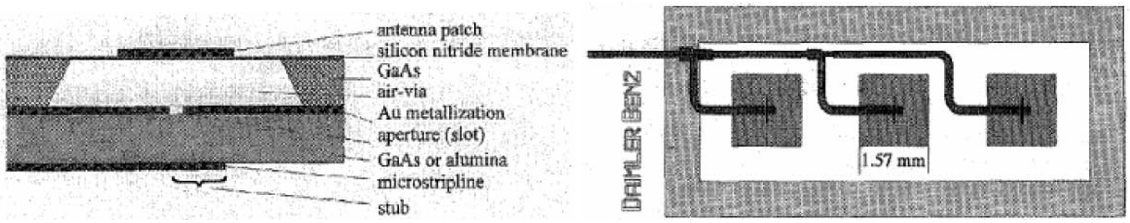
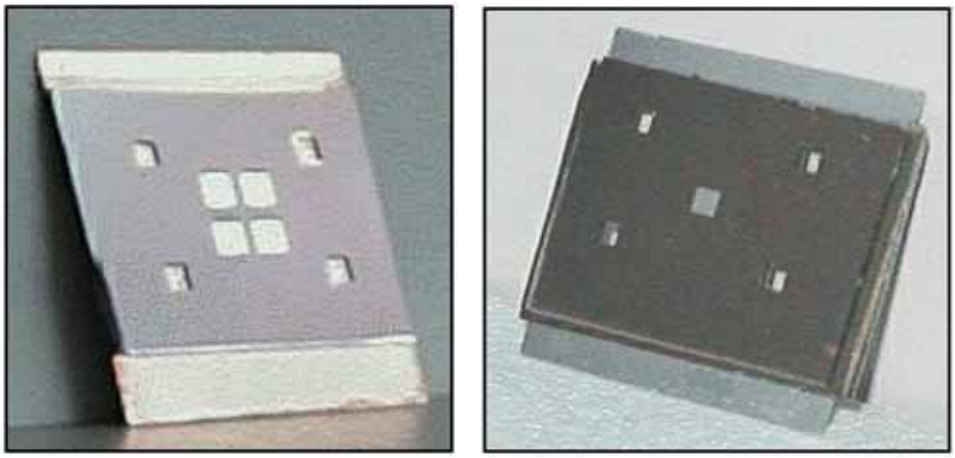


Figure 3.2.53: Planar millimetre wave antennas using SiN_x-membranes on GaAs substrate.



(ii) (ii)

Figure 3.2.54: (i) Aperture-coupled microstrip patch antenna operating at 58 GHz [32]. (ii) Aperture-coupled stacked patch antenna at 60 GHz [32].

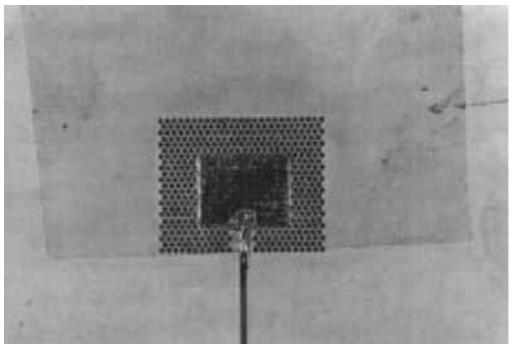


Figure 3.2.55: Fabricated microstrip antenna (0.70×0.92 cm) on a localized low-ε_r dielectric (ε_r=2.3) with a hole region of 1.3×1.6 cm. The substrate is a Duroid 6010 ε_r=10.8; h=0.635 mm [36].

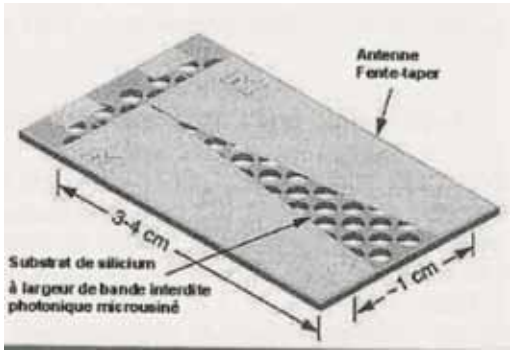


Figure 3.2.56: Tapered slot antenna on micromachined dielectric substrate [38], [39].

3.2.4.6 Results obtained at IETR

A conventional process of membrane-supported multilayer structures has been developed at IETR [32]. The main technological steps are summarized in Figure 3.2.57.

- a Fabrication of a dual-layer dielectric membrane SiO_2/Si_3N_4 (0.67µm/1µm) on a double-side polished high-resistivity (ρ>450Ω.cm) <100> Silicon substrate (h_2=200µm, $\varepsilon_{r,2}$=11.7),
- b Anisotropic KOH etching of the Si substrate along its <111> planes (see also Figure 3.2.58),
- c, d Evaporation of aluminium thin films (1.3µm) and chemical etching,
- e Wafer bonding.

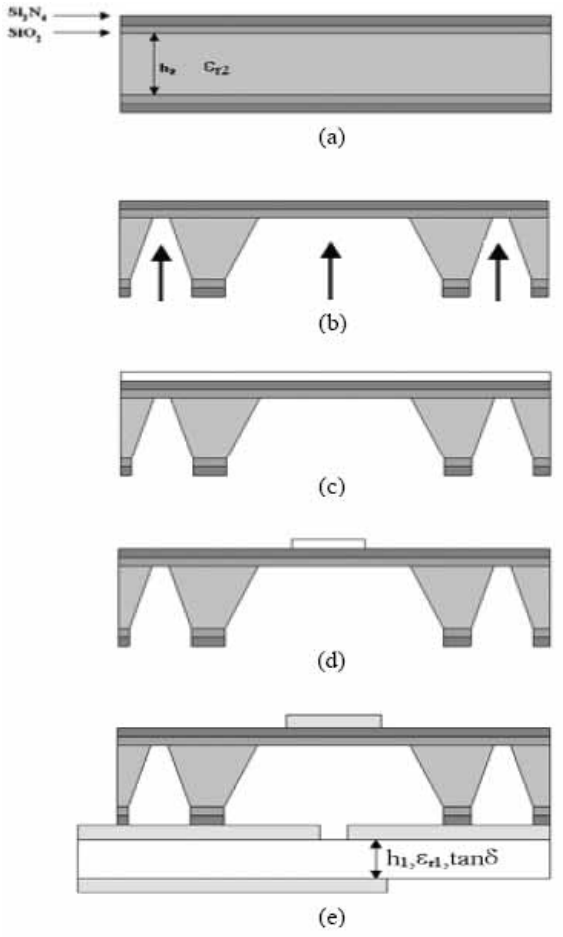


Figure 3.2.57: Main technological steps for the fabrication of micromachined aperture-coupled patch antennas [32].

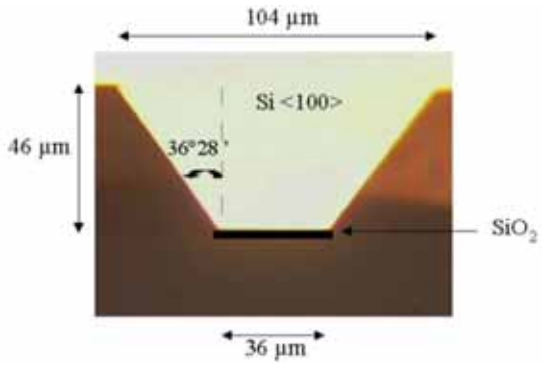


Figure 3.2.58: Cavity walls of an etched <100> substrate.

This process has been successfully implemented for the fabrication of aperture-coupled patch antennas and arrays (Figure 3.2.59), as well as stacked patch antennas (Figure 3.2.60).

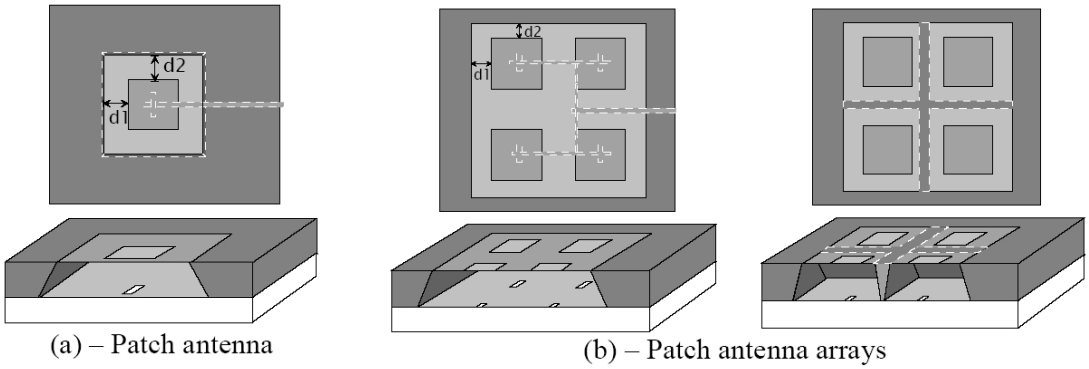


Figure 3.2.59: Examples of micromachined antennas [32].

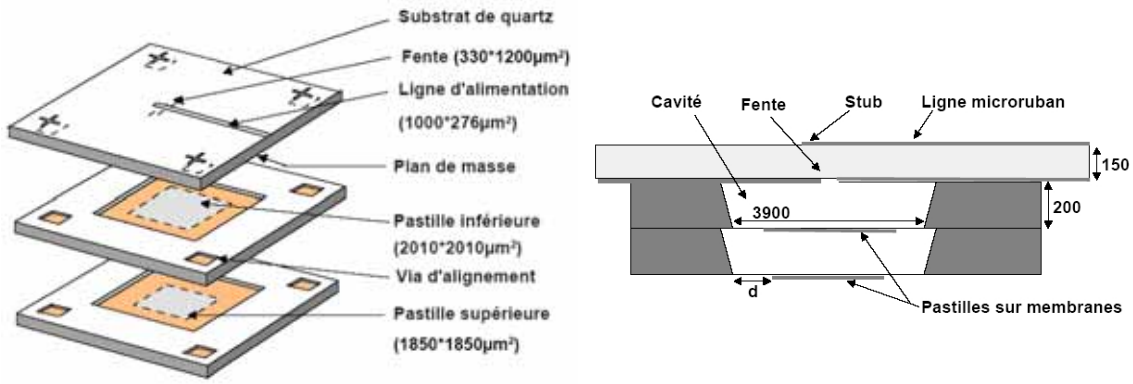


Figure 3.2.60: Stacked aperture-coupled micromachined patch antennas [32].

3.2.4.7 Low loss front-end on micromachined silicon at Alcatel

Reflectors with active focal arrays are solutions for satellite antennas in multimedia telecommunications systems. An issue is the integration of the focal array made of horns connected to the following equipment:

- Transition Wave guide to microstrip;
- Filtering;
- Redundancy switches;
- Low Noise Amplifiers.

The compactness of an active feed may be achieved by a monolithic integration approach of these equipements. By limiting the lengths of interconnections between the radiating element and the LNA, the overall G/T of the antenna is improved.

An innovative feed is being developed in the frame of a research project funded by the French Industry Ministry, and involving Alcatel Space, LAAS, MEMSCAP and IRCOM. It has the following features:

- the Low Noise Amplifier is flip-chip mounted on a Silicon module;
- in order to decrease the dielectric losses generated by the high resistivity Silicon, the Silicon material is micromachined on its area hosting the transmission lines and the filtering sections;
- the redundancy switch is achieved by MEMS switches deposed on the membrane.

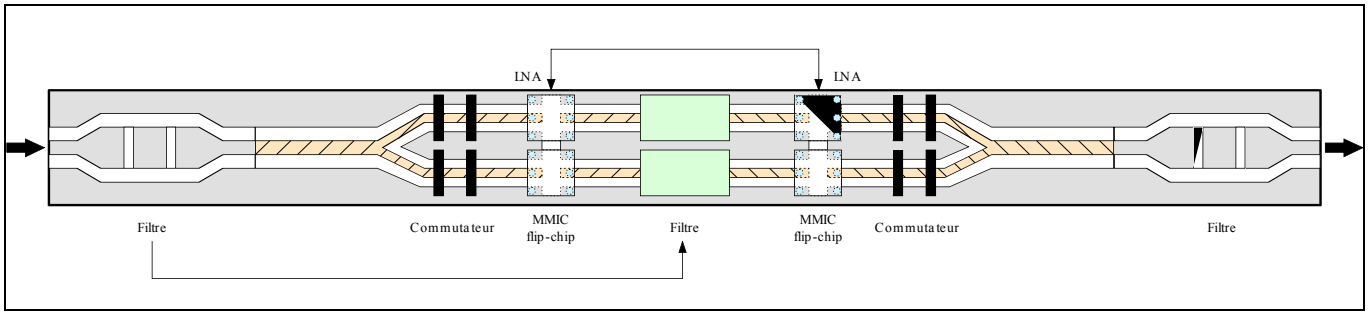


Figure 3.2.61: monolithic integration of a redudanced LNA module.

Filters using the technology on membrane allow the advantages of both planar and waveguide technologies. Indeed, as the figure shows below, micromachined filters combine simultaneously the miniaturization, the reduced production costs and high quality factors. This type of filter applies perfectly to the constraints of the integrated feeds for high frequencies (Ka band and beyond).

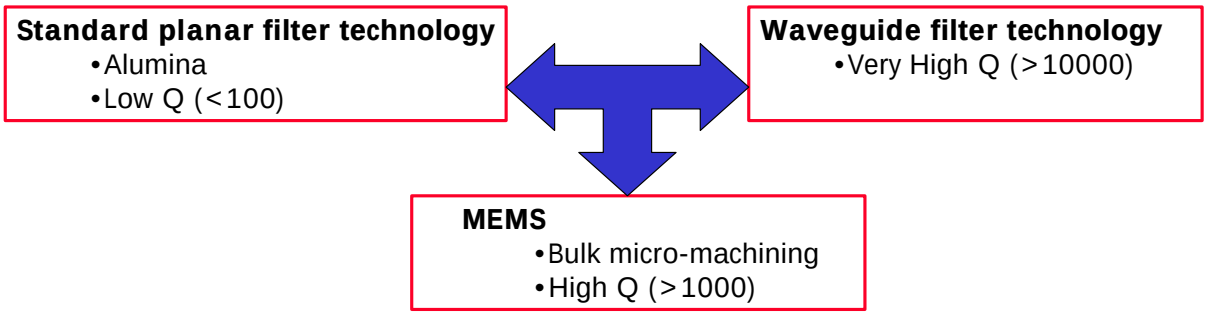


Figure 3.2.62: Principle of filters on membrane compared with the existing technologies.

It is also now well known that RF MEMS switches have better electrical performance than traditional switches, based for instance on PIN diodes. This is due to better intrinsic performance of the part: comparative measurements made at Alcatel show Ron / Coff 1.7 Ω / 10 fF for MEMS instead of 5 Ω / 22 fF for PIN diodes.

Nevertheless, the use the technology of membrane is not directly compatible with standard assembly process: gluing or flip chip by thermal compression, because membranes are very sensitive to temperature effects. For the time being, the only solution is to assembly the MMIC on massive silicon, which implies electrical transition and matching between membrane and massive silicon. The loss of this transition can delete all the gains brought by the use of membrane for switches and filters. Moreover, in spite of this care, membranes may be damaged by temperature.

It can therefore be stated that the success of MEMS technology, especially using membranes, is closely linked to improvements on packaging and assembly technology. Low temperature assembly process is necessary and remains to be developed.

3.2.5 Gallium-Arsenide Micromachining

3.2.5.1 Overview

With the recent advances in semiconductor technology and micromachining techniques the number of application fields for MEMS has been growing, extending from well-known electromechanical systems such as integrated accelerometers and pressure sensors to the so-called bio-MEMS [43]-[45]. Research on MEMS has become a large area of activity for the development of new types of devices conferring more functionality to conventional electronic circuits. All these efforts have been boosted by factors such as the growing demand for speed and capacity in data transmission and a constant need for a better interaction with our environment. In this connection, concepts of smart or intelligent systems, as well as "system on a chip" for complex combinations of sensors, actuators and microcontrollers on a single chip, have emerged [46]. The use of semiconductor technology has been a key feature as it provides the possibility to implement different sensing and actuation functions by using IC processing techniques. Here, the benefits are multiple and include advantages such as miniaturisation, low cost through volume production, low weight and power consumption, increased performance and reliability. From the material point of view, silicon has often been the material of choice due to the mature processing technology and the reduced cost. But as in electronic applications Si has also shown his limits for the development of microwave, optoelectronic as well as high-temperature devices [47]. To overcome this, new material systems and device concepts such as MESFET, HEMT, resonant tunnelling diodes and semiconductor lasers have been developed [48]-[50]. III-V compound semiconductors have emerged offering the possibility of bandgap engineering or the epitaxial growth of heterostructures with defined potential profiles and specific transport properties (Figure 3.2.63) [51]. In addition, III-V compound semiconductors possess a number of physical material properties that can be used to implement classical sensing functions with higher sensitivities and extend the operation range of MEMS to RF and optical communication [52]-[53].

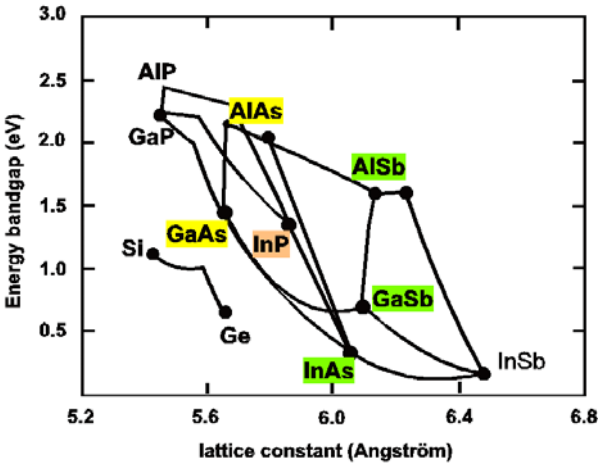


Figure 3.2.63: III-V compound semiconductors. Ternary and quaternary materials are obtained by combining different binary compounds. The material composition can be tuned for lattice-matched heterostructures as well as the definition of physical properties of interest.

Gallium arsenide (GaAs) is an important compound semiconductor that is widely used in high-speed and high-temperature components and optoelectronic devices. At the same time, GaAs is a very interesting semiconductor that has piezoelectric properties for force and resonant sensors [54][55], high Seebeck coefficients for infrared thermopile sensors [56], and a wide energy gap of the conduction and valence bands for high-temperature sensors [57]. GaAs is also very interesting for applications in radiofrequency (RF) and optical microelectromechanical systems (MEMS) devices [58].

3.2.5.2 Micromachining Techniques

3.2.5.2.1 Dry Etching

Dry etching is the removal of material, typically a masked pattern of semiconductor material, by exposing the material to a bombardment of ions that dislodge portions of the material from the exposed surface. Unlike with many of the wet chemical etchants used in wet etching, the dry etching process typically etches directionally or anisotropically. Dry etching is used in conjunction with photolithographic techniques to attack certain areas of a semiconductor surface in order to form recesses in material, such as contact holes (which are contacts to the underlying semiconductor substrate) or via holes (which are holes that are formed to provide an interconnect path between conductive layers in the layered semiconductor device) or to otherwise remove portions of semiconductor layers where predominantly vertical sides are desired.

3.2.5.2.2 Wet Etching

Wet etching is the removal of material by immersing the wafer in a liquid bath of chemical etchant. Wet etching is also used in conjunction with photolithographic techniques to attack certain areas of a semiconductor surface. There are two kinds of wet etching etchants, isotropic etchants and anisotropic etchants:

- Isotropic etchants attack the material being etched at the same rate in all directions;
- Anisotropic etchants attack the wafer ate different rates in different directions.

3.2.5.3 III-V compound material properties for MEMS

For standard functions like pressure or acceleration sensing, piezoresistance or piezoelectricity in III-V compound semiconductors and heterostructures can be used [59]. The latter, which is a dynamic effect and an elegant possibility to implement actuation functions in MEMS, is not available in Silicon. It allows the realisation of on-chip III-V compound based high-Q piezoelectric resonators for clocks and filters [60]. A static piezoelectric response can be obtained in III-V compound heterostructures and devices, where materials with different piezoelectric coefficients are combined [61]. Materials such as AlGaAs, AlSb, with high energy bandgap can be used for device operation at high temperatures without the need of additional technology such as SOI. The bandgap engineering not only allows tailoring electronic properties of heterostructures; but materials with high thermal resistivity, such as AlGaAs and InGaAs, can also be obtained. As will be shown later, thermal isolation is needed to increase the sensitivity of thermoelectrical MEMS. In the field of RF and optical MEMS, GaAs or InP-based microsystems present, in comparison to the silicon CMOS process, the advantage of monolithic integration with MMICs on the basis of the same material system. This avoids the use of hybrid systems where inserted matching components can lead to reduced bandwidth and increased losses.

Materials with direct and indirect bandgap are also available for optoelectronic applications. Ternary and quaternary compounds on the basis of GaAs, AlAs and InP can be engineered to implement optical functions for different wavelength regions. Micro-opto-electromechanical systems (MOEMS), involving the micromachining of actuated superlattice-based mirrors can be implemented [62]. An interesting consequence of the bandgap engineering with III-V compound semiconductors has been the appearance of quantum effects due to carrier confinement [63]. The increased functionality of quantum electronic devices can be combined with these material properties for the development of miniaturised MEMS with new opportunities for sensing and signal processing functions [64], [65].

3.2.5.3.1 Membrane technology with III-V compound heterostructures

Most of mechanical, thermal and optical functions are usually introduced in MEMS by means of microfabricated thin structures in form of cantilever, bridges and closed or suspended membranes. These mechanisms, which are used for sensing as well as actuating functions, are generally made of semiconducting materials, dielectrics or thin metals. Technologies based on high-aspect-ratio micromachining or other microfabrication techniques such as LIGA allow one to introduce classical mechanical functions involving structures such as microgears, lever systems as well as optical functions [66]. MEMS devices including membrane structures can be found in applications such as pressure sensing, microfluidic, thermal sensors, microwave and optical communication [67], [68].

Micromachining is the technology used in semiconductors MEMS to release these structures. This includes standard IC processes like lithography, etching and material deposition. Depending on the application surface or bulk micromachining can be used for the fabrication of the membrane. While the first method is based on the possibility to remove so-called sacrificial layers the second one use a stop layer technique [69], [70]. The sacrificial layer can be photoresist, a dielectric material, an ion- implanted region or an epitaxially grown layer. One or another system can be used depending on the thickness of the structures and other parameters related to the application. The etch stop technique allows the realisation of volume micromachining in the sense that large parts of the substrate can be selectively etched against a thin layer, which then plays the role of membrane. Here the etch stop layer can be an epitaxial layer, a dielectric material or an ion-implanted region. A big advantage of compound semiconductors lies in the fact that epitaxially-grown layers can be used as etch stop or sacrificial layers. This is due to the possibility of selective etching and adds more precision to the micromachining. The GaAs substrate can selectively be etched against AlGaAs, InGaP, GaSb or AlSb. The thickness control of the epitaxially-grown sacrificial layers provide the possibility of etching air gaps with defined thickness for applications in capacitive actuation or in optical MEMS.

The work here includes the definition of controllable and selective etching techniques for the fabrication of membrane structures. The so-obtained micromechanical structures can, as will be demonstrated, play different roles in a variety of MEMS devices. They can, in a classical way, be used to carry stress or pressure sensitive elements and as mechanical amplifiers or transformers to translate differential pressure or force into a surface stress which is then sensed by the strain-sensitive elements. A sample of surface and bulk-micromachined III-V membrane structures is shown in Figure 3.2.64. The best-known example is that of micromachined piezoresistive pressure and acceleration sensors. Thin suspended or closed membranes are also needed in thermal sensors such as infrared bolometers and gas flow sensors where thermally-isolated regions are required to increase the efficiency [71], [72].

Here again the bandgap engineering of compound heterostructures is of great advantage. Silicon nitride or dioxide are not the only material for membranes, the material composition of chosen semiconductor layers can be, so defined that they provide high thermal-resistance path between the centre of the membrane and the rest of the bulk.

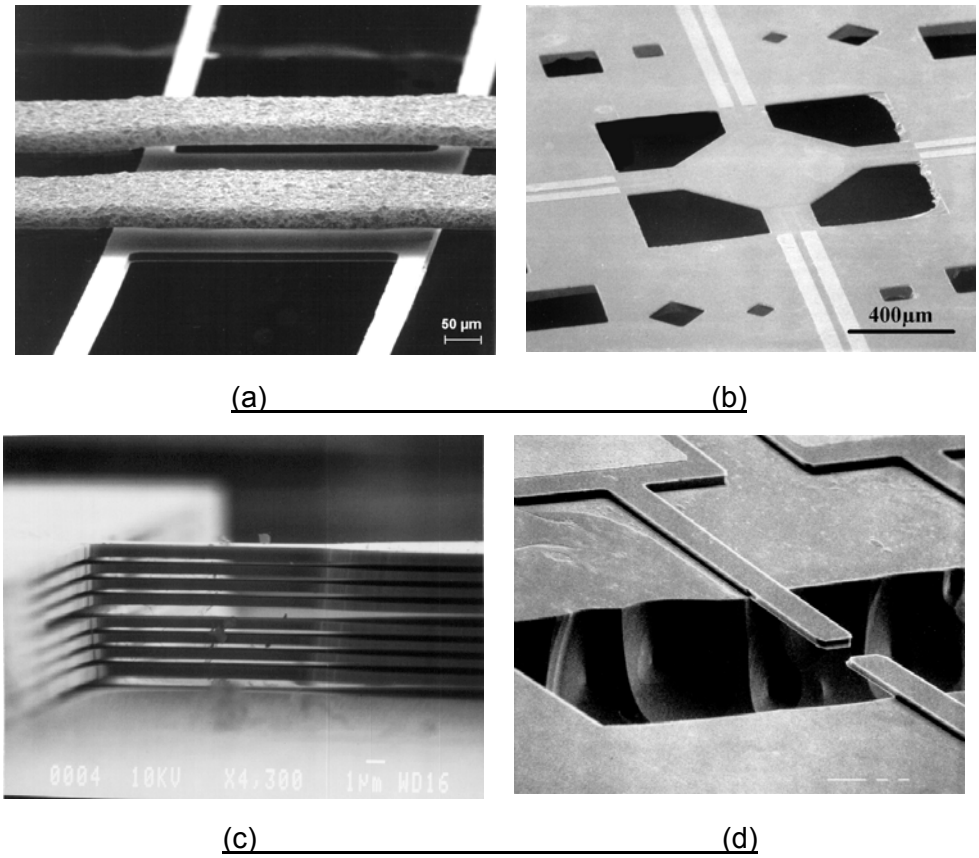


Figure 3.2.64: Example of compound semiconductor membrane and cantilever structures. (a) Suspended InP-based thin membrane with gold airbridge structure (b) and integrated resistors for electrostatic and thermal actuation, respectively. (c) Surface micromachined InP-based cavity structure with airgaps [32]. (d) Bulk-micromachined GaAs cantilevers for field-emitter wedge structures. InGaP is used here as etch stop layer [33].

The discussed features have been combined with other physical material properties of compound semiconductors to develop microsensors for gas flow, microwave power measurement as well as filters for optical communication. The fabrication technology of these sensor groups will be presented in the following sections.

3.2.5.3.2 Thermoelectrical GAAS/ALGAAS Sensors

This is a type of MEMS where thermal, electrical and etching properties of GaAs/AlGaAs heterostructures are combined. The GaAs/AlGaAs material system is characterised by a strong Seebeck effect and the possibility to tailor the thermal conductivity of AlGaAs through the variation of the Al mole content in AlGaAs [75][76]. This is also possible for the InGaAs/InP material system. Key functions are related to the creation of temperature gradients and the way to measure them. Depending on the application the temperature gradient between the center of a thin membrane structure and the rest of the bulk can, for example, be created by a dc current flow in an integrated metal or semiconducting resistor on the membrane. The heating of the center of the membrane can also be achieved with infrared radiation on a thin absorbing layer on the membrane or by the absorption of rf power in a terminating load or the dissipation of in a transmission line integrated on the membrane [77][78]. In this connection, $Al_{0.48}Ga_{0.52}As$ or $In_{0.53}Ga_{0.47}As$ are the materials of choice for membranes on GaAs and InP substrates, respectively then they provide maximum thermal resistance. The temperature difference is sensed by series of thermocouples with hot ends on the membrane and the cold ones on the bulk.

3.2.5.3.2.1 Gas flow sensors

An example of application-specific flow sensors on the basis of GaAs/AlGaAs material system is presented here. The heating of the membrane is realised, as explained, with a dc current flow in a Cr/Au resistor. The application is aimed at analysing the flow in the air gap (about 1mm) between the rotor blades and the stator of an axial compressor.

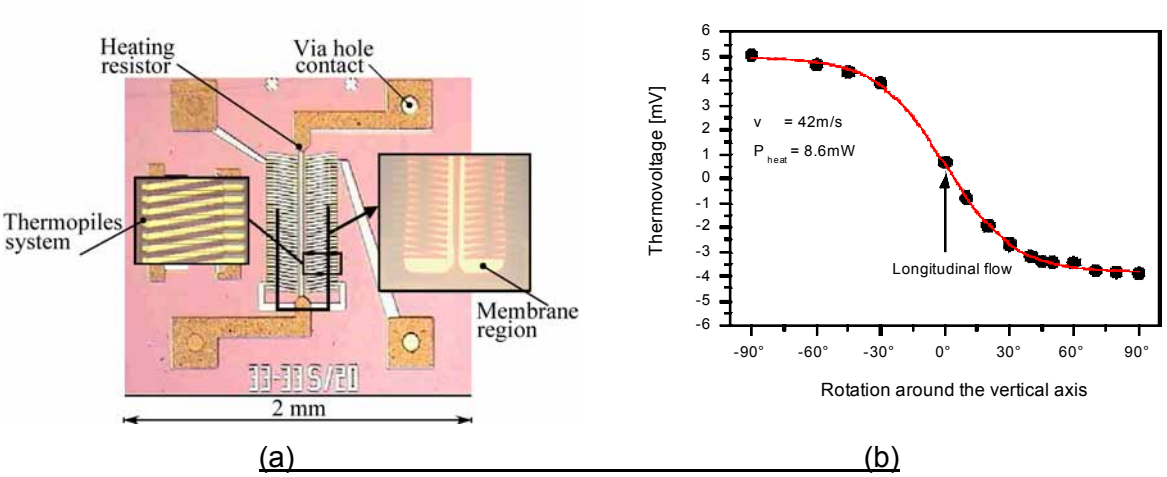


Figure 3.2.65: GaAs/AlGaAs membrane sensor for gas flow measurement. (a) Top view of the sensor chip with the central heating resistor and the series of GaAs/CrAu thermocouples for the measurement of the temperature gradient between the center of the membrane and the bulk of the chip. In the inset (right) the 2μm thick membrane region is illuminated from the backside. (b) Flow direction dependence of the sensor. The output thermovoltage is delivered by the voltage difference between the thermopiles left and right to the heating resistor.

To determine the flow velocity and direction, two series of integrated thermocouples measure the cooling down of a heating resistor (Figure 3.2.65a). The thin membrane (2 μm thick) provides a highly resistive path to the heat flow from the center of the membrane to the bulk of the chip. This results in high temperature gradients. For the thermocouples a combination of n-doped GaAs mesa and Cr/Au is used. Note here that the wafer structure is MESFET-compatible and the channel layer can be used for the mesa structures. A typical sensor response is shown in Figure 3.2.65b for measurements in a wind channel and rotation of the sensor. Additional technology steps have been involved in order to insure a reliable packaging for the sensor (Figure 3.2.66). These include the etching of via-holes, which provide the ideal means to realise electrical connections without disturbing the flow. Such an implementation is made easier due to the semi insulating nature of the GaAs substrate for which no isolation layer is needed between the gold metallisation and the substrate. A self-aligning scheme of the 150 micron chip is obtained by using solder bumps.

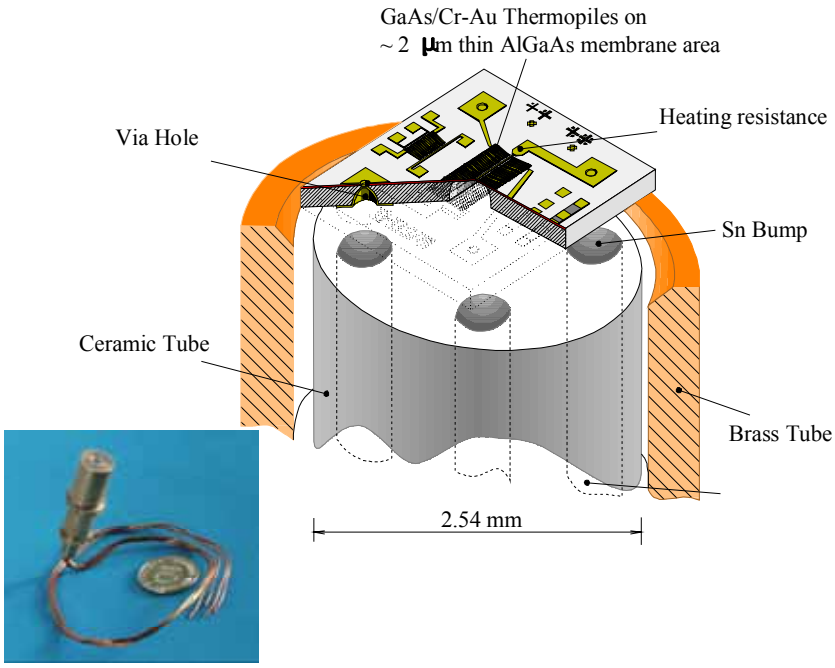


Figure 3.2.66: The sensor chip mounting is realised with via-hole technology and solder bumps technique to ensure a self-adjusting effect of the chip. An important parameter for a reliable operation is the burnout power of the heating resistor.

3.2.5.3.2.2 Microwave and millimetre-wave power sensors

The described sensing scheme can be used for MMIC-compatible thermal sensors for the measurement of power at microwave and millimeter-wave frequencies. The heating can be provided by the conversion of RF power into heat.

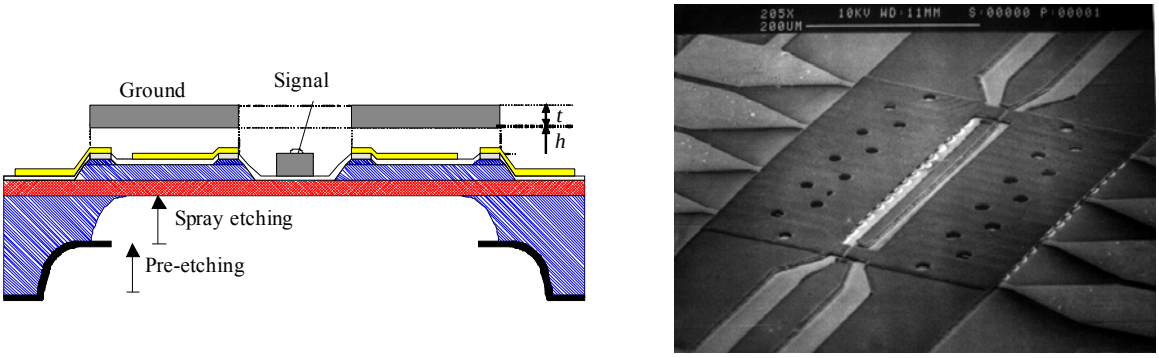


Figure 3.2.67: Micromachined GaAs sensor using the losses in the central conductor of a coplanar waveguide. The ground electrode is lifted above (air bridge structure) the membrane in order to avoid losses due to additional metal on the membrane [38].

This can take place in a matched resistive termination or through conduction losses in a matched transmission line structure. GaAs/CrAu thermocouples are also used to measure the temperature. Such a sensing scheme has the advantage of providing a dc output-voltage, which is an accurate measurement of the true rms power. The employed thermal sensing method allows for operation over a wide dynamic range with high linearity. This is a big advantage of thermal sensing, compared to diodes detectors, rms-to-dc converters and log-amplifiers, for modern telecommunication applications where complex modulation signals such as TDMA and CDMA are used.

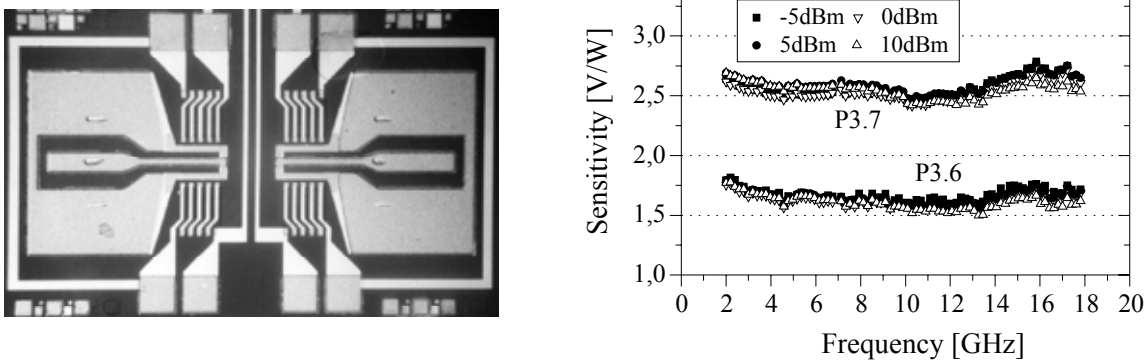


Figure 3.2.68: Microwave power sensor in 50 Ω termination structure. The sensor response shows a constant sensitivity on a frequency range of up to 18 GHz. The termination, which lies on a thin membrane, is a parallel combination of two 100 Ω NiCr resistors [80].

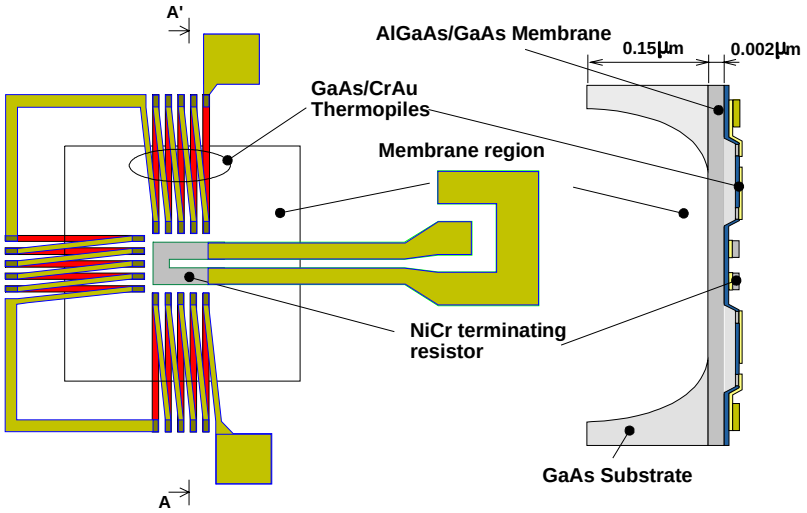


Figure 3.2.69: Sensor structure for a 60 GHz operation frequency. Additional segments have been introduced to form a GSG electrode configuration for on-wafer measurements. Reliability aspects are essentially related to the burnout of the NiCr resistor. This could happen at dc input power above 55 mW for a 126 Ω terminating resistor.

The flexibility of micromachining also provides the possibility of further optimisation in order to decrease the time constant which is typically around 1ms. Figure 3.2.67shows the realisation of a microwave sensor in a through-configuration in a coplanar waveguide technology.

The ground conductor is lifted above the membrane in form of an airbridge in order to minimise thermal losses. Depending on the frequency range the sensor design includes the definition of transmission lines, matching networks and terminating resistor. Here the transition bulk-membrane and the influence of the etch profile should be taken into account. The response of a terminating 50 Ω sensor shows a constant sensitivity for frequencies up to 18GHz (Figure 3.2.68). For higher frequencies the structure dimensions are attractive for the integration of further components such as antennas to which the terminating resistor should be matched [81]. Figure 3.2.69shows the schematics of such a sensor structure for an operation frequency of 60 GHz. A constant sensitivity of about 12 mV/mW is obtained for the frequency range up to 80 GHz (Figure 3.2.70).

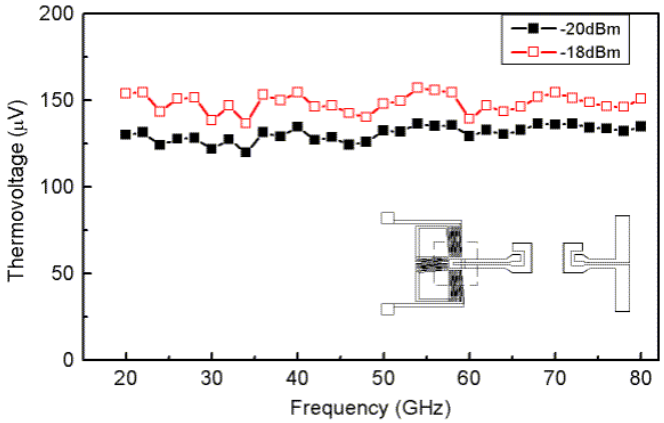


Figure 3.2.70: Sensor response with a constant sensitivity of around 12 mV/mW for the frequency range up to 80 GHz. The noise equivalent power for the 20 kΩ thermopiles correspond to a signal-to-noise ratio of 7.1×10^8 V/W.

With increasing frequencies the available small powers put more constraints on noise figure and sensitivities. The number of thermoelements and their proximity to the terminating resistor are important for sensor characteristics such as the noise equivalent power and the sensitivity. Higher thermocouple voltages can be obtained with lightly-doped GaAs or AlGaAs-based mesa but this happens at the cost of signal-to-noise ratio due to higher thermocouple resistance [82].

3.2.5.3.3 Optical filters

The requirement for increased bandwidth and transmission data capacity in existing and next-generation optical communication systems can be fulfilled by the use of the dense wavelength division multiplexing (DWDM) technology [68]. Filters belong to the building blocks of these communication systems where also the dynamic allocation of channels at the receiving or transmitting unit is needed. In this network architecture, tuneable Fabry-Pérot (FP) filters can be used for wavelength-selective detection of the connected channels. Here, III-V compound micromachining technology offers the possibility to integrate movable opto-mechanical and surface active optoelectronic components on the same chip [73][83][83]. III-V compound heterostructure-based mirrors are the main components of micromachined Fabry-Pérot filters, where highly reflective InGaAs/InAlAs Bragg mirrors are used (Figure 3.2.71).

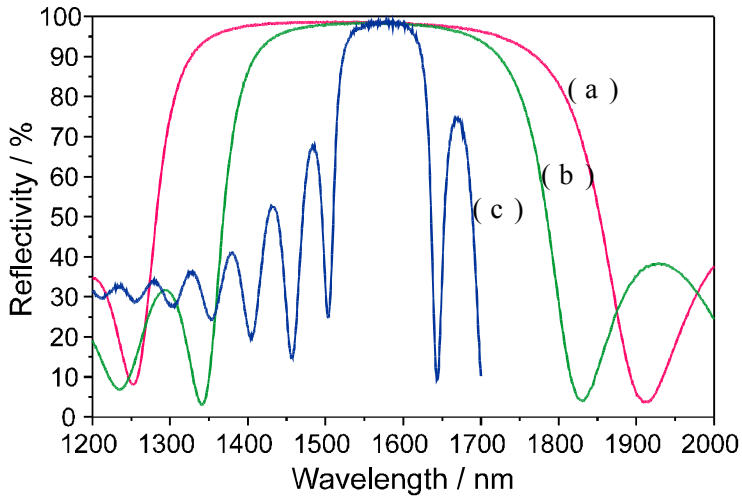


Figure 3.2.71: Spectral characteristics of Bragg mirrors for Fabry-Pérot filters. (a) 5.5 period TiO_2/SiO_2, (b) 7.5 period SiN_x/SiO_2, (c) 20.5 period InGaAs/InAlAs [80].

The tunability of the FP filter can be obtained by the variation of the resonator cavity length. The movable mirror can be electrostatically or thermally actuated. The definition of the mirror structure and characteristics as well as the cavity length is based on the requirements of wide tuning range, low insertion loss and low polarisation dependence. Schematics of three basic structures for FP filters are shown in Figure 3.2.72.

In concepts based on short cavity length, as developed with surface micromachining (Figure 3.2.72a), high-quality mirrors are required to achieve sufficient selectivity and crosstalk suppression. The device design of Figure 3.2.72b uses dielectric mirrors (e.g. TiO_2/SiO_2) with the curvature of the upper mirror achieving a stable spherical cavity. In the first case, the complete structure can be grown in one step but additional diffraction and the difficulty of fitting the curvature of the mirror to the phase front of the incident light results in increased losses due to diffraction and transverse modes in the cavity. For the two-chip concept detailed here (Figure 3.2.72c), epitaxial InAlGaAs/InAlAs superlattice structures (Bragg reflectors) are used as mirrors [87]. The movable one, in form of a suspended membrane, is released by selectively etching the InP substrate against the InAlGaAs/InAlAs heterostructure. The cavity length is defined by bar spacers and lies around 25 μm. This leads to more relaxed requirements on mirror reflectivity.

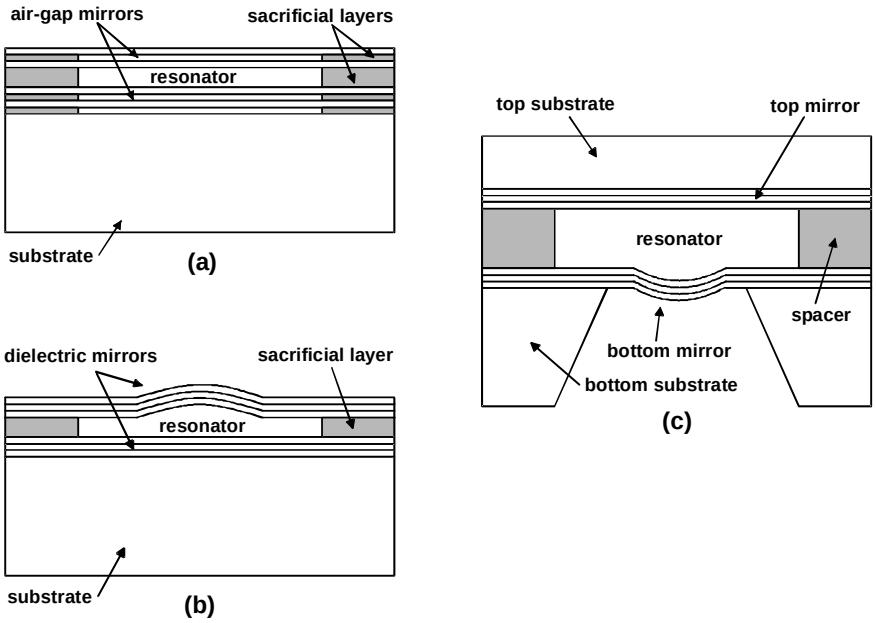
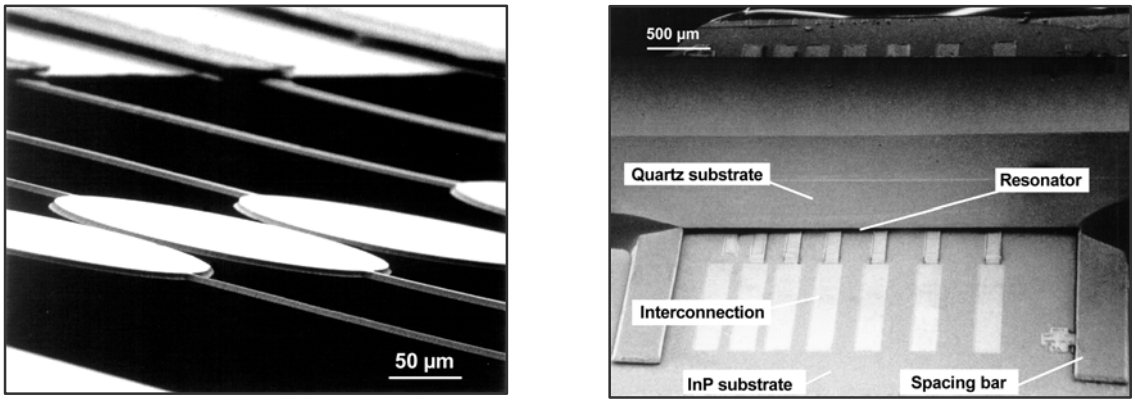


Figure 3.2.72: Schematics of micromachined FP filter design. (a) surface micromachined short-cavity resonator [86], (b) with dielectric mirrors and (c) two-chip long-cavity bulk-micromachined.



(a) (b)

Figure 3.2.73: Fabry-Perot filter with thermally actuated Bragg mirror. (a) The flexible suspension beams of the mirror structure provide uniform displacement of the mirror center.

The tuning of the filter, due to the variation of the cavity length, can be obtained by capacitive or thermal actuation. Suspended Bragg mirrors before the mounting of the complete two-chip FP filter are shown in Figure 3.2.73. A direct current flow in the membrane structure is used for the thermal actuation. Tuning characteristics of assembled filters (Figure 3.2.73b) with 250 μm diameter are shown inFigure 3.2.73, with typical FWHM of 0.13 nm, insertion loss at resonance wavelength of 1.1 dB. A sensitivity of 53 nm/mW is obtained over a spectral range of 30 nm. This technology is suitable for wavelength division multiplexing (WDM) around 1.55 mm and can be extended to related detectors and light sources.

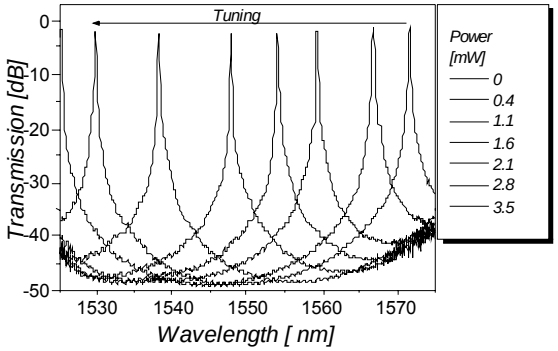


Figure 3.2.74: Spectral response of a thermally actuated filter. The contrast between minimum and maximum transmission exceeds 40 dB.

3.2.5.4 Photoelctrochemical etching of semiconductors

Photoelectrochemical (PEC) etching of III-V semiconductors has been used to fabricate unique structures in electronic and photonic devices, such as integral lenses on light-emitting diodes, gratings on laser structures, and through-wafer via connections in field-effect transistors. The advantages and characteristics of PEC etching are reviewed, and the extension of this processing technique to silicon is addressed. Three-dimensional structures are of great interest in silicon for electronic and micromechanical devices. Silicon is a challenging material to PEC-etch because the oxides formed during etching inhibit the dissolution rate and decrease the spatial resolution. In addition, the long carrier lifetime permits holes to react at unilluminated sites. Nonaqueous solvents provide a processing environment where oxides do not interfere with the spatial resolution and free fluoride is no longer needed in the dissolution of silicon [88].

The electrochemistry of semiconductors has played an important role in the development of integrated circuit (IC) technology. Many of the processes used in IC manufacturing are based on electrochemical principles, and electrochemistry is the foundation for understanding the basic mechanisms of etching, deposition, and corrosion.

One area that is of particular interest is the photoelectrochemical (PEC) etching of semiconductors. PEC etching is a topic encompassing light-induced electrochemical reactions of semiconductors in contact with liquids. The light-induced creation of minority carriers in semiconductors can stimulate spatially-selective or materials-selective etching and deposition reactions.

Much of the PEC etching to date has been focused on III-V semiconductors because of the need for optical components in III-V-based lightwave systems and the ease of PEC processing due to the solubility of the reaction products (e.g., oxides). There is currently considerable interest in PEC etching of silicon for microelectromechanical systems (MEMS) and three- dimensional features for silicon ICs (e.g., trench capacitors).

Figure 3.2.75: Energy-band structure of an n-type semiconductor in contact with an electrolyte.

3.2.5.4.1 Basic Principles

The semiconductor-electrolyte interface has been discussed in detail [89]-[95]. In PEC processing, the semiconductor is immersed in a conductive electrolyte, and electrical contact is made to the semiconductor. The semiconductor is biased with respect to a counter electrode, and the potential is measured versus a reference electrode. When the Fermi level of the semiconductor at the semiconductor-electrolyte interface is within the band gap, the density of carriers in the semiconductor is usually less than the density of carriers (ions) in the electrolyte, so that a majority of the potential difference across the interface occurs within the semiconductor. Figure 3.2.75 shows the case of an n-type semiconductor in contact with an electrolyte.

3.2.5.4.2 Properties of PEC etChing

The following useful properties of PEC etching can be understood from the above brief description:

- *Light-intensity dependence:* The rate of etching depends on the rate of minority-carrier photogeneration, and, in many cases, a linear relationship exists between the etch rate and the light intensity;
- *Spatial selectivity:* By spatial modulation of the light intensity, or by providing physical masking, one can "anisotropically" etch semiconductors, forming three-dimensional structures. The spatial resolution, which is discussed for specific cases, is dependent on the semiconductor transport and lifetime properties and on the rate of the chemical reactions;
- *Band-gap selectivity:* On structures having materials with different band gaps, the narrower-gap materials can be selectivity-etched by using light with a spectrum that is absorbed by the narrower-gap materials but not the wider ones;
- *Dopant-type selectivity:* Samples can be biased so that n-type materials are etched but not p-type materials. Alternatively, p-type materials can be isotropically etched in preference to n-type materials. In a more complex scheme, p-type materials can be photoetched [95][96];
- *Band-position selectivity:* Shifts in the conduction or valence bands can sometimes be used to selectively etch a particular composition by choice of the electrical bias;
- *Etch-rate monitoring:* When an electrical connection to the sample is made, the etch rate and amount of material removed can be monitored by measuring the current flow in the external circuit;
- *Process and mechanistic definition:* Photoelectrochemical studies can often be very useful in designing chemical processes or optimizing existing ones, because one can directly measure the rate of the individual reactions that make up complex processes, such as electroless processes.

3.2.5.4.3 Experimental Procedures

In PEC experiments, the semiconductor sample is immersed in an electrolyte in a cell that contains an optical window to allow it to be illuminated. Electrical contact is made to the semiconductor. A potential is applied between the semiconductor electrode and a counter electrode (e.g., a piece of platinum) immersed in the same electrolyte. The potential of the semiconductor is measured versus a reference electrode, such as a saturated calomel electrode (SCE), as used in these studies. In this way, the current flowing between the semiconductor and the counter electrode can be recorded as a function of the potential versus the reference electrode. In nonaqueous studies, care must be taken in the proper selection of materials to prevent corrosion. Additional details on the materials used in construction of cells and equipment used in scale-up of processes can be found in the literature (for example, [98][99]).

3.2.5.4.4 Surface relief etching

A class of surface machining (etching) which has been particularly useful for electro-optic devices is the formation of relief features. These features are typically produced by irradiating the surface with a spatially varying light intensity. Much of the work has used III-V semiconductors because they constitute the light-generating and light-absorbing components of many fiber optic systems. Figure 3.2.76 shows a holographic grating etched in a GaAs/AlGaAs substrate.

Figure 3.2.76: (a) Cross section of a patterned semiconductor for evaluating the spatial resolution of a grating etched into the surface. (b) cross section of a grating etched into a semiconductor with high spatial resolution. (c) cross section of a grating with poor spatial resolution.

Diffraction gratings can be etched into semiconductors by a direct holographic process [100]-[112]. The primary goal is to produce gratings that can be used in the fabrication of distributed feedback lasers, distributed Bragg reflector lasers, filters, and guided-wave couplers. These applications require sub-micrometer grating periods, usually less than 0.5 μm.

Most of the work has been performed on GaAs ([100]-[105], [107]-[121]), with many of the studies using dilute H_2SO_4:H_2O_2:H_2O in a volume ratio of 1:1:25-100. Very short-period gratings (< 0.4 μm) can be etched in GaAs; the total etch depth necessary to achieve a modest surface relief height is large for most optical device applications. That is, if the etched grating is to be 0.4 μm in depth, one may have to remove 0.8 to 4.0 μm (or more) of material (see Figure 3.2.64). On the other hand, the longer-period gratings (> 0.8 μm), which require the removal of less GaAs, have limited use in waveguide applications. Grating formation in InP has also attracted considerable interest because of InP-based optical communications at 1.3- and 1.55-μm wavelengths ([100], [105]-[107], [112]).

The analysis of the transport properties of the semiconductor and chemical reactivity of the surface has provided a framework for understanding many of the observations concerning the spatial resolution of PEC etching. A general feature of the experimental results is that the depth etched in the illuminated areas increases more slowly than the depth etched in the unilluminated area as the size of the features becomes smaller. This behavior is due to the diffusion of the photogenerated holes, reducing the spatial contrast of the hole distribution at the interface. Quantitative aspects of this have been discussed in several papers ([97], [113]-[117]). The conclusions are useful in understanding the parameters that control PEC etching and in improving its spatial resolution. The diffusional spreading of the holes is greatly enhanced by a slow chemical reaction. The spatial resolution of gratings can be improved by choosing an electrolyte with a high chemical rate constant, as has been demonstrated in GaAs, AlGaAs, and InP ([116], [117] and references therein). It has been shown that the rate of the chemical reaction can be increased by raising the temperature of the electrolyte [118]. A 25°C increase in the temperature of the electrolyte improved the grating amplitude by a factor of 1.7.

It was also shown that the spatial resolution degraded with deeper penetration of the light into the semiconductor, experimentally accomplished by changing the wavelength. Increasing the lifetime or mobility of the carriers degrades the spatial resolution of the PEC-etched gratings. In effect, the average time before the hole is consumed in the etching reaction was decreased while keeping the chemical reaction velocity constant. This analysis is particularly important because of the long lifetime of carriers in silicon compared to III-V semiconductors. The gratings etched in $Al_{0.3}Ga_{0.7}As$ are about three times deeper than in GaAs because of the lower hole mobility in $Al_{0.3}Ga_{0.7}As$ [117]. Thus, 0.3-μm gratings with high amplitudes can be fabricated in $Al_{0.3}Ga_{0.7}As$, as shown in Figure 3.2.64. These results were used to fabricate a 0.35-μm pixellated grating array on a GaAs waveguide with an AlGaAs cladding layer [119].

Matz demonstrated a two-step process for producing high-aspect-ratio gratings in n-GaAs and n-InP. After a shallow grating was formed along the [011] direction by direct illumination of the crystal with a diffraction pattern, the sample was chemically etched [109], [120]. A triangular grating pattern was formed owing to the slow-etching (111) Ga planes. This orientational dependence of the etch rate has been extended to the fabrication of Echelle-type diffraction gratings. GaAs was cut at an angle off the (100) plane toward the (011) plane and etched [121], yielding structures with the interior angles favored by the etching of the Ga-rich surface. The ability to monitor the total etch depth through the current is particularly important in this case.

In addition to gratings, numerous other shapes have been etched (chemically machined) into III-V structures. Integrated microlenses have been etched into InP light-emitting diodes (LED) by projection patterning [98]. The lenses are used to efficiently couple the light from the LED into an optical fiber. The lenses are 100 μm in width and 10 μm in height. The linear relationship between etch rate and light intensity is especially useful. Projection patterning was also used to form dish-shaped openings in an InGaAs layer used as an ion implantation mask for a novel InP/InGaAsP avalanche photodiode [112][113]. The gradual shape of the dish-shaped structure avoided edge breakdown at a sharp edge. A via-hole technology has been demonstrated by Podlesnik *et al*. using an electroless PEC process [124][125]. They showed that lasers can be used to produce many shapes, including straight-walled holes. It was demonstrated that fiducial patterns on one side of an n-InP wafer could be PEC-etched through a 90-μm-thick wafer [99]. The metal mask served the dual purpose of the electrical contact and etching mask.

The etching was carried out under potentiostatic control. A long-wavelength annular InGaAs photodiode was fabricated by etching a hole through the back of the device using controlled potential etching. The n-InP was photoetched, and the etching was stopped at the p/n junction by proper biasing of the sample [126]. Khare *et al*. showed that the dopant-type selectivity of n-GaAs on p-GaAs was 15000:1, and the selectivity for n-GaAs on unintentionally doped GaAs was 30:1 [127].

The micromachining of GaAs and InP was studied at high laser intensities [128]. Vertical walls were achieved at high laser intensities, while a crystallographic taper was found at lower intensities. It was observed that conductive n-type substrates etched rapidly, while semi-insulating substrates exhibited enhanced etching only when a metal mask patterned the substrate, providing a low-resistance contact for electron removal. The directionality is believed to be aided by confinement of the processing beam within the hollow etched structure. A 200-μm high-pass filter has been fabricated using PEC etching through a Si-doped n-GaAs wafer [129]. A series of highly anisotropic waveguides with a 3:1 aspect ratio were formed. The effects of orientation and doping were demonstrated on the etching of deep trenches in GaAs [130]. Grooves were etched using a complexing agent (4,5-dihydroxy-1,3-benzene disulfonic acid) for Ga. The pointed bottoms of the grooves were formed along the [011] direction. The high doping density decreased the undercutting of the mask. The field in highly doped material is large, which reduces the lateral diffusion of carriers.

Khare *et al*. have demonstrated highly selective band-gap etching of AlGaAs [131]. Material having a high Al concentration was PEC-etched in $HCl:H_2O$ 1:20 by using wavelength selectivity. Relative etch rates of 10000:1 and 1000:1 were found for Al mole fractions of 0.15 and 0.05, respectively.

PEC etching has been used to improve the performance of solar cells. Soltz *et al*. etched antireflection relief microstructures into n-InP [132]; the triangular features were holographically formed parallel to the (011) direction. The improvement in performance of thin-film polycrystalline $CdSe_{0.65}Te_{0.35}$ solar cells was realized by PEC etching and annealing [133]. Maximum quantum efficiencies near 100% were achieved.

A PEC-etching technique was developed for electromechanical sensors, mesa structures, and bipolar and CMOS SiC devices [134]-[136]. Etch rates as high as 100 μm/min have been achieved; these are the highest reported rates for any room-temperature SiC etching process. High-aspect-ratio structures were formed, and the p/n junction was used as the etch-stop.

The photoetching of n-type semiconductors is relatively straightforward because the photogenerated minority carrier (holes) often leads directly to the decomposition of the lattice. In the case of p-type semiconductors, the etching reaction must depend on the minority carrier (electrons) in order to have photoinitiated process. The ability to PEC-etch p-type materials has been demonstrated with p-InP and p-GaAs. In a two-step process, the p-InP was first photoelectrochemically reduced, forming phosphene and metallic indium [95][96]. In the second step of the process, the indium was electrochemically oxidized from the surface. In a further development by Quinlan on this same theme, the zero-valent indium was chemically oxidized off the surface using dilute nitric acid [96]. An analogous process for silicon would be very interesting, yielding silane; however, none has been reported.

The observation that mechanical damage inhibited the PEC etching of n-GaAs led Yamamoto and Yano to pattern the surface of a GaAs wafer for selective material removal with the damage induced by ion bombardment [137]. The ion damage provides a recombination center for the photogenerated carriers [138][139]. The PEC etching was completely suppressed by a 20-keV dose of nitrogen ions at a density of 10^{15} ions/cm^2. The method has been extended by use of a direct-write, focused ion-beam (FIB) patterning step. A dose of only 10^{10}-10^{11} ions/cm^2 was needed to write patterns in n-type GaAs, InP, InGaAs, and InGaAsP [139]. The minimum feature size obtained was about 1 μm.

There are several ways in which semiconductor materials can be used to initiate the deposition of metals. The reduction of electroactive solution species (via conduction-band electrons) can be carried out using photogenerated minority carriers in p-type materials or directly on n-type semiconductors in the dark. The filling of small, high-aspect-ratio structures is of particular interest in micromachined devices. The electroless deposition of gold was carried out in GaAs FET via holes by the photoinitiated dissolution of semi-insulating GaAs [99]. The GaAs undergoes photodecomposition, which provides the source of electrons for reducing $Au(CN)_2^-$:

$$6Au(CN)_2^- + GaAs \rightarrow 6Au + 12CN^- + Ga^{3+} + As^{3+}$$

The Schottky barrier within the GaAs allows only holes to migrate to the semiconductor-solution interface. In this way, the via holes are filled from the bottom to the top.

Photoelectrochemical etching of III-V semiconductors has been used to form unique structures in electronic and photonic devices; these include integrated lenses on light-emitting diodes, gratings on laser devices, and through-wafer via connections in field-effect transistors. The PEC etching of silicon is of considerable interest for micromachining devices in silicon wafers, because it offers several advantages over conventional processes. However, two significant obstacles remain for the PEC etching of high-spatial-resolution structures in silicon: the interference of oxides and the long diffusion length of carriers in silicon. Nonaqueous solvents provide a non-oxide processing environment; however, many technological details remain to be addressed.

3.2.5.4.5 Micromachined coplanar waveguide on GAAS for optoelectronic IC applications

One of the most successful techniques for building hybrid optoelectronic integrated circuits (OEIC) involves integrating flip-chip optoelectronic devices directly on electronic IC chips. To take full advantage of optoelectronic integration, incorporating optical waveguides into IC chips or flip-chip substrates is indispensable. Advances in electronic ICs with as high a bit rate as 100 Gbit/s require an ultra-broadband microwave waveguide, which is also better suited for an OEIC package with good connectivity to optical fibres and waveguides.

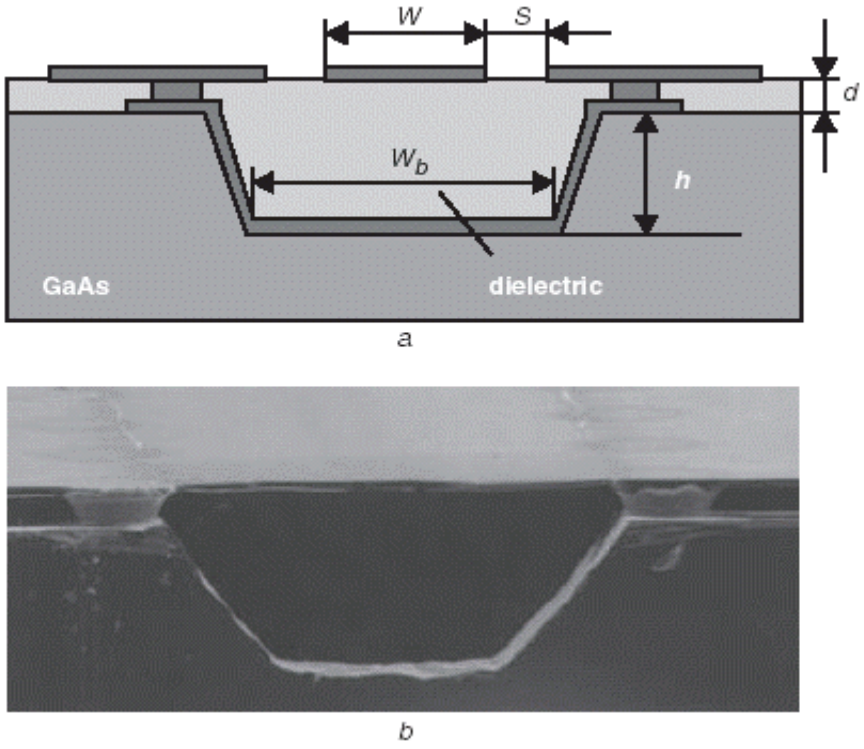


Figure 3.2.77: (a) Schematic cross-sectional view of grooved conductor-backed coplanar waveguide (b) SEM micrograph of realised structure.

Micromachining is an emerging technique for millimetre-wave applications. Several types of micromachined interconnections and transmission lines have so far been proposed and tested up to around 100 GHz [141][143]. However, the compatibility or connectivity with optical fibres or waveguides was not taken into account. We have developed a new micromachined waveguide based on the concept of microshielding for use in OEICs with optical waveguides. The new waveguide shields the electromagnetic field of the dominant CPW like a coaxial cable does, preventing leakage to the substrate and eradicating the causes of unwanted modes and resonances [104]. In addition, because it is suitable for wide waveguides, microshielded coax-to-waveguide transitions or flip-chip solder-bump pads can be simultaneously fabricated on the chip. In [101], the fabrication and the characteristics of this novel micromachined waveguide for ultra-broadband OEIC packaging applications are presented.

Figure 3.2.77a shows a schematic cross-sectional view of the newly developed micromachined waveguide, called a grooved conductor-backed coplanar waveguide (GCBCPW). The substrate right underneath the central part of the coplanar waveguide is etched. The etched facets are metallised as a bottom conductor, and the groove is filled with a dielectric material. The bottom and top ground planes are connected by microvias. The new waveguide is advantageous as an ultra-broadband waveguide for OEICs in several ways:

(i) An electromagnetic field of the dominant mode can be effectively confined in the groove dielectric like a coaxial cable can so that it prevents electromagnetic leakage to the substrate and eradicates the sources of unwanted modes and resonances.

(ii) A GCBCPW can be fabricated simultaneously with a V-groove for fibre alignment. The main problem of an OEIC is that a lot of labour and time are needed to align the optical axis between a fibre and an optical component. A V-groove structure on a flip-chip motherboard can be used to passively align the optical axis. The GCBCPW motherboard has good connectivity to optical fibres.

(iii) The microwave property only depends on the groove dielectrics, irrespective of the substrate. If the groove dielectrics have a dielectric constant as low as 3, a waveguide as wide as twice the groove depth can be made, the dominant mode of which is the CPW mode. Then the GCBCPW is suitable for a wide waveguide. As the inner conductor radius of the W-band coaxial connector is 150 mm, the W-band coaxial-to-waveguide transition can be fabricated simultaneously on the wafer if the groove is as deep as 80 mm.

(iv) UV curable pressure-sensitive epoxy resin is chosen as the groove dielectric. Because it is generally used for a polymer optical waveguide, a GCBCPW has good compatibility with an optical waveguide. The GCBCPW can be applied for both an optical and a microwave waveguide in polymer optical modulators. Figure 3.2.77b shows a SEM microphotograph of a fabricated GCBCPW. The depth of the groove is 80 mm and the width is 140 mm. The applicable impedance range of the GCBCPW is 30 170 Ω, since the dielectric implanted under the signal line is as low as 3 and a photolithography resolution of a slot is as narrow as 1 mm. However, an impedance of less than 10 Ω can be made if it is without the groove. This wide impedance range enables, for example, making an ideal step impedance filter.

In [49], a novel micromachined waveguide has been developed on a GaAs substrate, which has good compatibility with optical waveguides. By adopting a microshielded structure, unwanted substrate modes and resonances can be suppressed by preventing electromagnetic fields leaking to the substrate. No fine dips could be detected in the measured S-parameters, which verifies the effectiveness of the newly developed GCPCPW at the frequencies up to 110 GHz. The new micromachined waveguide might be a good candidate for ultra-broadband transmission lines for use in both OEIC chips and flip-chip motherboards with optical waveguides.

3.2.5.4.6 Etching Technology with Reactive Ion Etching System for GAAS Via-Hole Etching

In GaAs monolithic microwave integrated circuits (MMICs), the via-hole grounding technique is very important because it can reduce the source grounding inductance and heat dissipation, thus the high-frequency characteristics such as RF gain, distortion, and efficiency, can be improved. Using the technique, an improvement in the RF gain of MMICs of at least 2 dB, compared to those with wrap-around source ground, has been reported [145], [146]. Traditionally, wet etching has been used to implement the via-hole process, but it suffers from the uniformity limitation, lack of via-hole profile control, and undercut. Recently, plasma dry etching such as inductively couple plasma (ICP), electron cyclotron resonance (ECR), and reactive ion etching (RIE) have been successfully used to replace wet etching for their tighter etching condition controlling to get the better uniformity and desired via-hole control [147] [149]. However, the plasma densities in ICP or ECR are so high they cause the profile to be too sharp for real application. Only the RIE can get a sloped profile to release the problem of step coverage in backside metallization. In [144] a detailed study is presented using the RIE system with a two-step recipe in base of BCl Cl gas mixtures to implement the via-hole process for the first time. With the two-step recipe, about an 80 sloped angle of the etched via-hole measured from the horizontal surface can be obtained reproducibly. The average etching rate is larger than 1 m/min (cf. Figure 3.2.65) and selectivity between GaAs and photoresist is higher than 25:1. The uniformity deviation is less than 10% as well.

3.2.5.4.7 Dry Via-Hole Etching of GAAS using high-density C12 AR plasma

Through-wafer low-impedance via connections can improve the characteristics of GaAs monolithic microwave integrated circuits. Such vias will lead to higher packing densities, improved gain by reducing parasitic impedance, and simplified design layout. While GaAs has a relatively low thermal conductivity, existing vias can act as heat sinks to the integrated circuits. GaAs via holes have been produced using reactive ion etching (RIE) [153], electron cyclotron resonance etching (ECR) [156][157], inductively coupled plasma [158] and laser micromachining techniques [159]. ECR is an important plasma etching technique as processes can be developed in high plasma density, low pressure, and low temperature environments [160][161]. ECR processes typically have broad process windows and numerous varieties of process applications. A number of different plasma chemistries have been reported to yield good results for etching GaAs substrates. These gases include BCl3/Cl2 [162], CCl2F2 [127] [163], and SiCl4/Cl2. [152] reports on a high etch rate GaAs via hole processes in an ECR system using a Cl2 /Ar plasma.

As for the production of GaAs via connections using ECR, Shul *et al*. [156] investigated and compared RIE and ECR etch results using both polyimide and STR-1110 photoresist masks. Using a Cl2 /BCl3 ECR-generated plasma, GaAs etch rates greater than 3.2 μm/min were achieved with selectivities to STR-1110 photoresist and polyimide of approximately 20:1 for a 5 min plasma exposure. Pearton *et al*. [157] etched small diameter (<30 μm) via holes using a Cl2 /BCl3 discharge. The influence of the Cl2 to BCl3 ratio, masks (either Ni or resist) on the profile, and etch rates were studied. Due to the enhanced plasma density, acceptable etch rates for via hole formation (0.5 1.5 μm/min) were obtained. The influences of process parameters on the profile and GaAs etch rates were studied in detail. A maximum etch rate of 6.7 μm/min was obtained for a sample etched using a 150 W, and 50 mTorr, respectively. Therefore, higher throughput can be achieved. Moreover, controllable profiles were obtained under different conditions for various applications.

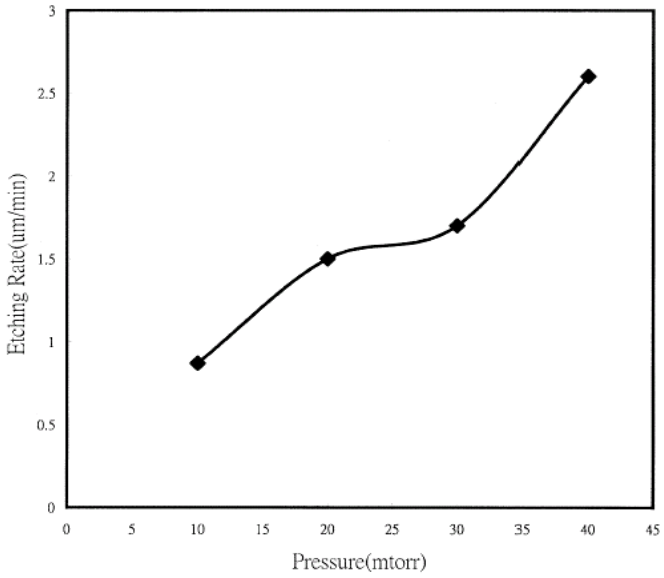


Figure 3.2.78: Dry etch rate vs. pressure.

An n-type, Te-doped, 100 oriented GaAs substrate was used in this study. The samples were cleaned using isopropyl alcohol and acetone prior to resist coating and lithography to define the reversed 70 mm diam via patterns onto the wafer. A bilayer of 200 nm Ni and 10 nm Ti was then evaporated and lifted off to transfer the 70 mm diam via patterns onto the samples. The process was developed in an ECR system equipped with an RF-biased chuck capable of accommodating various sizes of samples and operating at various temperature ranges. The RF chuck is powered with a 13.56 MHz, 500 W generator. The reactor is configured with an Nd Fe B permanent magnet to generate the resonance zone. The process chamber is surrounded by a permanent magnet jacket, which helps to confine the plasma at the center of the chamber, away from the chamber walls. Ar gas enters the reactor chamber through an upstream gas manifold, while Cl2 enters the chamber through the downstream. After etching, samples were cleaved to reveal the cross-sectional view of the vias. The GaAs etch rates were measured using a Dektak stylus profilometer. Via hole profile, surface, and sidewall morphology were investigated using an optical microscope and a scanning electron microscope (SEM). Unless otherwise mentioned, the study of the GaAs etch rates and etch profiles was carried out with the process time, process pressure, microwave power, and RF power fixing at 5 min, 10 mTorr, 800 W, and 150 W, respectively.

The dependency of the GaAs average etch rate on the chuck temperature, between 35°C and 300°C, under a constant Cl2 /Ar flow rates of 30 sccm/10 sccm, was studied. The process etch rate was found to stay at about 560.5 μm/min at this range of temperature. The relationship between the average GaAs etch rate and the process pressure is shown in Figure 3.2.78. The process was carried out at a constant microwave power of 800 W, Cl2 /Ar gas flow rates of 20 sccm/10 sccm, and RF power of 150 W. The process pressure was varied from 5 to 50 mTorr, which resulted in an increase of dc bias from 30 to 105 V. The etch rate increased almost linearly as the process pressure was increased from 5 to 30 mTorr, suggesting that the process is at a reactant limited regime at this low process pressure window [156]. The etch rate is expected to increase with increasing process pressure as more chlorine reactants will be transported process conditions, the resulting dc bias increased from 5 to 40 V. The etch rate was found to increase almost linearly with increasing Cl2 percentage in the Cl2 /Ar plasma.

A similar process trend has been observed by Nordheden *et al*. [164] and Salimian. It can be seen that the average GaAs etch rate increased by a factor of about 85 (i.e., from 0.06 to 5.1 μm/min) as the Cl2 percentage in the Cl2 /Ar plasma increased from 0% to 80%. In these experiments, the RF power was varied from 50 to 350 W, resulting in an increase of dc bias from approximately 10 to about 110 V. In these processes, the flow rates of Cl2 /Ar were kept at a constant rate of 30 sccm/10 sccm. The etch rate increased by approximately a factor of 3 as the RF power increased from 50 to 200 W (i.e., from 2.0 to 5.7 μm/min). At a high RF power, the enhancement of the etch rate might be due to the effect of sputter desorption of the etch products from the surface after the bombardment of the energetic ions.

3.2.5.5 Ion Implantation

Ion implantation is, in general, used for doping purposes, but it is also a useful micromachining technology for MEMS applications. Depending on the ion dose, implanted atoms can modify the semiconductor doping level or material property, to produce either etch-stop or sacrificial layers. The ion penetration depth in the semiconductors can be precisely controlled by the ion energy. Using proper masking, localized ion implantation can be used to create localized sacrificial regions for sensor applications [165].

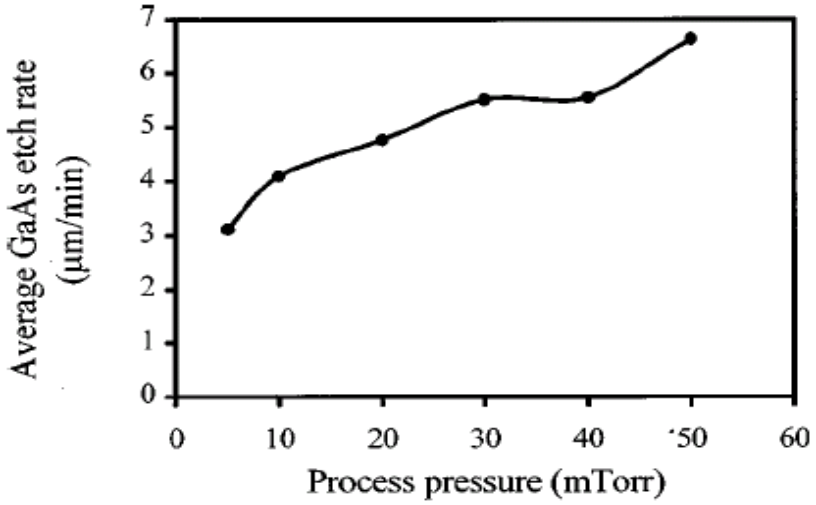


Figure 3.2.79: Dry etch rate vs. Pressure.

The cross-bridge, coiled and corrugated GaAs membranes have been successfully fabricated using deep nitrogen implantation and pulsed electrochemical etching. Figure 3.2.79 schematically illustrates the fabrication steps for the GaAs cross-bridge and coiled membranes. Nitrogen with a low dose is implanted into n-GaAs, forming a damaged layer on the top of the n-GaAs substrate. The sample is then annealed at 600°C for 10 min with plasma-enhanced chemical vapour deposited (PECVD) Si_3N_4 a as cover layer to compensate for the top damaged layer which becomes a semi-insulating GaAs layer. An ohmic contact was fabricated on the reverse side. The photoresist was used to define the membrane pattern. Non-selective etching of GaAs using H_3PO_4:H_2O_2: methanol = 1:1:1 in volume has been performed in order to etch through the top semi-insulating layer down to the n-GaAs substrate. This etching solution leads to a smooth etching surface with an etch rate of about 6 μm/min and almost vertically etched GaAs sidewalls. Subsequently, the selective etching was carried out in the pulsed anodic etch bath to release the top semi-insulating GaAs membranes.

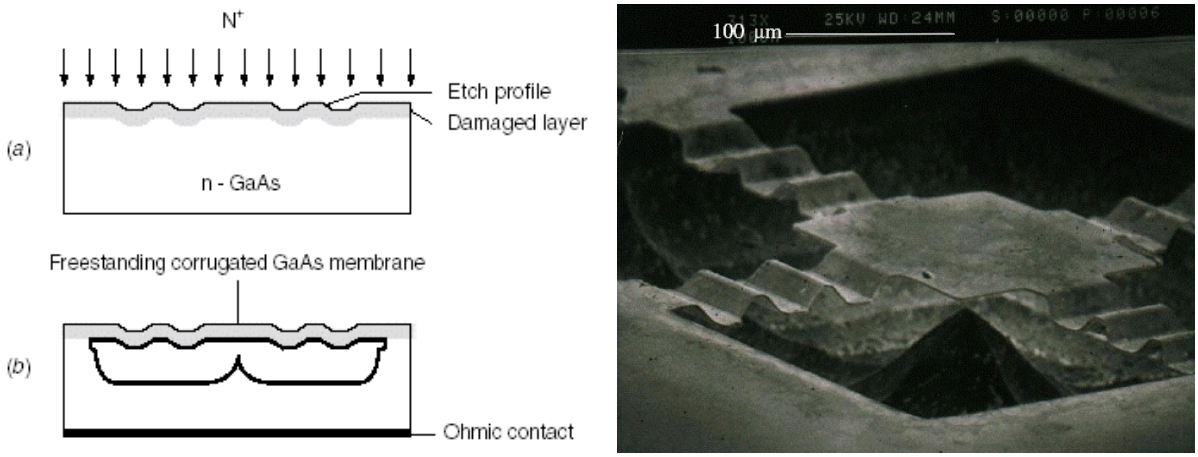


Figure 3.2.80: Fabrication process of a GaAs membrane by nitrogen implantation and pulsed electrochemical etching.

Nitrogen implantation with subsequent annealing is a suitable process for micromachining GaAs membrane structures in combination with the pulsed electrochemical etching. The nitrogen-implanted n-GaAs layer has the highest resistivity after annealing at 600°C for 10 min. Due to the relatively low ion dose, there is no significant residual stress introduced in GaAs membranes and the fabricated membranes show good mechanical stability, which is very critical for MEMS applications.

3.2.5.6 Conclusions

The presented III-V compound MEMS describe the potentialities of the different material systems for various application of the information technology. This short review of membrane-based technologies shows that bandgap engineering can be used to include new and efficient sensing and actuation schemes in MEMS. More is still to be done to solve packaging problems. This will speed up the insertion of MEMS in many areas of our life and help to reduce manufacturing costs.

3.2.6 CNC Milling

3.2.6.1 Overview

Computer Numerically Controlled milling (CNC) is the process of producing physical objects from its digitised 2D or 3D description, by automatically excavating the object shape out from a block of raw material.

This type of fabrication process is relevant for antennas when there are complex shapes involved with tight tolerances on dimensions and surface finish as happens for instance with shaped lens antennas or reflector antennas at millimetre-waves.

This technology tends to be more indicated for small series production or for lab prototyping as opposed for instance to the injection moulding process, which is cost effective for mass production. CNC milling may, however, be used for mould production for the latter technology.

The CNC milling technology is completely general, not specific for antennas, so the description that follows is general. Application examples of this technology for the fabrication of a shaped dielectric lenses is presented at the end.

3.2.6.2 CNC Milling Process

First a digitised model of the antenna (or antenna part) is required. This may be exported directly from the electromagnetic solver in a standard format, or be generated by appropriate computer aided design tools like the commercially available AutoCAD [43] or MasterCam [167].

CNC milling process involves two steps: the first step is the *toolpathing*, the process of translating a 3D or 2D computer model into a series of 'paths' for the CNC milling cutter to follow as it excavates the model, taking into account aspects such as cutter size and shape, material type and the constrains of the machine. Commercial software like MasterCam is available for this task.

The second step of the procedure is the actual machining, which involves translating the *toolpaths* into commands to move the milling head incrementally along the axis directions that are available on the machine. For instance 3-axis CNC mills have two axes for horizontal movement of the table (*x*- and *y-axis*) and another for its vertical movement (*z-axis*). A 4-axis machine may have a further axis associated with a z-movement of the milling head, or with its horizontal pivoting. The larger the number of axis the better the flexibility to obtain complex shapes with less operator intervention during the milling process.

Software tools like MasterCam also can produce the code to command the axis movements according to the defined *toolpaths*. CNC milling machines are traditionally programmed using a set of commands known as *G-codes* that represent specific CNC functions in alphanumeric format. These are uploaded to the CNC mill through a communications port (ex. Serial port). In the limit, the user can generate the necessary *G-codes* within his home-developed antenna design tool, provided that he completely understands the required *toolpathing* requirements.

The CNC mill that is available at IST (Dep. of Electrical and Computer Engineering) is a 3-axis machine – FIRST CV-205 – with a FANUC 20F controller (Figure 3.2.81) [168]. Achievable accuracy is of the order of 50 microns.

Figure 3.2.81: CNC milling installation at the Dep. Electrical and Computer Eng. of IST.

3.2.6.3 Using the Technology

Depending on the complexity of the antenna and on the number of available CNC axis on the machine, it may be required to split the milling process for one antenna object into separate jobs. Each of these jobs involves the object manual rotation and re-alignment to continue the milling process in the parts of the object that were not accessible in the previous job by simple translation or rotation of the available axis. This is the first aspect to look at to decide if an available CNC mill is enough for the fabrication of a given antenna model.

Determining the size and shape of the cutting tool is related to the antenna surface curvature radius or required type of cuts, required surface finish and type of material. To excavate the object, the mill must not cut deeper than at the most half the cutting tool diameter in order not to break. On the other side, in order to have a smooth finish the cutting tool must overlap itself each time it makes a pass on the object surface by at least its half diameter. These aspects together have an impact on the length of time required for machining one object and may easily reach several hours.

There are no special limitations on the materials that can be used for CNC milling, except that they must be machineable. Several types of low loss machineable dielectrics are commercially available. For instance, Emerson & Cuming [169] produces these materials with a large range of dielectric permittivities. The rotation speed of the cutting tool and the cutting speed must be appropriate for the object material. Dielectrics may be cut faster than metals. The material of the cutting tool must be also adequate for the object material. Note that there are soft dielectric materials (for instance, ECCOSTOK HiK from Emerson & Cuming [169]) that are quite abrasive and require hardened cutting tools, such as carbide tools.

3.2.6.4 Application Examples

IST has been working for the past decade on homogeneous and non-homogeneous dielectric lenses for millimetre-wave applications. One of these applications – Mobile Broadband Communication Systems at Millimetre Waves – was studied in the framework of two European funded projects (RACE-MBS, and ACTS-SAMBA), required the development of constant flux antennas for illumination of shaped cells.

IST proposed for this task a homogeneous lens antenna configuration with an unconventional 3D shape that was designed to transform the radiation pattern from an embedded waveguide feed into a highly shaped output beam [170]-[172]. Examples of theses lens antennas are shown in Figure 3.2.82. Because of its 3D shape, the lenses in both examples were fabricated with CNC milling technology.

(a) (b)

Figure 3.2.82: Shaped dielectric lens antennas for Mobile Broadband Communication Systems. (a) MBS Project, 62-66 GHz – constant flux illumination of elongated cells; (b) Constant flux illumination of square cells at 62.5 GHz.

The lens in Figure 3.2.82a was designed to produce a constant flux illumination of elongated cells, like a 200 m section of a narrow street when positioned at half street length, while the lens in Figure 3.2.82b was designed to produce a square footprint with constant flux intended for illumination of a square room.

One of the challenges in mm-wave mobile broadband communication systems is to control reflection from walls and lateral objects [173]. With this objective the antennas were designed to produce sharp illumination boundaries as shown in Figure 3.2.83. The overall dimensions of the covered region may be scaled up or down simply by changing the antenna installation height.

Further work is being carried out presently at IST related with double shell shaped lenses that will require CNC milling for its fabrication. CNC milled lenses with exotic 3D shapes were also recently produced in IETR [174] to obtain constant flux beams and Gaussian beams.

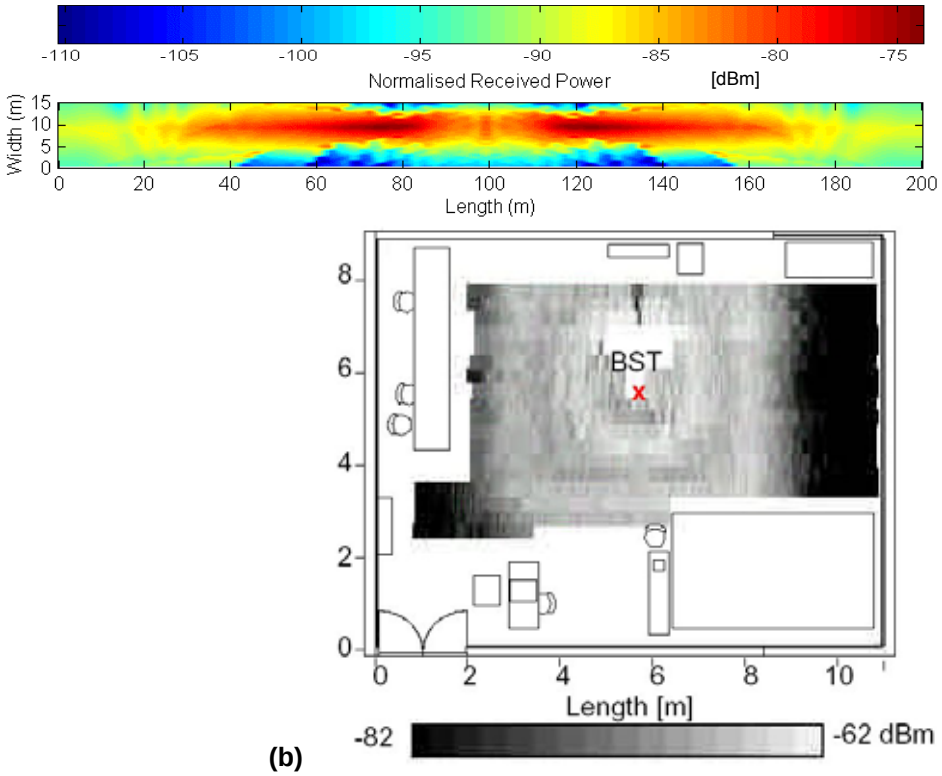


Figure 3.2.83: Received power distribution on rectangular cells produced by shaped dielectric lens antennas in the 60 GHz band. (a) Elongated cell lens; (b) Square cell lens.

3.3 POTENTIAL ANTENNA APPLICATIONS

3.3.1 State of the Art

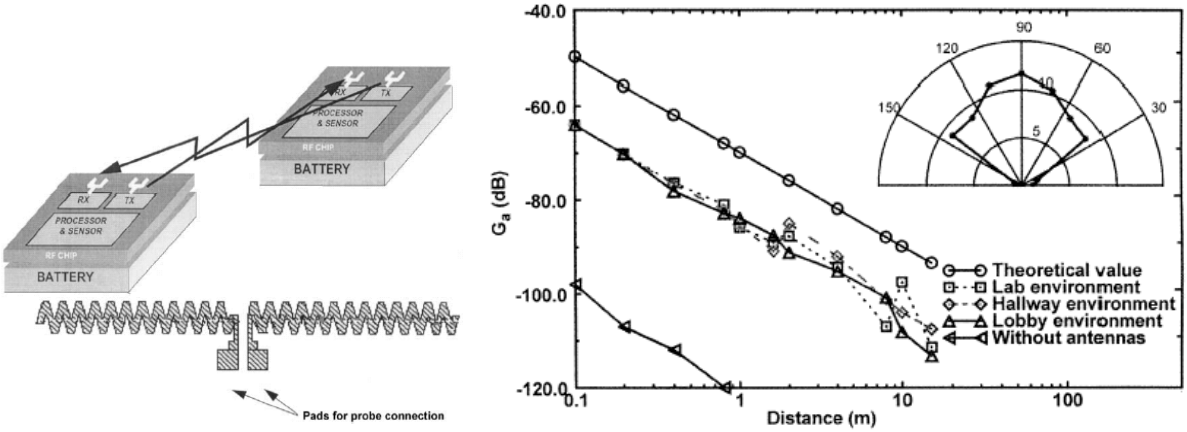
3.3.1.1 Introduction

As system requirements for faster data transmission in lighter compact designs drive the technology area, higher frequency design solutions with large density layouts require integration of microwave devices, circuitry, and radiating elements that offer light weight, small size, and optimum performance. Compact circuit designs are typically achieved in high-index materials, which is in direct contrast to the low-index substrates imposed by antenna performance requirements.

Below 1µm minimum feature size, interconnect parasitic effects begin to hurt circuit and system performance seriously. Though much work is going on to reduce resistivity of conductors and dielectric constant of interlayer dielectric materials, this approach will soon encounter fundamental material limits for which no known solution exists. With this background, projected increase of clock frequency and a large die size for CMOS circuits have led to the concept for on-chip wireless clock signal distribution using microwaves. However, a large increase in transmission gain is necessary to cover the future chip size.

3.3.1.2 Antennas on electrically thick substrate

On-chip 2-mm zigzag antennas with a bend angle of 30° are fabricated in [175] on 20Ωcm silicon substrates with a 1μm oxide layer. The substrate thickness is ≈ 670μm. Figure 3.3.1 shows a layout of a zigzag dipole antenna. This chip is similar to that used for investigating antennas for intra-chip communication. All antennas are fabricated using a single aluminum-level process. The metal thickness and width are 1.5μm and 30μm, respectively. The metal and oxide layer thicknesses as well as metal widths and lengths are compatible with standard CMOS fabrication technology. The spacing between the chip edge and zigzag antennas is 100μm. This spacing is kept small in order to reduce the loss in silicon substrates. The transmission-gain results indicate that for a communication link at 24GHz with a data rate of 100kb/s and receiver sensitivity specification of −96dBm (the minimum signal power level that can be detected with acceptable robustness by a receiver) a distance of 5m can be bridged with a transmitted power of 10dBm. This demonstrates that the 2mm-long zigzag dipole antennas fabricated on 20Ωcm silicon substrates despite the loss associated with the conductive substrate are adequate for inter-chip-communciation applications.



(a) (b)

Figure 3.3.1: Single chip radio. (a) Layout of a 2mm zigzag dipole antenna. The working range can be up to 5m. (b) Antenna pair power gain versus distance at a 52cm height from the floor. The gains are measured using a pair of 2mm zigzag dipole antennas in three different environments at 24GHz. The inset shows the 2mm zigzag antenna radiation pattern. The antenna pair separation is 1.7m.

Another application of interest is the wireless data transmission from one part of the chip to another. A common problem for large microprocessors is the distribution of a clock-signal, which experiences significant delay when lead by microstrip lines through the chip-area. A wireless clock distribution system consists of a clock transmitter, located on or off chip, broadcasting a microwave global clock signal at frequencies around 20GHz or higher, and a grid of integrated clock receivers.

There are three main paths for electromagnetic wave transmission from an on-chip antenna. One path is along the surface (surface wave) and the other two are through and below the substrate. The feasibility of integrated antennas for a wireless clock distribution system is investigated in [176]. The measured antennas are shown in Figure 3.3.2. The loop antenna with a compact size, having a diameter of 200μm, and an isotropic radiation pattern is ideal for a transmitter antenna. The antenna test structures were fabricated using a single aluminum level process with no passivation. The thickness of the metal line is 2μm fabricated on a 20Ωcm substrate at 15GHz. The metal width of the antennas is 10μm.

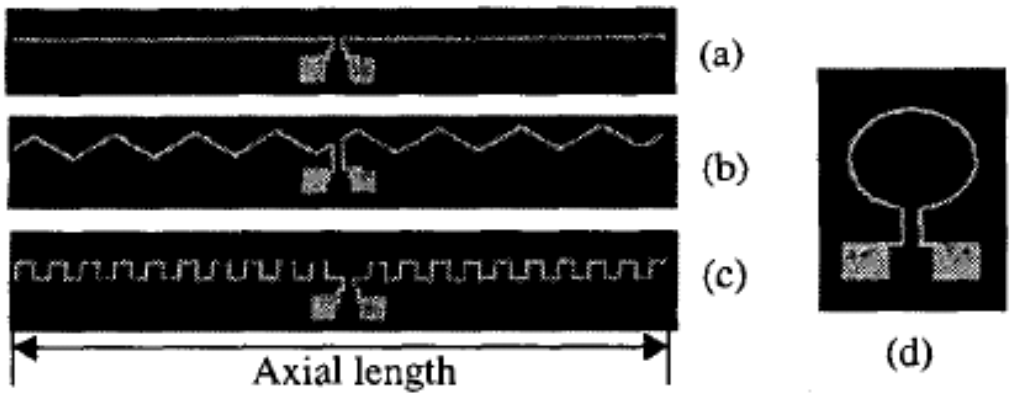


Figure 3.3.2: Microphotographs of (a) linear, (b) meander, (c) zigzag dipole and (d) loop antennas.

A wide range of linear, meander, zigzag dipole, and loop antennas on 10 and 20Ωcm silicon and SOS substrates have been experimentally evaluated. A 9μm thick oxide layer on top of the silicon substrate reduces losses. A 2mm long, 30μm wide, 30-degree zigzag dipole antenna pair on a 20Ωcm silicon substrate has shown −56dB of transmission gain near 18GHz with a distance of 10mm.

For millimetre-wave applications the on-chip patch or slot antenna is an attractive technique for realising fully integrated monolithic transmitters and receivers. However, the chip area consumed by the radiating elements and feed lines represents a major drawback, especially at the lower frequencies. To overcome this, the possibility of using the back face of the chip as an integral part of the antenna is very attractive.

In [177] a technique is described for using the back face of amonolithic chip to realise integrated radiation elements. By using the thin-film microstrip (TFMS) transmission-line medium, electrical isolation between the radiating elements and the front-face circuitry is achieved. Through-GaAs via holes are used to interconnect the radiating elements and the TFMS feed lines. A 35GHz prototype monolithic antenna has been successfully tested.

The TFMS technique uses a ground plane on the front of the chip, with a thin dielectric film deposited on top to form the substrate for the miniature microstrip lines. With this technique the back-face metallisation can be patterned to form the radiating elements, which are isolated from the front-face TFMS circuitry by the intervening ground plane. Interconnections between the radiating elements and the TFMS feed lines can readily be achieved with through-GaAs via holes.

The advantage of this technique are in its small size, the ability to optimise the semiconductor chip thickness for improved radiation efficiency and bandwidth and the scope for employing a new range of quasioptical techniques using the chip mounted directly onto a dielectric lens arrangement. The size of the patch is 1.9×1.5 mm^2 for a resonance frequency of 35GHz.

3.3.1.3 Micromachining

Compact circuit designs are typically achieved in high-index materials, such as Silicon or Gallium Arsenide, which reduces the antenna performance. In the past, this disagreement over substrate material was satisfied by selecting the substrate that offers optimum component performance. Unfortunately, this led to hybrid integration schemes and high development cost. As the frequency increases, however, this approach becomes increasingly difficult and costs are prohibitively high.

Micromachining is a technique that improves radiation element performance by removing some of the substrate material under the radiating element. The air and substrate combination produces a lower effective dielectric constant and prevents excitation of surface waves. This results in increased bandwidth and improved radiation efficiency of the radiating element.

There are a number of basic techniques that can be used to pattern thin films that have been deposited on a silicon wafer, and to shape the wafer itself, to form a set of basic microstructures (bulk silicon micromachining).

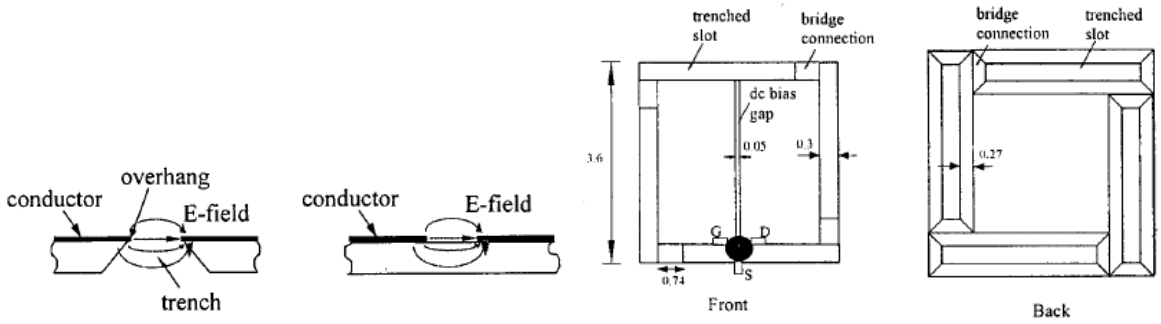


Figure 3.3.3: Silicon active slot loop antenna with micromachined trenches. (a) Comparison of slot field radiation with reverse-side etching and without trench. (b) Configuration of a trenched slot loop antenna on silicon wafer.

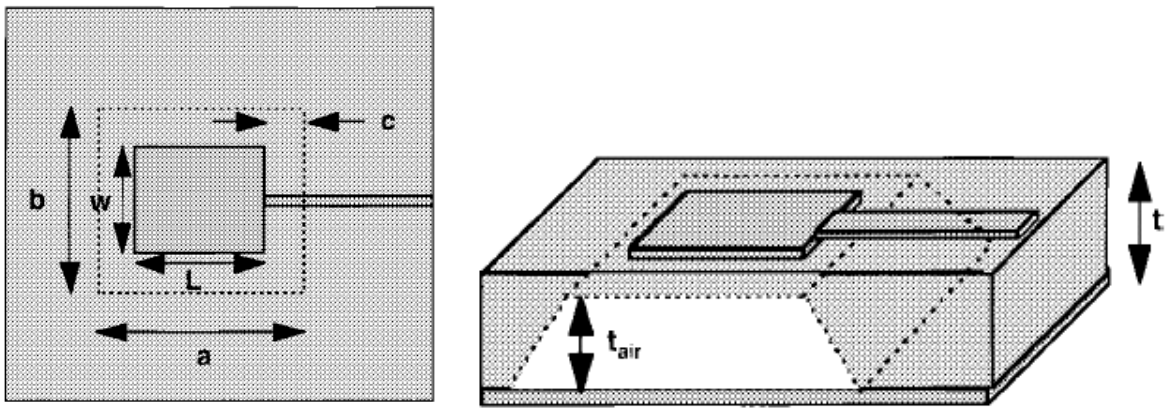
A structure for a slot antenna fabricated on a high resistivity p-type (10kΩ) silicon wafer with a thickness of 630μm is described in [28]. Wet etched micromachined trenches with conductor hangovers form the slot loop as shown in Figure 3.3.3. This method effectively reduces the effective dielectric constant of the substrate to $\varepsilon_r \approx 8.9$ and enhances radiation efficiency by 1−2dB. This can be understood since the absence of silicon material at the radiating edges of the slot makes it more efficient for the electromagnetic fields to radiate since they are mostly in air.

Microstrip patch antennas printed on high-index substrates have been revised in [35] with the primary objective to develop design solutions that can be integrated into monolithic circuit layouts while enhancing antenna performance. Microstrip antenna designs show significant performance degradation due to the pronounced excitation of surface waves in high-index materials. As a result, the antenna has lower efficiency, reduced bandwidth, degraded radiation patterns and undesired coupling between the various elements in array configurations. Optimum antenna performance depends on the choice of dielectric material as well as the choice of feeding network and is achieved when the radiated power occurs primarily as space waves with little or no components of undesired surface waves.

In [35], the use of selective lateral etching based on micromachining techniques have been presented to enhance the performance of rectangular microstrip patch antennas printed on high-index wafers such as silicon, GaAs, and InP.Micromachined patch antennas on Si substrates have shown superior performance over conventional designs where the bandwidth and the efficiency have increased by as much as 64% and 28%, respectively. In this paper, the silicon material is removed laterally underneath the patch antenna to produce a cavity that consists of a mixture of air and substrate with equal or unequal thicknesses as shown in Figure 3.3.4.

Material is removed underneath the antenna by using selective etching techniques and the excitation of surface waves is suppressed by creating a micromachined cavity air and silicon. The micromachined planar antenna design can be integrated on the same wafer with Si and GaAs IC s without affecting circuit requirements.

The measured efficiency data show 73±3% for the cavity-backed patch having an air-to-substrate thickness ratio of 3:1 and 56±3% for the regular antenna printed on the high-index material. The patch printed for comparison on 2.2 duroid was found to have an efficiency of 76±3%.



(a) (b)

Figure 3.3.4: Micromachined patch antennas.
(a) Top view of the geometry of the micromachined patch antenn with mixed air-substrate region that has been leterally etched away.
(b) Side view of the substrate cavity and the pathc antenna.

A similar approach has been followed in [34], where the selective etching process has been circumvented by using two Si substrates. One substrate carries the patch and is placed on top of of a second substrate, which has a 12 x 12mm hole. Here, preprocessing for the selective etching is circumvented by using the second substrate. Both substrates have a thickness of 254µm.

It was found that the effective dielectric constant of this patch antenna is only 2.8, compared to 9.7 for a non-cavity-backed antenna of the same thickness. The 10dB impedance bandwidth of the antenna is 12.5%, which is much larger than the typical values of 2% and 4.4% for conventional microstrip antennas of dielectric constants of 10 and 2.2 with the same substrate wavelength-to-thickness ratio.

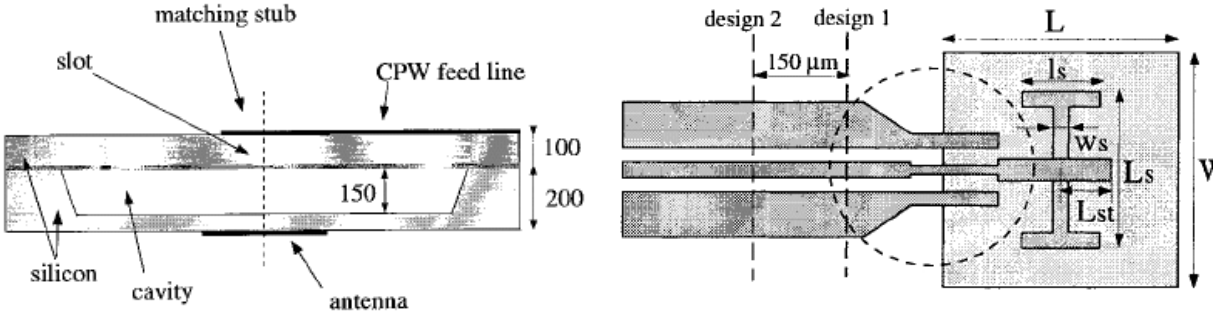


Figure 3.3.5: A 94GHz aperture-coupled micromachined microstrip antenna. (a) Cross-section of the aperture-coupled micromachined microstrip antenna. (b) Top view of the microstrip antenna design and of the CPW-to-microstrip transition.

In [178], an aperture-coupled micromachined microstrip antenna operating at 94 GHz is presented. The design consists of two stacked silicon substrates: 1) the top substrate, which carries the microstrip antenna, is micromachined to improve the radiation performance of the antenna and 2) the bottom substrate, which carries the microstrip feed line and the coupling slot. The antenna is shown in Figure 3.3.5.

The patch has a size of 380 x 380µm2. The measured return loss is −18dB at 94GHz for a 10dB bandwidth of 10%. A maximum efficiency of 58±5% has been measured and the radiation patterns show a measured front-toback ratio of −10dB at 94GHz.

The micromachined microstrip antenna is an efficient solution to the vertical integration of antenna arrays at millimeter-wave frequencies. This microstrip-type antenna has an excellent 10dB bandwidth (10%), good patterns, and high-efficiency performance and is compatible with silicon or GaAs MMIC technology. The measured radiation efficiency improved from 27±5% for the 100µmm-thick silicon substrate (ε=11.7) to 58±5%for the micromachined antenna with a effective dielectric constant of 3.

Tapered-slot antennas (TSAs) are desirable for millimeter-wave applications (such as phased arrays and focal-plane imaging systems) due to their compact design, wide bandwidth, and end-fire radiation pattern. The main limitation of the TSA comes from its sensitivity to the thickness and dielectric constant of the supporting substrate.

An effective thickness, which represents the electrical thickness of the substrate, has been defined as $t_{eff} = t(\sqrt{\varepsilon_r} - 1)$. An accepted range for good operation of a TSA has been experimentally determined by Yngvesson *et al*. to be $0.005 \leq t_{eff}/\lambda \leq 0.03$.

W-band Fermi TSAs (Figure 3.3.6) were designed on 100μm-thick silicon substrate and on 150μm-thick quartz substrate. The antennas were $4\lambda_0$ (13.3mm) long where λ_0 is the wavelength in air at 90GHz. The Fermi tapering follows with and $Y(x) = a/(1+e^{bx+c})$, where $b = 2.5/\lambda_0$ and $c = -3.25$. The aperture opening 2a is $0.86\lambda_0$ (2.85mm) at 90GHz. The slot-line feed is 20μm wide corresponding to a slot-line impedance of 67Ω. A 300 × 400μm pad at the feed of the TSA is used to place a Schottky diode, which was mounted and soldered using silver epoxy.

A 100μm-thick wafer is chosen because it is compatible with 90−100GHz low-noise amplifier circuits on GaAs or InP substrates. The effective thickness of the substrate was reduced by selectively micromachining holes in the silicon wafer using deep reactive ion etching (deep RIE). The effective dielectric constant on silicon was reduced from 11.7 to 5.1 due to the micromachining approach. The radiation patterns of the micromachined antennas were significantly better than the non-micromachined version and had similar radiation patterns to the quartz design. This shows that the predominant reason for the improved patterns lies in the reduced effective dielectric constant and not in substrate-mode suppression effects. This type of antenna is well suited for millimeter-wave imaging arrays.

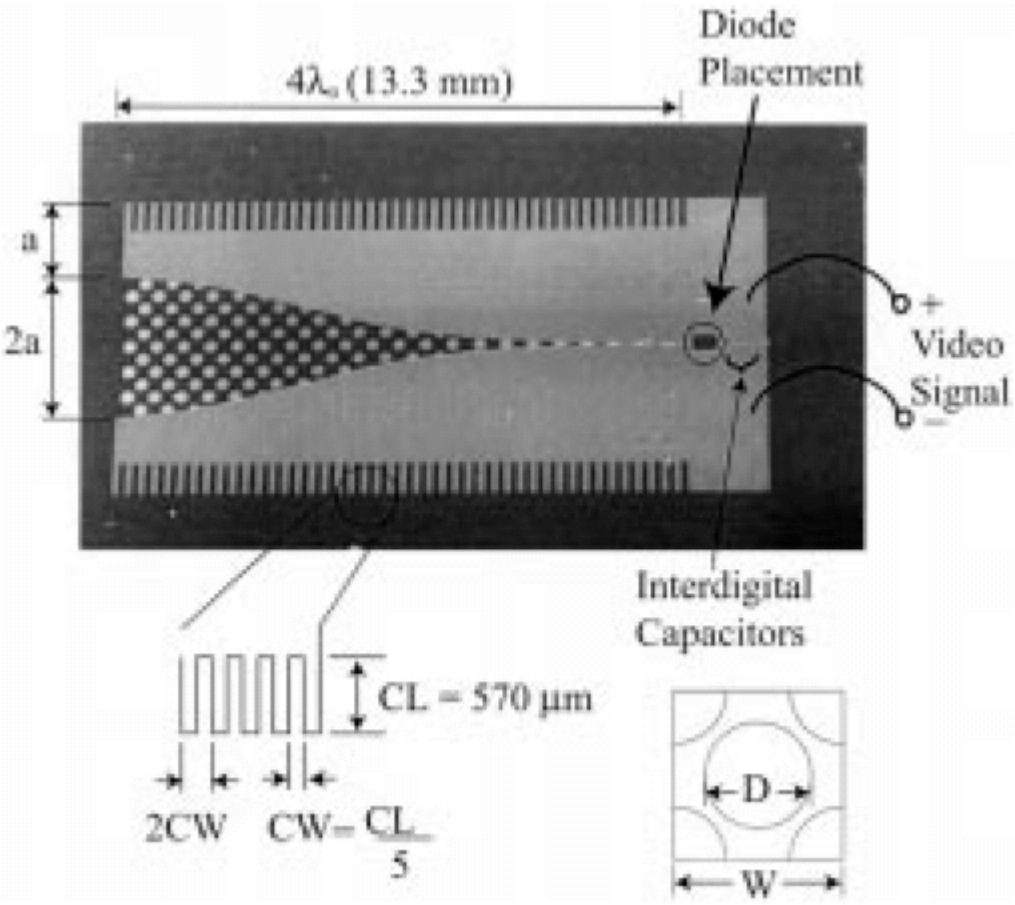


Figure 3.3.6: Picture of the W-band Fermi TSA fabricated on 100 μm-thick silicon substrate with 300 μm-wide holes etched from the reverse side.

Planar aperture coupled microstrip antennas for 77GHz are demonstrated in [31]. As far as possible, standard GaAs monolithic microwave/millimeter-wave integrated circuits (MMIC) technology is used to realize the antennas.

The antenna patches are suspended on a thin dielectric SiN_x membrane on GaAs substrate. Therefore a novel plasma-enhanced chemical vapor deposition (PECVD) process step for the fabrication of the membrane is developed and described. The single antenna patches are coupled to a microstrip line through an aperture in the ground metallisation. The method of moments in spectral domain is applied to design the patches. The feed network of a 3×1 antenna array for homogeneous excitation is simulated and optimized with a microwave design system (MDS).

From reflection measurements the operation frequency of this triple patch antenna is determined to be 77.6GHz. The far-field antenna characteristics aremeasured in an anechoic chamber, showing good agreement between simulated and measured results and a co- to cross-polarisation isolation better than 30dB.

For the fabrication of thin mechanically stable membranes on GaAs substrate new process steps have been developed. The SiN_x layers are deposited in a parallel plate plasma-enhanced chemical vapor deposition (PECVD) system. A 2µm layer thickness is suitable to support the patch metallisation. The stress in the SiN_x layer is reduced using multiplex RF frequency deposition.

After the deposition of the SiN_x layer, optical lithography is used to define the patches and microstrip lines. TiW/au is sputtered as a starting metallisation followed by a 3µm-thick electroplated Au layer. In the following the 625µm-thick GaAs wafers are thinned down to 150µm. Afterwards, the GaAs below the patches is removed by using wet chemical etching. Figure 3.3.7 shows a schematic cross section and a layer layout of a microstrip aperture coupled antenna patch on a thin SiN_x membrane.

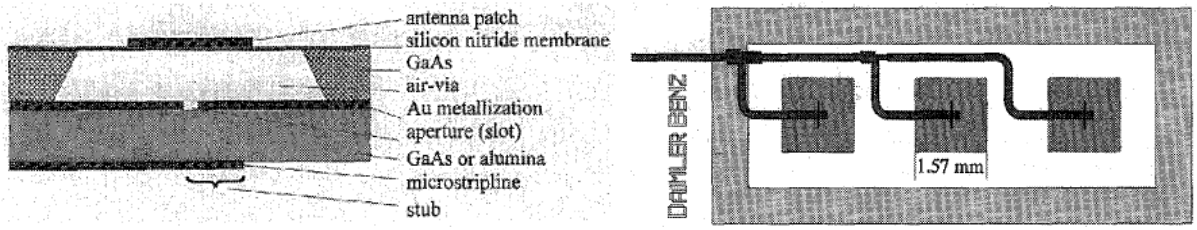


Figure 3.3.7: A 94-GHz Aperture-Coupled Micromachined Microstrip Antenna. (a) Schematic cross-section of an aperture-coupled antenna patch suspended on a thin SiN_x membrane. (b) Layout of layer of anaperture coupled 3×1 patch antenna array.

By using the developed technology, freestanding SiN_x membranes up to a size of 4.6×4.6 mm^2 are realized on GaAs wafers. The thermal stability of the membranes is tested over a wide temperature range from 77K up to 400K. Layers with tensile stress are destroyed when cooled down to 77K, while membrane antennas under small residual compressive stress withstand temperature cycles between 77K and 400K without any problems.

The resonant frequency of an aperture coupled triple patch antenna is determined to be 77.6GHz. The measured input reflection coefficient at that frequency is −44dB. The antenna shows very symmetrical patterns. The 3dB and 10dB main beam widths are 22° and 38°, respectively. Measured and simulated data show very good agreement. The cross polarisation isolation of the triple patch antenna is better than −30dB at 0°.

3.3.1.4 Silicon Proton Implantation

In the work of [181], antenna test structures were fabricated on standard Si substrate with a resistivity of 10Ωcm and a thickness of 260μm. A 500nm field oxide was grown before fabricating the antenna patterns using 1μm thick aluminum layer. Proton implantation was then performed on the patterned wafer with a fixed dose of 10^{15} cm^{-2} and at a fixed energy of 17.4MeV in a cyclotron chamber from the reverse side of the wafer.

The wafers were kept in a circular flange covered by aluminum sheet and implantation was done in six steps by changing the aluminum absorber thickness in order to provide a uniform proton profile throughout the entire depth of the Si substrate. The thickness of the aluminum absorber was 1630μm during the first implantation step. In each subsequent implantation steps, the thickness of the aluminum absorber was reduced by 40μm from the previous value. The implanted proton creates high defect density in Si, which effectively trap free carrier and increase resistivity. The measured resistivity of proton implanted Si was 0.1MΩcm.

The highest transmission gain for integrated dipole antenna on Si has been reported by [181], using an integrated antenna for ULSI on-chip wireless interconnection purpose. A 2mm long and 10μm wide dipole antenna pair at a distance of 1cm shows a transmission gain of 36.5dB at 18GHz, which is 20dB higher than previously reported gains.

This large increase in gain is achieved by proton implantation on Si substrate, which increased the resistivity from 10Ωcm to 0.1MΩcm. It is also found that transmission gain can be maximized for a given resistivity by optimizing the Si substrate thickness or by inserting a low-dielectric layer below the substrate.

In [182] the performance of integrated antennas on Si for possible application in wireless communications and wireless interconnects has been improved. For practical VLSI integration, the antenna size has been reduced and proton implantation has been optimized to a low energy of 4MeV with a depth of 175μm. To avoid any possible contamination, the ion implantation is applied after device fabrication. Excellent performance such as very low RF power loss up to 50GHz, record high 103GHz antenna resonance, and sharp 5GHz bandwidth have been achieved.

3.3.1.5 High-Resistivity Substrate Materials

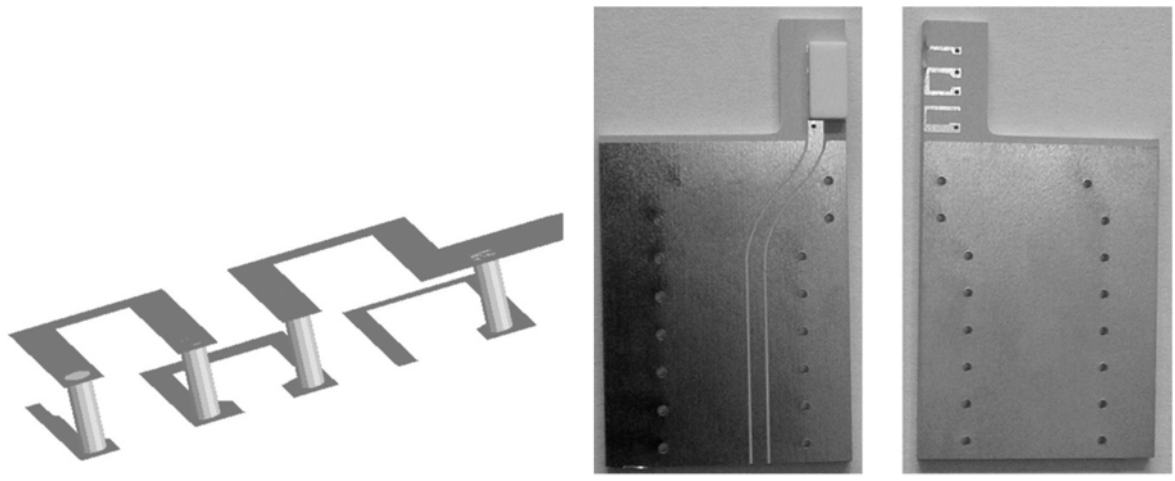
A millimetre-wave Finite Ground Coplanar (FGC) folded slot antenna on low-resistivity Si substrate (1Ωcm) with a polyimide interface layer is presented in [183]. The antenna resonates around 30GHz with a return loss of 14.6dB. Measured radiation patterns indicate the existence of a main lobe, but its radiation pattern is affected by a strong surface wave mode.

This antenna can be part of various low cost wireless communication systems used to transmit data from one chip to another. This wireless scheme is studied as an alternative to traditional conductor-based interconnects for future systems. Another application is the development of mm-wave, low cost phased-arrays on silicon that are traditionally built on GaAs substrates.

In [184], high-resistivity polycrystalline silicon wafers are utilized as low-loss substrates for three-dimensional integration of-on-chip antennas and RF passive components in wafer-level chip-scale packages. Sandwiching of HRPS and silicon wafers enables to integrate large RF passives with a spacing > 150μm to the conductive silicon substrate containing the circuitry, while providing mechanical stability, reducing form factor and avoiding any additional RF loss.

Antenna performance comparable to glass substrates and high quality factors for large spiral inductors (Q = 11 at 1GHz for 34nH) are demonstrated. The HRPS substrates have high dielectric constant, low RF loss, high thermal conductivity, perfect thermal matching, and processing similar to single crystalline silicon.

In [185], a novel chip-type ceramic dielectric antenna using the advanced meander-line technique for 2.4/5.8GHz dual ISM-band applications is proposed as shown in Figure 3.3.8. The proposed antenna is composed of small ceramic dielectric (8mm, 4mm, 1.5mm alumina) and substrate (thickness of 1.52mm, TMM-4). In order to minimize the antennas available area on the substrate and to reduce the coupling effect with the ground plane, the antenna is located at the corner of the substrate.



(a) (b)

Figure 3.3.8: Meander-line antenna on a dielectric ceramic chip. (a) Three-dimensional perspective view of the metal patterns. (b) Photographs of the antenna (top and bottom views).

The measured bandwidth and maximum radiation gain are 2.35−2.57GHz (VSWR < 2, 2.07dBi @ 2.44GHz) and 5.29−6.01GHz(1.17dBi @ 5.75GHz), respectively. From these results, it is demonstrated that this proposed antenna can be applicable to the dual-ISM band applications.

3.3.1.6 Active Antennas

Microwave antennas integrated with active elements or active antennas have found a wide interest in the last years. Most of them are transmitting antennas incorporating Gunn elements or field effect transistor (FET) oscillators; some of them are operated in a receiving mode. Due to the microwave frequency range, most active elements are based on GaAs. For mobile communication or local area network (LAN) applications, silicon still is the preferred material due to its mature technology and its compatibility with digital integrated circuits.

The increase in the bit rate or in the range and the reduction of the power consumption of future multimedia wireless terminals need high performances for RF front-end components including antenna. Thus, this element can be considered as an important part of the RF front-end and its characteristics have to be improved in the same way. Moreover, a rather recent tendency is the integration and the miniaturization of these devices. For example, a more and more frequent use of patch antennas or ceramic antennas can be noticed in RF interfaces.

The study of on-chip integration of a 10 GHz dipole antenna with a VCO using standard BiCMOS7^{TM} (0.25µm) STm technology has been carried out in [186]. The antenna configuration, which had been chosen, was a folded dipole, which allowed the reduction of the chip dimensions to 2.7 × 4.48mm. For a RF power injected from VCO to the antenna of −7dBm (0.2mW), the EIRW of antenna is about −15dBm. Thus the estimated value of antenna isotropic gain is about −8dBi. This result is consistent with simulation values of radiation efficiency of the order of 10%.

The antenna has been designed in BiCMOS7^{TM} STm technology. A 0.25µm bipolar-CMOS process has been used. The investigated antenna topology is a dipole structure. However, for this structure, the excitation is differential, which allows the use of active devices with differential output, and consequently avoid the common mode that needs a ground contact from the bottom of the chip, which is difficult to realize with a standard BiCMOS technology. The dipole is printed over the last aluminum metal layer having a thickness of 2.5µm. The substrate has the following characteristics; silicon substrate resistivity 15Ωcm (6.66 S/m conductivity), thickness of 350µm, oxide layer thickness 9.2µm. An Epitaxial layer, which is highly-doped silicon, of resistivity 0.6Ωcm (167 S/m conductivity) and thickness of 0.9µm between the two previous layers, is used. There is no ground plane in the bottom of the chip (see Figure 3.3.9).

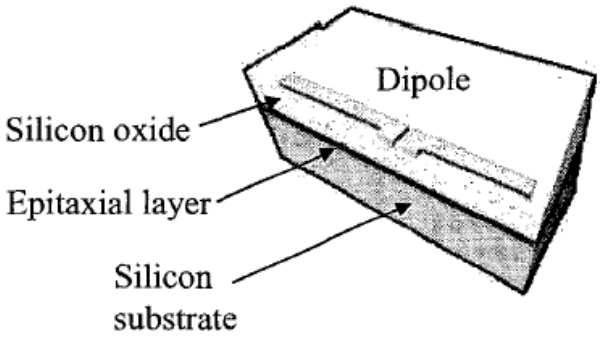


Figure 3.3.9: Dipole antenna configuration.

In the case of silicon substrate (ε_r = 12, h = 350μm), the first resonance is about 10GHz, for a simulated linear dipole of 3.4mm length of each arm, corresponding to an effective permittivity of 2.25. To obtain the same operating frequency with the folded dipole, the total unfolded length is adjusted to 3.8mm. It can be observed that folding the dipole structure does not significantly modify the resonance frequency.

The simulated radiation efficiency for an integrated dipole operating around 10GHz is investigated. If the epitaxial layer is omitted in the simulation, an efficiency of about 53% is obtained. This result agrees well with HFSS simulation, where the obtained efficiency is about 58%. Obviously for better radiation efficiency, the silicon should be highly resistive. Considering also the effect of low resistivity epitaxial layer, the radiation efficiency is then drastically reduced to about 10%. For a supply voltage of 2.5V, an available output power delivered by the VCO to each dipole arm is 0.1mW (−10dBm).

In [187], a millimeter-wave photonic integrated circuit (MWP-IC) on Si substrate is presented, which can be applied to millimetre-wave broadband communications and measurement systems. A millimetre-wave coplanar waveguide (CPW) and a patch antenna have been integrated with a photodiode on Si substrate. For this circuit, a high-output, high-speed InP/InGaAs uni-travel.

In order to reduce conductor loss, the CPW and patch antenna are made of thick Au. For the CPW, the loss due to the high permittivity and conductivity of the Si can be reduced by separating the CPW from Si. For the patch antenna, this technology allows to fabricate the antenna and circuit ground on the same substrate, which eliminates vias through substrate and complicated backside process.

The circuits were made on 2-inch high-resistivity (3kΩcm) Si wafers. The UTC-PDs were fabricated on a Si substrate by using full-wafer bonding. After removing the InP substrate, a conventional UTC-PD process was carried out. 10μm-thick Au CPWs and patch antennas were fabricated on a 30μm-thick interlayer dielectric. Polybenzoxazole (PBO) was used in the fabrication and has low dielectric constant (ε_r = 2.9) and positive photo-sensitivity. The maximum radiated power was ≈ 0.1mW at 120GHz.

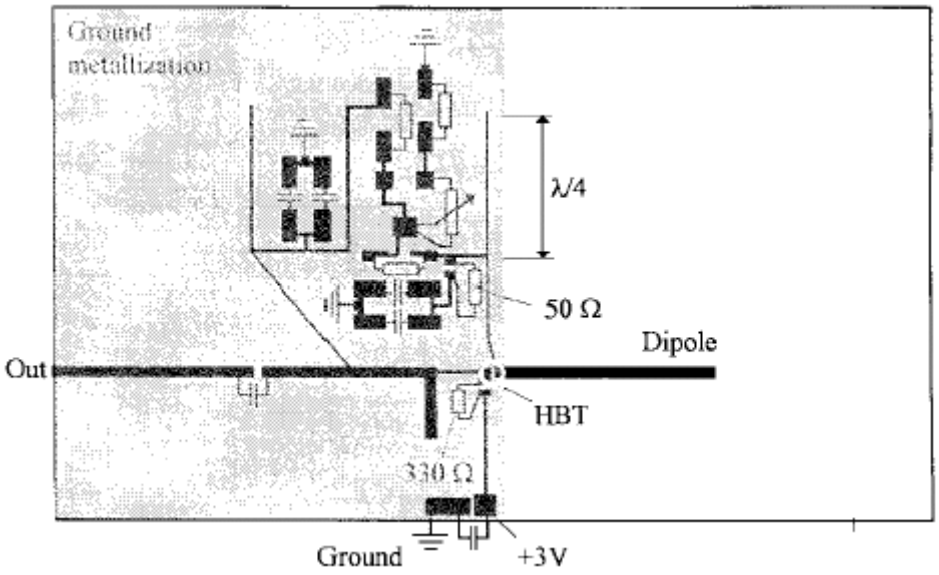


Figure 3.3.10: Basic layout of low-noise active receiving antenna using a SiGe HBT.

A low-noise active receiving antenna based on a printed dipole and a Si/SiGe HBT in the 5.8GHz band is presented in [188]. As an antenna element, a dipole was used printed on a thin dielectric sheet and placed a quarter wavelength in front of a metal plate as shown in Figure 3.3.10. In the area of the amplifier, an additional backside metallisation of the substrate is provided.

At 5.8GHz a power gain of 8.3dB compared to the respective passive antenna and a noise figure of 1.4dB at center frequency were achieved. To improve the antenna gain, two of these components were combined to a small array with reduced beamwidth and comparable noise figure.

A fully monolithic X-band twin-dipole antenna mixer consisting of a uni-planar twin-dipole antenna and a GaAsMESFET single gate mixer on the same GaAs substrate fabricated by monolithic microwave integrated circuit technology (MMIC) is reported in [189]. The total chip size is $5 \times 5mm^2$.

This circuit receives an RF signal of 10GHz and down-converts it to an IF signal of 1GHz with a worst-case conversion loss of 22dB, defined as the ratio of output IF power dissipated in a 50Ω load to the RF available power received by the twin-dipole antenna. The LO and RF signals are designed to be received by the twin dipole antenna and then applied to the input port (gate-to-source) of the MESFET, in which mixing operation is performed.

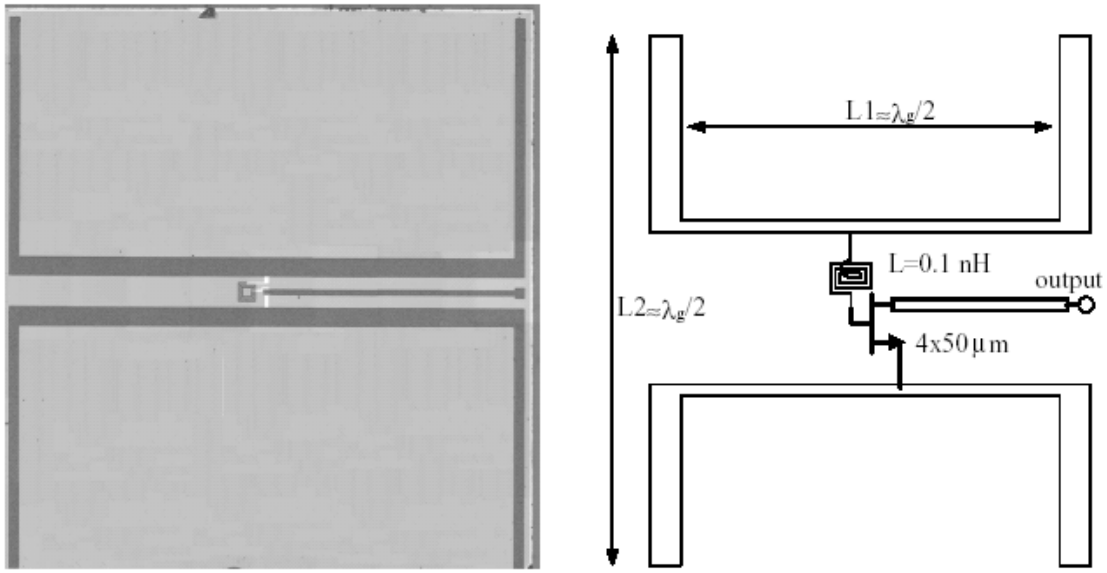


Figure 3.3.11: A fully monolithic integrated twin dipole antenna mixer on a GaAs substrate. (a) A photograoh of the integrated twin dipole antenna mixer fabricated by GaAs MMIC technology. The chip area is 5×5 mm^2. (b) Schematic of the integrated antenna with MESFET single gate mixer.

The desired IF signal is extracted from the output port (drain-to-source) of the MESFET. Specifically, the balanced RF signal is received by the two parallel dipole antennas spaced half wavelength apart and then fed to input of the FET through a pair of coplanar strips. The unbalanced IF appears at the output of the FET and is transmitted out by a coplanar waveguide transmission line.

Half wavelength rather than full wavelength dipole antennas were used in order to minimize the chip size. One reason that two dipole antennas are spaced half wavelength apart (see Figure 3.3.11) is to make the main beam of the resultant antenna pattern directed perpendicular to the GaAs substrate. Since the FET is located at midway between two-dipole antenna, the distance between the FET and one of the antennas is quarter wavelength.

The coplanar strips connecting the FET and two dipole antennas are used as quarter wavelength transformers to fulfill the impedance matching of the twin dipole antenna and the FET. This is the other reason that two dipole antennas are spaced half wavelength apart.

A 0.1nH inductor has to be inserted between the quarter wavelength transformers and the MESFET to resonate out the imaginary part (gate-to-source capacitance, C_{GS}) of the FET input impedance. The wavelength was chosen to be the free-space wavelength of a 10GHz signal. The single gate mixer is based on a 4-finger (total gate width 200μm) MESFET working at X-band with gate length 1μm. The FET is biased near the pinch-off region, where the nonlinear characteristics of drain-to-source current versus gate-to-source voltage are used. This whole circuit is built on one side of a 200μm thick GaAs substrate. Note that coplanar strip (CPS) and coplanar waveguide transmission lines are used, which allows fully uni-planar process technology and thus requires no via holes.

The experimental results demonstrate that this topology has potential applications in future low-cost millimeter-wave receivers for smart munitions seekers and automotive collision avoidance radars.

In [190], a new generation of Contactless Smart Card Chip is described which integrates an on-chip coil connected to a power reception system and an emitter/receiver module compatible with the IS0 14443 standard, together with an asynchronous quasi-delay insensitive (QDI) 8-bit microcontroller.

Beyond the Contactless Smart Card application field, this new chip demonstrates that system-on-chip, integrating power reception and management, radio-frequency communication, and signal processing, is feasible. It associates analog/digital parts as well as synchronous/asynchronous logics and has been fabricated in a CMOS six metal layers 0.25μm technology from STMicroelectronics.

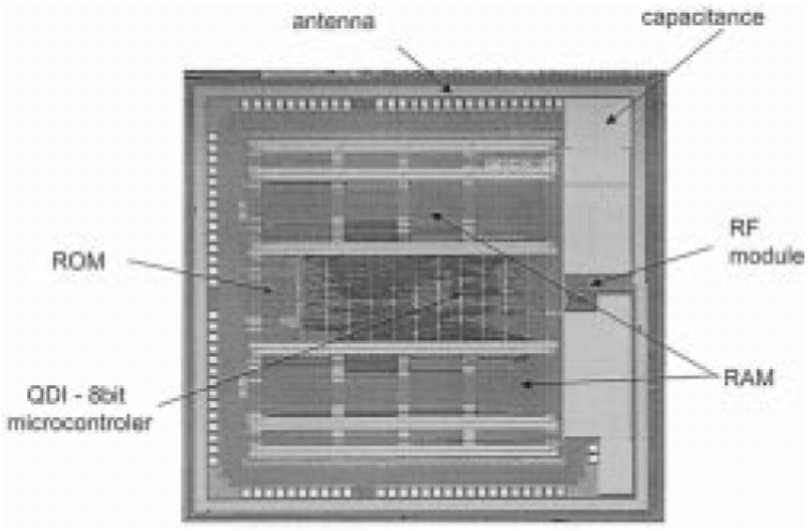


Figure 3.3.12: Chip micrograph.

The absence of contacts induces lower maintenance cost, improves ease of use, reliability, and, therefore, end-user satisfaction. They are declined in several types according to the location of the antenna. It can be on the card, on the module, or integrated directly on the chip. This later technique significantly decreases card fabrication cost. Moreover, as the user still inserts his card in a reader slot, transactions remain as safe as when using cards with contacts.

Since most applications require low-cost low-power systems, the goal of this work is to integrate on a single chip an antenna, an ISO14443 compliant radio-frequency emitter/receiver, together with an asynchronous microcontroller. Integrating the whole system on silicon should pave the way to new reliable low-cost Contactless Smart Card chips.

The Smart Card chip is composed of four main blocks as shown in Figure 3.3.12. The RF front-end recovers power at 13.56MHz from the integrated antenna, which forms a transformer with the external reader antenna. The recovered power is then stabilized and supplies the whole chip: the asynchronous microcontroller and a synchronous dedicated interface between the RF block and the asynchronous circuit. This interface is driven by a reception-enable signal (REN) controlled by the microcontroller.

In reception mode, the RF interface demodulates data sent by the reader. In emission mode, data are sent to the reader using a load modulation at an 847kHz BPSK rhythm. It is noticeable that the chip only consumes 800µW at 1V, still delivering a computational power of 4.3 MIPS. The total chip area is 16mm^2. The coil is made of six turns implemented with the upper five metal layers. Its area is 1.5mm^2.

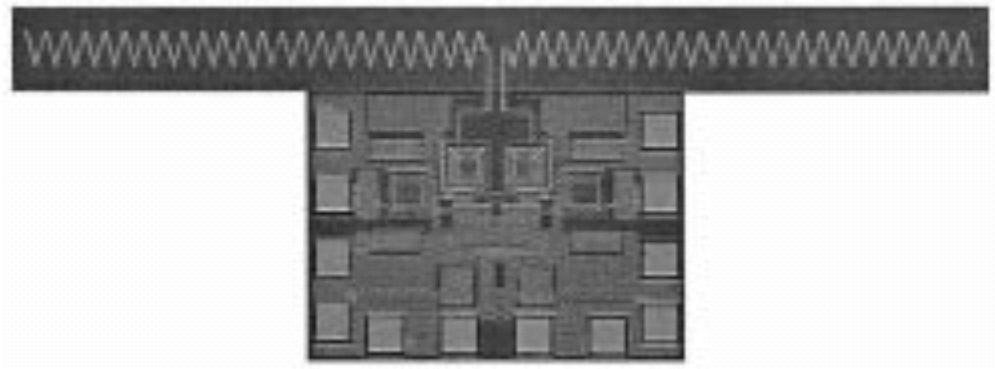


Figure 3.3.13: Die photograph of a 0.18 μm clock receiver with a 2 mm zigzag dipole antenna.

A wireless interconnect system which transmits and receives RF signals across a chip using integrated antennas, receivers, and transmitters is proposed and demonstrated in [191]. The transmitter consists of a voltage-controlled oscillator, an output amplifier, and an antenna, while the receiver consists of an antenna, a low-noise amplifier, a frequency divider, and buffers. Using a 0.18µm CMOS technology, this circuit is demonstrated at 15GHz on a substrate with a resistivity of 15−25Ωcm.

Wireless interconnection for clock distribution is demonstrated in two stages. First, a wireless transmitter with integrated antenna generates and broadcasts a 15GHz global clock signal across a 5.6mm test chip, and this signal is detected using receiving antennas. Second, a wireless clock receiver with an integrated antenna detects a 15GHz global clock signal supplied to an on-chip transmitting antenna located 5.6mm away from the receiver, and generates a 1.875GHz local clock signal.

The signal is generated on-chip at 8 times the local clock frequency and applied to an integrated transmitting antenna which is located at one part of the integrated circuit (IC). Since the microprocessor is extremely noisy at the local clock frequency and its harmonics, transmitting the global clock at a frequency higher than the local clock frequency provides an increased noise immunity for the system. Clock receivers distributed throughout the IC detect the transmitted signal using integrated antennas, and then amplify and synchronously divide it down to the local clock frequency.

Also, operating at a higher frequency decreases the required antenna size. The receiver is implemented in a fully differential architecture, which rejects common-mode noise (such as substrate noise), obviates the need for a balanced-to-unbalanced conversion at the input, and provides dual-phase signals to the frequency divider. These local clock signals are then buffered and distributed to adjacent circuitry.

The size of the receiver, including the antenna, is $0.66 \times 2\text{mm}^2$, while the active area is 0.37×0.58mm. The receiver consists of a zigzag dipole antenna, a differential LNA with source-follower buffers, an 8:1 frequency divider, and output buffers. Due to size constraints, the antenna is not designed to be resonant, hence its reactance is nonzero, and additional series inductance in the LNA is used to complete the match.

For on-chip antennas, the antenna size is limited by the size of the chip. Therefore, to maximize the antenna's radiation while limiting the physical size of the antenna requires operating at higher frequencies (e.g., 15GHz), corresponding to smaller λ.

The dipole antenna length has been limited to 2mm, corresponding to λ_{eff} / 5 and λ_{eff} / 3 at 15GHz, in silicon dioxide and silicon substrate, respectively. The zigzag antennas, illustrated in Figure 3.3.13, have a 10μm trace width, an 80μm arm element length, and a 30◦ bend angle. At 15GHz, transmission gain G_a is −53 and −45dB for 6.7 and 3.2mm separations, respectively.

3.3.1.7 Reconfigurable antenna using MEMS switches

Reconfigurable multi-band antennas are attractive for many military and commercial applications where it is required to have a single antenna that can be dynamically reconfigured to transmit or receive on multiple frequency bands. Such common-aperture antennas result in considerable savings in size, weight and cost. They find application in space-based radar, communication satellites, electronic intelligence, aircraft and many other communications and sensing applications. The reconfigurable antenna can be envisioned as an array of elements that are resonant at the highest operation frequency f_{max}, and that can be connected together using switches to form groups of elements that are resonant at several lower frequencies f_{max} / n, where n is a scale factor related to the element groupings.

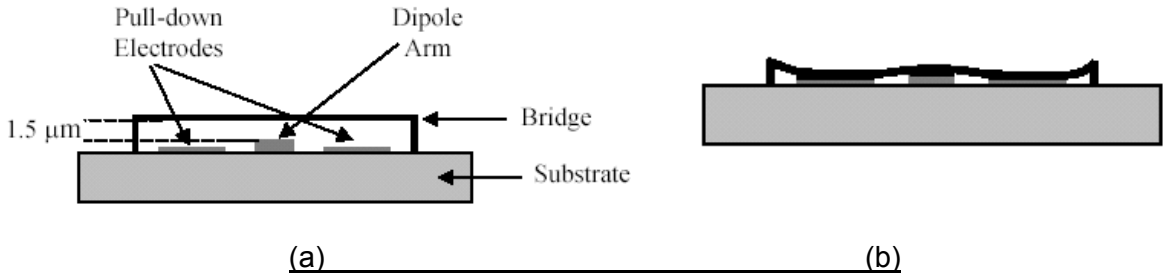


Figure 3.3.14: Schematic of the MEMS switch geometry for the reconfigurable antenna. (a) Geometry of the MEMS switch in up state. (b) Geometry of the MEMS switch in down state.

In [192], a reconfigurable dual-band 4.86 and 8.98GHz dipole antenna on silicon, using series MEMS switches, is presented. The reconfigurable dual-band dipole is firstly designed assuming ideal switches (ON/OFF). The effects of the two series MEMS switches on the antenna performance are studied. The design is performed using the 3D electromagnetic simulator HFSS.

The dual-band dipole antenna configuration consists of a High Resistivity Silicon (HRS) substrate (525μm) over which two layers of silicon dioxide and nitride are deposited SiO_2/Si_3N_4 (0.8μm/0.6μm). The dipole antenna is patterned on the topside of the wafer using a 0.2μm gold electroplating technique.

The series switch is composed of an all-metal gold bridge suspended 1.5μm over the dipole arm in the gap location. A gap of 80μm is defined in the line. The bridge length is 300μm, thickness 0.9μm, and width 120μm (thus insuring a 20μm overlap with the line from each side). The bridge is anchored at both sides.

Two pull-down electrodes are defined near both anchors of the switch and have an area of $55 \times 120\mu m^2$. In order to insure that the bridge makes good contacts with the line, the line is made 0.4μm thicker than the pull-down electrode. The insertion of the narrow line (30μm) reduces the up-state capacitance, due to fringing fields between the edges of the two main lines, and also provides better contact in the down state position (see Figure 3.3.14).

As can be observed, return loss of −10.3dB at 4.88GHz and of −23.8dB at 9.24GHz, are obtained. The bandwidth of the antenna is 2.3% at the lower frequency band, and is 13% at the upper frequency band. However, comparable to the case of ideal switches, a frequency shift of 0.4% and of 2.8% at the lower and upper frequencies, respectively, are observed. The antenna, including the two MEMS switches, has bandwidth of 1.9% and 13.6% at the lower and upper frequencies, respectively. The antenna radiation efficiency is 86% and the directivity is 2 dB at the lower band, and 94% and 3 dB at the higher one. As expected for a dipole antenna, the E-plane 3-dB beamwidth is wide and is equal to 84° at the low frequency, and 60° at the high frequency.

3.3.2 Butler Matrix for Millimetre Wave

Electronic scanning of an array antenna provides both high gain and angular resolution. At millimetre wavelengths however, the required phase shifters are costly, and introduce high loss. An alternative is to use a switched beam system, as shown in Figure 3.3.15 Providing that the combined loss of the switch matrix and beamforming network can be kept low enough, this may be a more cost effective solution.

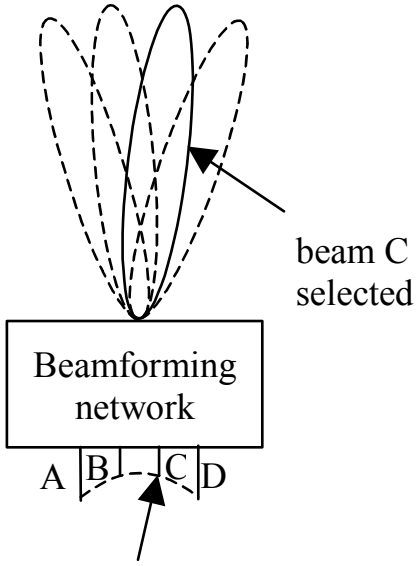


Figure 3.3.15: 4-beam system.

The beamformer can take several forms (for example, a resistive network, a quasi-optical system using a lens or reflector, a Blass network, or a Butler matrix). The latter is a well-known technique, but due to the complexity, size, and loss, is usually limited to a maximum of 16 or 32 beams. An example of a 4 × 4 Butler matrix without switching matrix, designed for operation at 63 GHz is shown in Figure 3.3.16. It is in microstrip form, and uses 0.005" thick Duroid 5880 substrate.

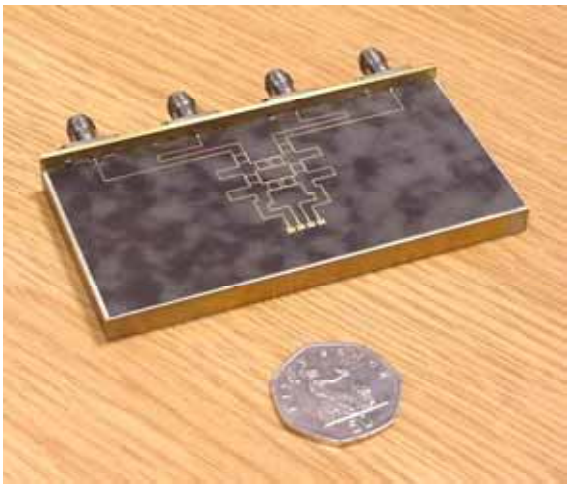


Figure 3.3.16: 4x4 millimetre wave Butler matrix.

The beams are selected by connecting to the V-connectors at the input of the matrix. The four outputs are connected directly to rectangular patch antennas. The loss in the microstrip was predicted to be approximately 10 dB. This high loss is partly due to the long input line lengths used in the model.

The losses can be reduced by using silicon micromachining to form a suspended membrane version of the network, as shown in Figure 3.3.17.

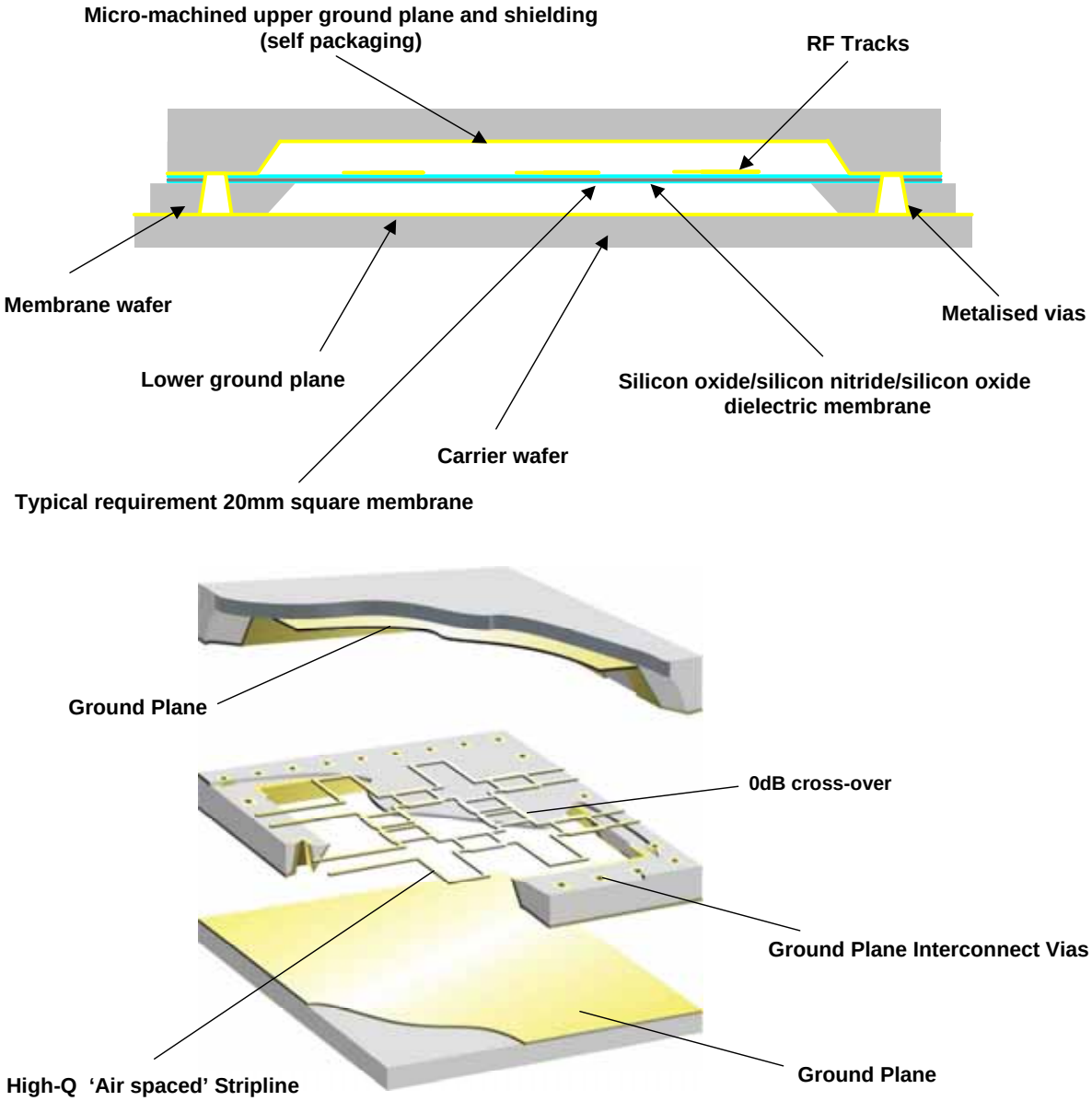


Figure 3.3.17: Model of micromachined Si form of Butler matrix.

As the structure is effectively air spaced, the dielectric losses are almost completely eliminated. Also, the copper surface produced by micromachining is much smoother that that of conventional microstrip, thereby reducing copper losses.

In order to provide a valid comparison, the micromachined model was made electrically the same length as the microstrip version. The predicted loss of the micromachined Butler matrix is approximately 2 dB, which is considerably lower than the 10 dB value predicted for the microstrip version.

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CHAPTER 4

STRUCTURING TECHNOLOGIES

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4. STRUCTURING TECHNOLOGIES

4.1 SUBSTRATES TECHNOLOGIES AND BULK DIELECTRIC MATERIALS

4.1.1 Soft and rigid substrates

4.1.1.1 Introduction

Soft substrates are used at microwave frequencies and up to millimeter wavelength to manufacture printed circuits and antennas. These kind of substrates are often based on PTFE and ceramic material. Fiber glass can be introduced to rigidify these substrates layers. Generally, a classical chemical etching is done to realise circuits and antennas. This kind of process allows an accuracy in the order of 10-20 micrometers.

On the other hand, conventional thin film processes (lift-off process and chemical wet etching) have been developed for the fabrication of antennas printed on fused quartz or alumina substrates. These rigid substrates are more suitable to realise active and integrated antennas because it's easier to report active devices (MMIC, MEMS, …) on these kind of substrates. In this case, Lift off process is often applied to realise circuits and antennas. Compared to chemical etching process, these thin film processes allow an accuracy in the order of a few micrometers, which is generally sufficient enough below 100 GHz

More details for these two substrates categories will be given in the following parts concerning substrates characteristics (tgδ, εr) and suppliers (particularly in Europe). Lift off process steps will be given to explain this particular technology.

4.1.1.2 Review of Soft substrates

Soft substrates are commonly used at microwave frequencies for producing beamforming networks and printed circuit antennas. Their advantages include being low profile, and relatively low cost. However, when used for printed circuit antennas, the resulting bandwidth is usually small (~2%), and the loss is relatively high when compared with other media such as waveguide. Loss is of paramount importance at conventional microwave frequencies, and is even more critical for passive millimetre wave antennas.

This report briefly reviews the properties of commonly used substrates. Factors affecting loss are discussed, and simulation and measured results are given for microstrip line losses at millimetre wavelengths. The information found in the open literature is also reviewed.

Commercially available substrates

A list of some of the more commonly used substrates is shown in Table 1, along with their loss tangents at microwave frequencies. Most of those listed have a low dielectric constant, as these are more suitable for printed circuit antennas. A large proportion of substrates are made from a mixture a PTFE and fibre glass. Whilst pure PTFE is very low loss, its mechanical properties make it very difficult to work with. To overcome this, fibre glass is added, either in woven form, or as random fibres. This has the unwanted effect of increasing the loss tangent.

Other types of substrates are used, such as those in the Rogers TMM series (e.g. TMM3 or TMM10). These are thermoset resin/ceramic composites, available in a range of dielectric constants. Such composites have an extremely low thermal coefficient of dielectric constant, typically 30ppm/°C. This is of considerable importance for air and land based vehicular applications, where the antenna may be subjected to temperatures in the -20° to +70° C range. Any frequency shift caused by thermal expansion/contraction must be tightly controlled as the bandwidth of the antenna is usually small. Dimensional stability is also important from the manufacturing point of view, especially for multilayer circuits. Other manufacturing aspects must also be considered. For example, TMM substrates do not soften with heat, making it suitable for applications requiring wire bonding.

Moisture absorbed by a substrate adds significantly to the loss tangent and therefore the loss of a microwave network or antenna. An example showing the effect on microstrip line losses is given in [22]. Unless steps can be taken to hermetically seal the antenna, the moisture absorption characteristic is one of the factors affecting substrate choice.

FR4 is also included in Table 4.1-1. Unlike the other substrates, its loss tangent is given at 1 MHz. FR4 is a generic name for a type of substrate that is readily available from a number of manufacturers. As such its properties are not tightly controlled, and it has a high loss tangent. However, it has been included as it is affordable, and is used for low frequency applications (below ~ 2 GHz).

It is often costs for high volume production environmental stability that dictate the choice of substrate, even though this leads to higher losses than desired. For example, an automotive radar at 77 GHz may use Rogers 3003 rather than 5880 [4], as it is a third of the cost and its dielectric constant is stable over a wide temperature range. However, its loss tangent is 40% greater (at 10 GHz).

To summarise: before a substrate is chosen for a particular application, several factors should be taken into consideration, including:-

- Substrate size, cost, and availability
- Processing costs/ease of manufacture
- Dielectric constant and loss tangent

- Environmental stability (thermal expansion, water absorption etc.)

Information on standard microwave laminates at microwave frequencies can be found on the web at sites such as [1], whilst a searchable database is available at [2].

Supplier	Product	Composition	Dielectric Constant	Loss Tangent
Rogers	Ultralam 1217	PTFE/ Woven Fibreglass	2.17 ± 0.02	0.0009
Arlon	IsoClad 917	PTFE/Non-Woven Fibreglass	2.17, 2.20 ± 0.04	0.0010
Taconic	TLY	PTFE/Woven Fibreglass	2.17-2.40 ± 0.02	0.0010
Rogers	RT/Duroid 5880	PTFE/Non-Woven Fibreglass	2.20 ± 0.02	0.0009
Rogers	RT/Duroid 5870	PTFE/Non-Woven Fibreglass	2.33 ± 0.02	0.0013
Rogers	Ultralam 2000	PTFE/Woven Fibreglass	2.40-2.60 ± 0.04	0.0019
Rogers	RT/Duroid 6002	PTFE/Ceramic	2.94 ± 0.04	0.0012
Arlon	AD 300	Commercial Grade PTFE	3.00 ± 0.05	0.003
Rogers	TMM 3	Thermoset Resin / Ceramic	3.27 ± 0.016	0.002
Arlon	25FR	Thermoset Resin with Ceramic filler	3.43 ± 0.08	0.0035
Metclad	MCX-348	PTFE/Woven Fibreglass/Ceramic	3.48 ± 0.04	0.0035
-	FR4	Glass Epoxy	4.34@1GHz	0.016 @1MHz
Rogers	TMM 6	Thermoset Resin / Ceramic	6.00 ± 0.080	0.0023
Rogers	RT/Duroid 6006	PTFE/Ceramic	6.15 ± 0.15	0.0019
Metclad	MNX8	PTFE/Non Woven fibreglass/ ceramic	8.50 ± 0.2	0.003
Rogers	TMM 10	Thermoset Resin / Ceramic	9.20 ± 0.23	0.0022
Rogers	RT/Duroid 6010LM	PTFE/Ceramic	10.2 ± 0.25	0.0023

Table 4.1-1: Sample characteristics of substrates at X-band.

Suppliers in Europe

ROGERS, ARLON and TACONIC are american corporation but with possibility to buy products in Europe. METCLAD (NETLEC is the new name) is a french supplier of substrates (Neltec Route des Usines - 65300 LANNEMEZAN).

4.1.1.3 Review of Rigid substrates

Traditional substrates for millimetre wavelength applications tend to be either 0.005" thick Alumina or Quartz. They have very low loss tangents, and are suitable for integration with active devices. Standard substrate sizes are 1"x 1" or 2"x 2", although 4" x 4" substrates are available. Whilst Alumina and Quartz have attractive electrical properties, thin substrates made from them are relatively fragile and more difficult to work with compared to soft PTFE based substrates, especially when electrically large antennas are required.

Conventional thin film processes (lift-off process and chemical wet etching) have been developed for the fabrication of antennas printed on fused quartz or alumina substrates. As an example, Figure 4.1-1 summarizes the main technological steps involved in the lift-off process of single layer microstrip antennas.

These thin film processes allow an accuracy in the order of a few micrometers, which is generally sufficient enough below 100 GHz, excepted for particular cases such as resonant frequency selective surfaces or planar metamaterials. Nevertheless, we should mention that the accurate fabrication of antennas and associated feeding network requires to control the uniformity of (i) the photoresist spin-coating and development, (ii) and the metal deposition (thickness and temperature) and etching over the whole surface of the wafers.

Similar techniques are developed for the fabrication of multi-layer structures. In that case, the main problem consists in the alignment and adhesion of both substrates. Specific *wafer bonding techniques*, based on Indium or Photo-resist adhesion thin films, have been proposed in [23]. The advantages of these techniques are threefold: they compatible with low-temperature processes, the additional losses induced by the adhesion films are negligible, they guaranty the absence of any residual air gaps whose consequences on the electromagnetic performance could be dramatic [24].

The thickness of the fused quartz and alumina at 60 GHz typically varies between 100 and 200 µm. Their relative permittivity and loss tangent are 3.80 and $3x10^{-4}$, and 9.6 and $5x10^{-4}$, respectively.

Metallic layers are typically composed of Au, Al or Cu with Ti or Cr adhesion layers. Their thickness varies from 1µm and 3µm.

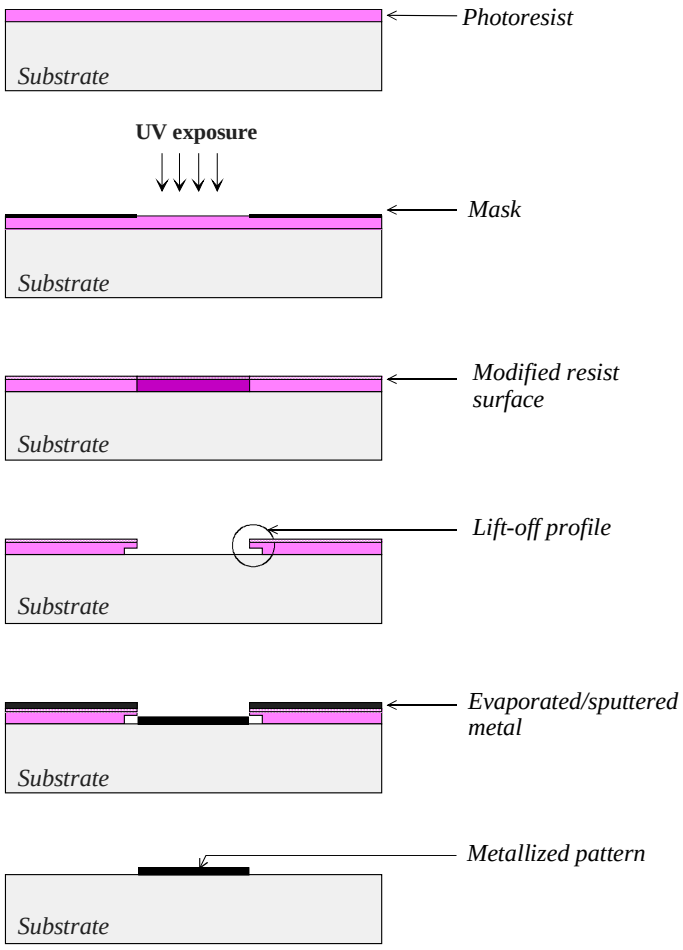


Figure 4.1-1 : Lift-off process of sputtered copper films

Quarts suppliers

HERAEUS QUARTZ GLASS in Germany for headquarters and production in UAS, Great Britain, Japan, China and Korea.

ALUMINA supplier

KYOCERA FINECERAMICS GMbH in Germany.

4.1.1.4 Multilayer technologies / thick ground plane added

LTCC Technology

The most well known multilayer technology is LTCC (**L**ow **T**emperature **C**ofired **C**eramic). The **L**ow **T**emperature **C**ofired **C**eramic (LTCC) technology can be defined as a way to produce multilayer circuits with the help of single tapes, which are to be used to apply conductive, dielectric and / or resistive pastes on. These single sheets have to be laminated together and fired in one step all. This saves time, money and reduces circuits dimensions. An other great advantage is that every single layer can be inspected (and in the case of inaccuracy or damage) replaced before firing; this prevents the need of manufacturing a whole new circuit. We don’t give more any details in this part chapter because the LTCC technology is developed and explained in chapter 3 of this technology assessment report.

A description of technology steps is given on the following picture :

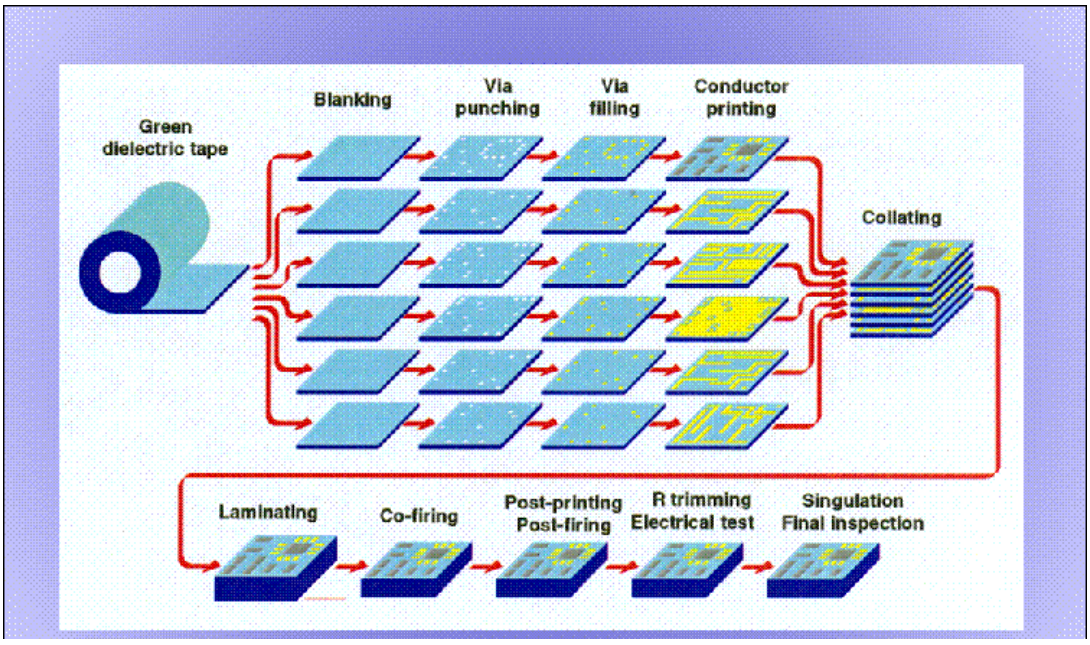


Figure 4.1-2 : LTCC technology

LTCC suppliers :

The following companies offer LTCC tapes for various applications.

DuPont, Ferro, Heraeus, CeramTec, ESL Electro-Science, Kyocera, Nikko, Northrop Grumman

Samsung

Substrate and thick ground plane / commercial consideration

In addition to conventional one or two sided copper foil clad substrate, laminates are also available with a thick metal laminated to one side and copper foil on the other. This thick metal serves as ground plane for stripline and microstrip circuit boards.

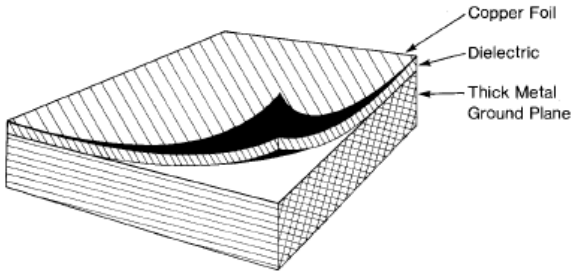


Figure 4.1-3 : Substrate with thick support

Active and passive components , such as diodes and resistors, are mounted directly on the ground plane in slots or blind machined through the dielectric. For example conventional die attach methods using eutectic silicon gold or conductive epoxies may be used to bond transistors to the plated ground plane. Electrical connections are made by the well known processes of wire bonding, ribbon bonding or soldering. Moreover, the thick metal ground plane provides a rigid base attachment when substrates are very thin in millimeter wavelength.

Suppliers

ROGERS Corporation :

Thick ground planes can be done in Copper, Brass or Aluminium with thipical thickness comprised between 0.02 inches and 0.5 inches. The using substrates are PTFE composites such as RT/duroid 5880 or ceramic PTFE such as RT/Duroid 6010.

An example is given as follow for a power amplifier circuit on brass-clad RT/Duroid 6010.

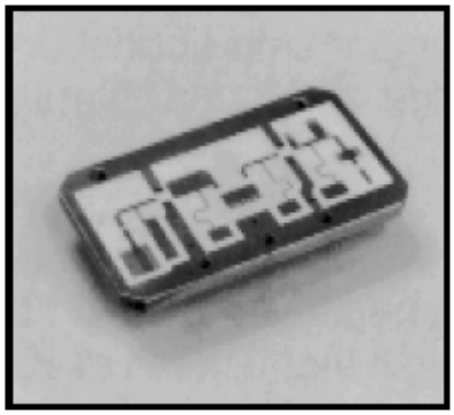


Figure 4.1-4 : Power amplifier on Brass-clad Rt/Duroid 6010

NELTEC CORPORATION/ subsidiary of Park Electrochemical Corp.

Similar technologies with thick ground planes and substrates layers have been developed in IETR laboratory and in collaboration with industrials. These technologies are explained in following part. Moreover, it allows to realise multilayer antennas and circuits

Multilayer technology with thick ground plane developed by IETR laboratory

IETR institute works on 2D technology antenna and associated circuit. For low-dielectric constant substrates, very similar technologies have been developed to realise passive and active antennas. The objective is to separate feeding line network layer to radiating elements layer. These technologies allow to avoid spurious radiation due to feeding line and active components.

Some studies have been done up to 60 GHz using:

- low-permittivity soft substrates such as Glass Teflon, TPX (Polymethyl-Pentene) or Polypropylene.
- and rigid substrates such as fused quartz and alumina materials.

Both technologies are described below.

Multilayer technology with polypropylene substrate

This technology has been developed in collaboration with CNET and after with a local company Avi-Peschard [25, 26, 27] in France. In this kind of technology, a thick metallic support can be introduced between the different substrates layers to rigidify the circuit and allows to report active components (MMIC). To realise the multilayer circuits, several sheets of substrate are stacked and pressed at high temperature to obtain correct polypropylene thickness (0.25 mm to 1.6mm or more). Low cost is a real advantage of this technology.

The fabrication of polypropylene printed circuit boards is a very simple procedure. Two types of board are condidered :

Polypropylene of different thicknesses (ranging 0.25mm to 1.6mm or more) are manufactured by heating polypropylene granules to the melting point (170°) and pressing them. Pressure and cycles are described in the following table. Copper foil or thick mettalic support is first chemically processed and then laminated to the polypropylene – based – dielectric by the same procedure.

Thick backing construction offers significant advantages over conventional designs :
If a thick ground plane is added, significant advantages are interesting :

- It provides high reliability for connector mounting,
- For high power applications heat generated by devices can be dissipated,

Because the substrate is not loaded with fiber glass, it tends to warp when internal stress between copper and polypropylene is too high; a thick metal cladding can insure flatness. The same process can be extended to multilayer structures (table 4.1-3) :

RF characteristics of polypropylene in low frequencies : $\varepsilon r = 2.18$, $\tan \delta = 0.001$, cost (low).

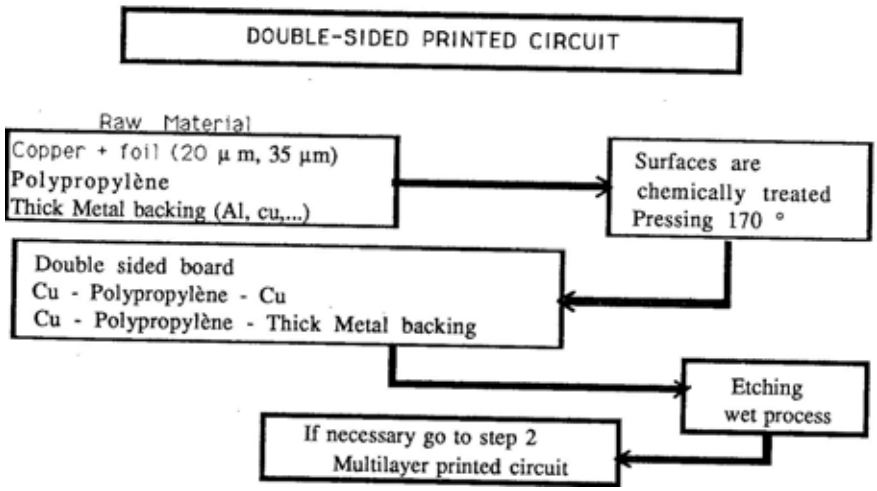


Table 4.1-2 :

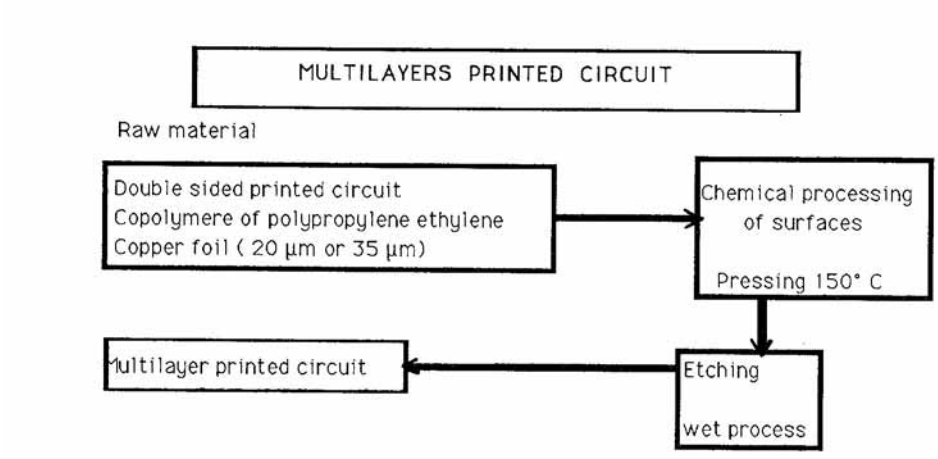


Table 4.1-3 :

Multilayer technology with TPX substrate and polypropylene

A very similar process is employed for polymethyl pentene substrate (better in millimeter waves). An example of multilayer circuit is described on figure 4.1-5 where a slot full of TPX allows to connect the different layer by electromagnetic coupling.

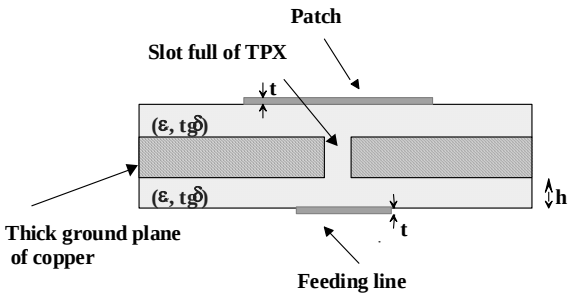


Figure 4.1-5 : Multilayer TPX technology

Multilayer technology with glass teflon substrate

This technology has been developed in IETR laboratory [4] and compared with the precedent technology based on TPX substrate. In term of realisation, the initial copper film is first removed and after the two substrate layers are stuck and pressed at high temperature. It needs to oxide metallic support to stick substrate layers on this thick plane (figure 4.1-6).

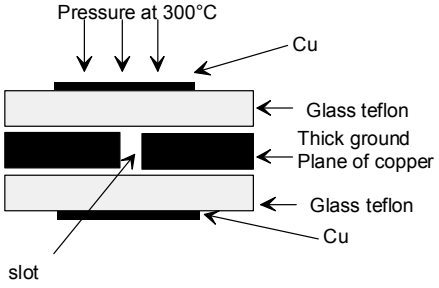


Figure 4.1-6 : Multilayer Glass teflon technology

4.1.1.5 MULTILAYER PANELS

For enhanced electrical properties (reduced losses, extended bandwidth,…), and for mass reduction optimisation, there is often a need to use low dielectric constant materials for a multilayer microstrip antenna. In this case, spacer layers are required which are sandwiched between thin dielectric layers on which patches are etched.

A typical embodiment can be :

- Kapton-copper foils with a Kevlar/resin stiffening layer for the thin dielectric layers (to support the patches or the microstrip lines)
- Honeycomb or Foam separators for the spacer layer

The sandwich is then mounted on a carrier Sandwich plate, which is designed to meet the mechanical requirements. In this case, the stiffness and electrical layers are separated

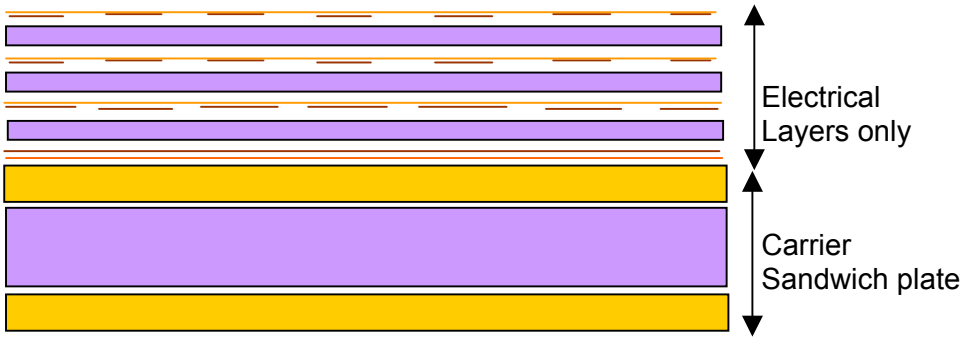


Figure 4.1-7 : Separation of the electrical and stiffness layers

Another approach can consist of distributing the stiffness layer within the electrical panel. For this case, the thickness and consequently the mass of the panel can be reduced. This may however result in higher losses, since high stiffness materials do not have often optimized electrical properties.

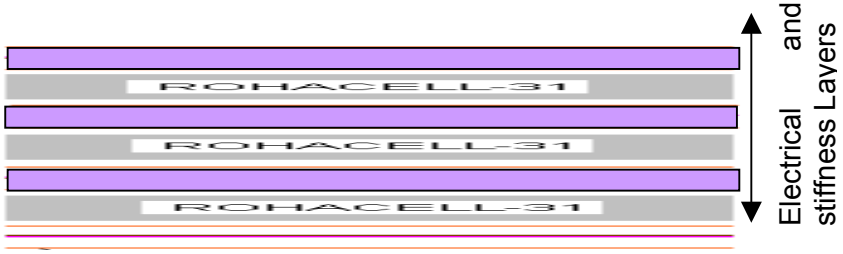


Figure 4.1-8 : Distribution of the stiffness layer within the electrical layer

An alternative option may be to distribute the stiffness layer within the electrical layer, and to keep a consistent carrier layer.

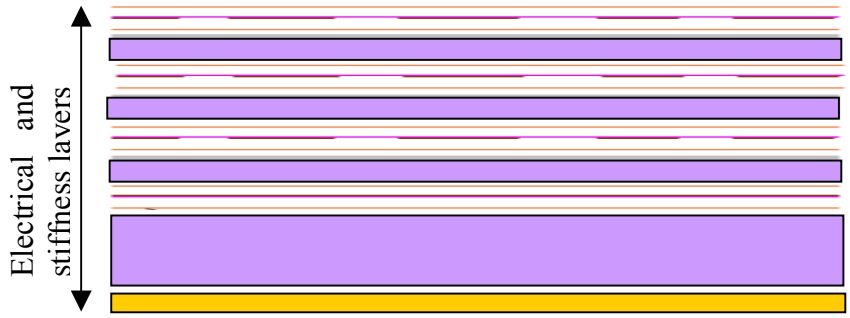
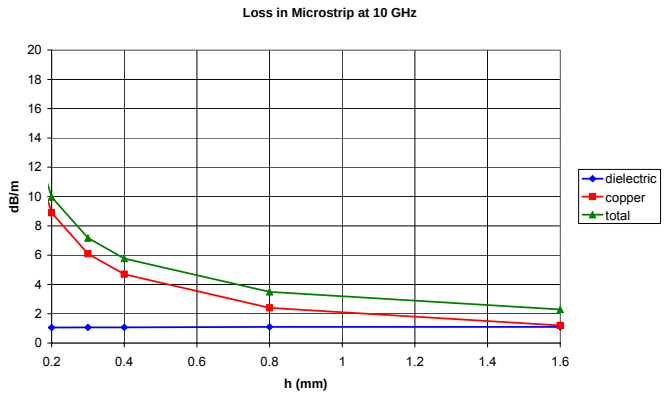


Figure 4.1-9 : Combined approach

The choice between these concepts depends on the mechanical and electrical requirements. Mixing the electrical and stiffness layers should be more attractive in terms of mass, but it may also results in higher losses.

4.1.1.6 LOSS MECHANISMS

Although substrate losses (tgδ) were considered in the previous Section, copper losses must also be considered, especially at millimetre wavelengths where thin substrates must be used. To see this, consider Figure 4.1-10. This shows how the loss in a 50 Ohm microstrip line varies as a function of substrate thickness at 10, 60 and 100 GHz, as calculated by LINECALC [5]. In the simulation, a surface roughness of 1.9 microns was used. Also, the loss tangent at 60 GHz and 100 GHz is assumed to be 4 times greater than that at 10 GHz, based on values presented in [7].



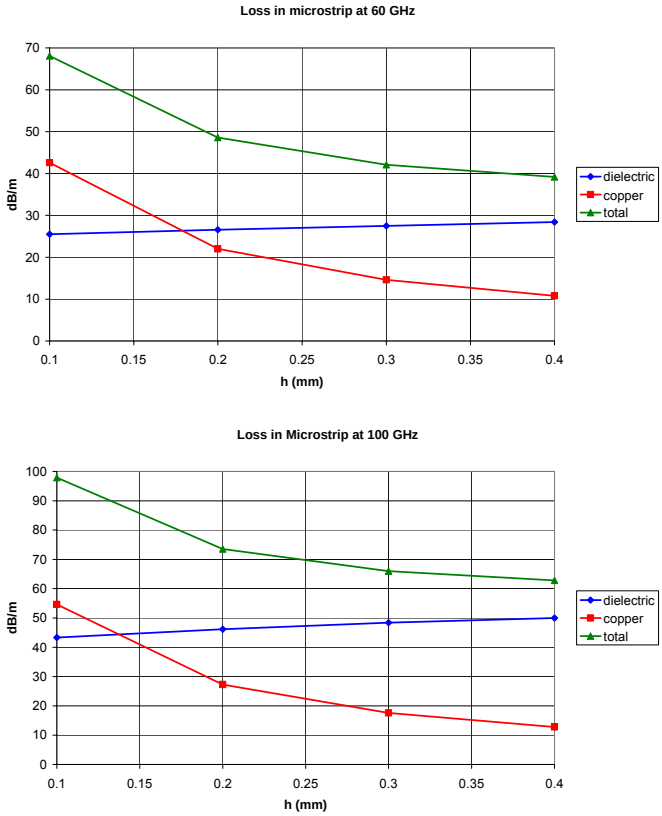


Figure 4.1-10: Trends in microstrip loss

As can be seen, at 10 GHz the copper losses dominate for small substrate thicknesses. However, at a sufficiently large frequency the dielectric loss eventually dominates. This is because the dielectric loss is proportional to frequency, whilst the copper loss is proportional to the square root of the frequency.

Figure 4.1-10 suggests that large thicknesses should be used to reduce losses. However, this leads to unwanted radiation/generation of surface waves from discontinuities. In order to avoid this problem at millimetre wavelengths, very thin substrates must be used. As an example, consider the contributions to the quality factor of a half wave resonator at 60 GHz. There are three contributors to the total quality factor: dielectric, copper, and radiation losses. As can be seen from Figure 4.1-11, the dielectric loss is almost constant with substrate height. The copper loss however, increases as the substrate thickness decreases, and the radiation loss shows an opposite trend. This results in the total quality factor Q_t peaking at a specific substrate thickness. For the example shown, the optimum thickness is extremely small. However, the Figure is indicative only, as it applies to a half wave resonator, and no consideration is given to the effects of packaging. A typical thickness used at millimetre wavelengths is 0.1 mm.

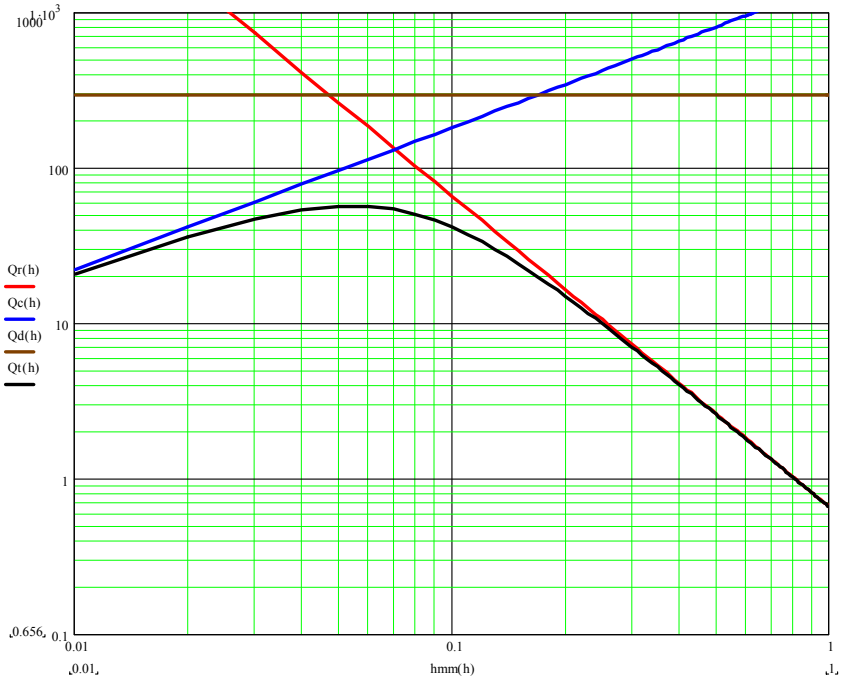


Figure 4.1-11: Q-factor for half wave resonator at 60 GHz

Review of substrate properties at mm wavelengths

A useful review of dielectrics and their electrical properties at millimetre wavelengths is given in [3] and [20]. However, these dielectrics are ‘pure’, in the sense that they are not the PTFE/fibre glass or resin/ceramic composites that are commercially available. Results given in the literature are therefore of limited interest to engineers designing practical circuits. Very little is published on the properties of commercial substrates at millimetre wavelengths. Usually the microwave designer must build and test their own circuits in order to determine dielectric constants and losses. As an example of the latter, the loss of a 100mm long 50 Ohm microstrip track on 0.1 mm thick RT/Duroid 5880 was measured to be 50 dB/m at 60 GHz (see Figure 4.1-12). As total loss was of most interest, no attempt was made to measure the separate loss contributions due to the dielectric and copper.

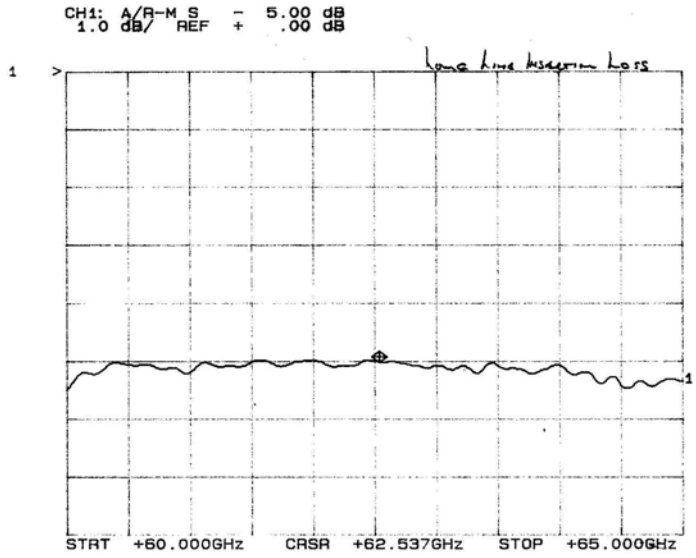


Figure 4.1-12 : Measured loss of 100mm line

For the case shown in Figure 4.1-12, LINECALC predicts 63 dB/m, assuming a surface roughness of 1.9 microns, and a loss tangent of 0.004 (4 times that at 10 GHz). Note that software packages commonly used to design circuits (e.g. HFSS) are usually unable to model surface roughness effects.

Once a dielectric substrate has been chosen, the dielectric loss is fixed. However, copper losses can be reduced somewhat. Particularly important is the surface roughness of the copper, especially the surface in contact with the substrate. For RT/Duroid 5880 this is 1.9 microns, and is rougher than the other surface, improving the adhesion to the substrate, but adding to the copper loss. Using rolled/annealed copper instead of electro-deposited copper reduces surface roughness and leads to a modest reduction in copper loss.

For a passive printed antenna array, as the size increases, so do the beamformer losses. These losses can be substantial. For example, Figure 4.1-13 shows the effect of beamformer losses, assuming a microstrip corporate feed network and a loss of 50 dB/m at 77 GHz.

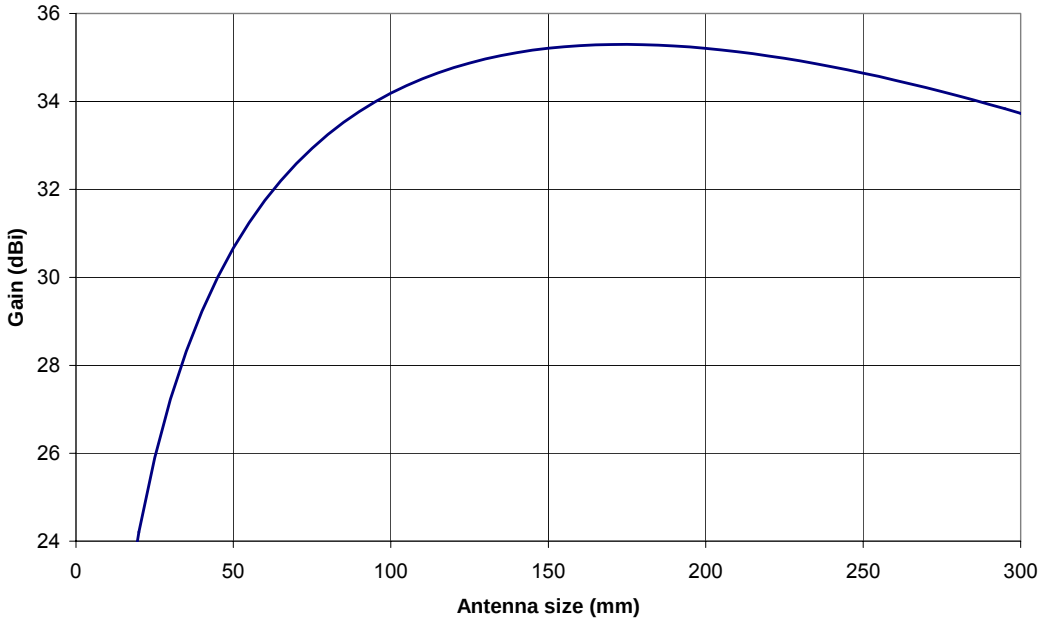


Figure 4.1-13: Gain vs. size of an array fed by a microstrip corporate beamformer at 77 GHz

As can be seen, the beamformer losses mean that there is no advantage (in gain) of making the array more than 150 x 150 mm in size. To increase the achievable gain, a lower loss feed network (e.g. a series feed, or an alternative transmission line structure) is required.

An example of a planar array of 8x10 microstrip patches operating at 63 GHz is shown in Figure 4.1-14 [8]. The array is approximately 40 x 30 mm in area, and is printed on 0.005" RT/Duroid 5880 substrate. In order to reduce copper losses in the beamformer, a series feed is used to excite each row of the array. The gain was measured to be 18 dBi, which was significantly lower than the predicted value. This is thought to be mainly due to the inadequacies of the model, which did not include surface roughness for the copper, and possibly an underestimate of the loss tangent (the manufacturer's quoted value at 10 GHz was used).

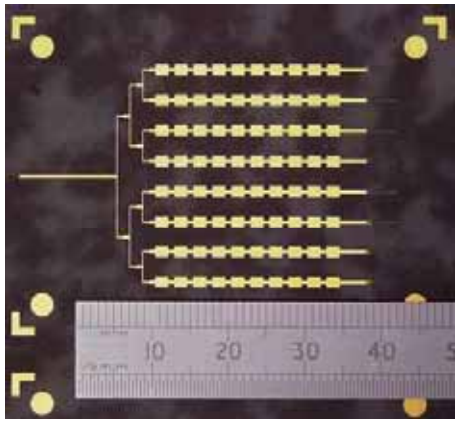


Figure 4.1-14: 63 GHz microstrip patch array

Experience has shown that losses for microstrip are generally in line with predictions given by programs such as LINECALC at low microwave frequencies, as long as surface roughness is taken into account. Excess loss is sometimes found, and this can usually be attributed to the manufacturing process, or to the influence of the environment. For example, it may be necessary to nickel plate small areas of track in the vicinity of connectors. Also, even for substrates such as Rogers 5880 which has low water absorption characteristics, significant reductions in line losses can be achieved if the substrates are baked in an oven to remove excess moisture. This indicates that for production, such devices need to be hermetically sealed to prevent moisture absorption during the device's operational lifetime.

Recently, liquid crystal polymers (LCP) have emerged as an alternative substrate material for microwave and millimetre wave applications. They are low cost, have very low moisture absorption characteristics, and can be formed into flexible circuits.

Characterisation of LCP at millimetre wave frequencies (30-110GHz) using microstrip resonator techniques indicate that the dielectric constant is constant at about 3.16 with a loss tangent of below 0.0049 throughout the lower millimetre wave band. It is envisaged that LCP will find increasing application for integrated systems and will be competitive with other materials for high-volume cost effective manufacture of millimetre wave devices and components [21].

At millimetre wavelengths, losses are usually higher than those predicted using data supplied by the manufacturer (quoted values of loss tangent are often given at 10 GHz). Experience gained with liquid crystal polymer (LCP) substrates (e.g. R/flex 3000 series from Rogers) tends to confirm this. The loss of microstrip using 100 micron thick R/flex 3850 substrate with a 50 micron protective covering of R/flex 3850 has been derived from resonator measurements, and the results are summarised and compared against theoretical predictions in Figure 4.1-15. The closest prediction to the measured values is provided by LINECALC (NB. LINECALC does not include a model for embedded microstrip). The prediction is based on the standard microstrip model, with no allowance made for the covering layer. The results show that at 24 GHz the measured loss is 30% greater than predicted by LINECALC, and this difference is likely to increase at millimetre wavelengths.

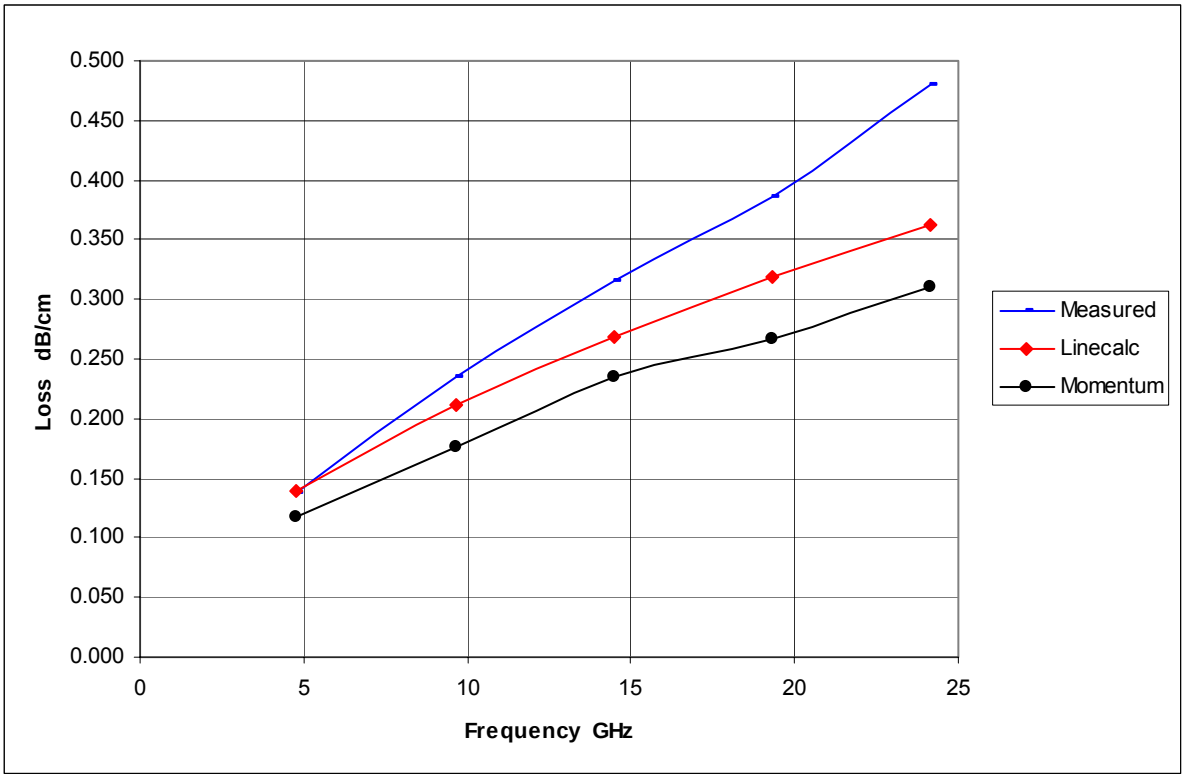


Figure 4.1-15: Loss results for microstrip using LCP substrate

Packaging may also influence the choice of substrate. For example, traditionally, an active array antenna may use separate T/R modules with their own metal enclosure, alumina substrate, and connectors. These then have to be connected to an antenna and beamformer on another substrate. This is obviously a high cost, high mass and volume solution. As an alternative, a number of companies are investigating chip on Duroid type solutions. Chip on Duroid solutions avoid much of the mass and cost by integrating one or more T/R modules (without metal enclosure) onto the beamformer substrate directly. However, significant challenges need to be met. For example, RT/Duroid 5880 is soft, making wire bonding difficult. A better alternative may be RT/Duroid 6002 or 6202. Harder substrates such as thermoset resin RT/Duroid 4350B can be used in place of 5880, as it lends itself better to the multi-layer processes required by T/R module components. However, its electrical properties may not be good enough at millimetre wavelengths.

Characterisation of Substrates at Millimetre Wavelengths

The characterisation of substrates is of paramount importance in the design of antennas and devices at microwave and millimetre wave frequencies. The important parameters for substrate characterisation are the dielectric constant and loss tangent. Both parameters are generally slowly varying functions of frequency. However, as material parameters are often quoted at 10 GHz, it is important to accurately characterise the substrate properties at millimetre wavelengths.

In the characterisation of substrate materials, a number of measurement processes can be applied. The most common involve the use of a waveguide cavity or microstrip resonators (rings or strips). For the latter, it can be difficult to accurately separate out the substrate losses (and hence obtain an accurate loss tangent) from copper and radiation losses. This technique of printed resonator has been used in IETR to characterise nitride Alumina substrate and result of magnitude S21 parameter is presented on figure 4.1-16. This picture shows the resonant frequencies between 2 and 60 GHz. From the resonant frequency, it become possible to find the dielectric permittivity. For this example, closed to 50 GHz, εr = 8.5 compared to 9 for supplier data [9].

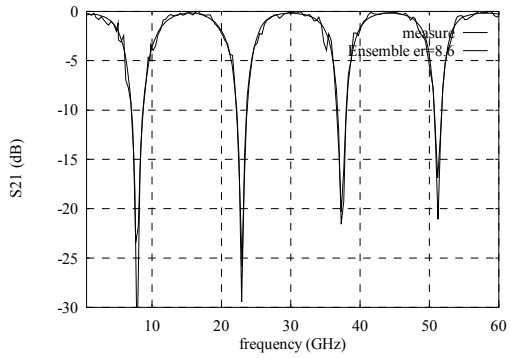


Figure 4.1-16: Printed open stub resonator (S21 result)

An other example concerns TPX substrate which is used by IETR for multilayer technology.

The Polymethyl-Pentene (TPX, Goodfellow catalogue) is a plastic material with these characteristics at 10 GHz :

tg δ = 0.001 and εr = 2.14

This substrate has been characterised at 60 GHz (for indoor communication application) and the results are **tg δ = 0.0035 and εr = 2.17**.

Concerning RT/Duroid 5880 (Rogers corporation), a similar technique has employed to characterise it. Supplier datas are : tg δ = 0.001 and εr = 2.2. This substrate has been characterised at 60 GHz and **tg δ = 0.004 and εr = 2.24**.

Finally, results concerning neltec PTFE substrate (MYST-220(MY2). : tg δ = 0.001 and εr = 2.2) are given at 60 GHz : **tg δ = 0.005 and εr = 2.26.**

At millimetre wavelengths, quasi-optical methods such as the open resonator technique are the preferred choice for the characterisation of substrate properties. This is largely due to the losses in the cavity walls resulting in poor Q (quality factor) values [11]. In the measurement process, the frequency variation technique or the cavity length variation technique can be used. The frequency variation technique employs a fixed cavity length and frequencies are scanned to determine the resonance frequency difference and the Q of two respective resonance peaks with and without the material specimen. The permittivity and loss tangent are

subsequently determined. For the cavity-length variation technique, the cavity length is initially set to a fixed value, and then changed to determine the resonance length difference and the Q-factors of two peaks for the calculation of the permittivity and loss tangent. Recently, new improvements to the cavity length technique to enable more accurate measurements have been reported [12], [13], [14]. A lot of results have also been given in the following table 4.1-4 by AFSAR.

MILLIMETER-WAVE DATA OBTAINED WITH OPEN RESONATOR SYSTEMS

Material	λ(mm)	Freq(GHz)	n	ϵ'	$\tan\delta$ (μ rad)	Ref.
Alumina	8.834	33.906	3.119 ± 0.015			38
Polyethylene (High Density)	.87	344.83		2.31 ± 0.05		39
	2.1	142.86		2.31 ± 0.05		39
	8.57	35	1.5218 ± 0.0015	2.316 ± 0.004	134 ± 7	39
Polyethylebe (Rigidex 2000)	8.6	34.88	1.5360 ± 0.0015	2.3593 ± 0.0042	173 ± 9.9	40
Polypropylene	8.718	34.38	1.5858 ± 0.0004			41
	8.862	34.80	1.5012 ± 0.0004			38
	8.57	35	1.5014 ± 0.002	2.254 ± 0.004	154 ± 8	40
Teflon (Sintered)	.87	344.83		2.07 ± 0.04		39
	2.1	142.86		2.07 ± 0.04		39
	6	50	1.433 ± 0.007	2.052 ± 0.020	315 ± 26	33
	8.6	34.88			250 ± 30	41
Teflon (unsintered)	8.6	34.88		1.952 ± 0.007	48 ± 3.9	40
TPX	8.677	34.57	1.4589 ± 0.0013			38
	8.508	35.26	1.458 ± 0.002	2.126 ± 0.004	427 ± 21	40
Polystyrene	.87	344.83		2.57 ± 0.05		39
	2.1	142.86		2.56 ± 0.05		39
	6	50	1.590 ± 0.008	2.528 ± 0.025	721 ± 58	33
	8.6	34.88			520 ± 60	41
Plexiglass	.87	344.83		2.61 ± 0.05		39
	2.1	142.86		2.60 ± 0.05		39
	6	50	1.599 ± 0.008	2.557 ± 0.026	3270 ± 262	33
Crystal Quartz (Ordinary ray)	8.57	35		4.430 ± 0.004		42
(Extra-Ordinary ray)	8.57	35		4.633 ± 0.004		42
Slip-Case Fused Silica	3.18	94.34	1.812 ± 0.003	3.285 ± 0.007	2640 ± 142	43
Liquid Cyclohexane	8.436	35.56		2.014 ± 0.003	79 ± 4	44
	4.167	72		2.018 ± 0.002	154 ± 8	44
	2.083	144		2.016 ± 0.004	294 ± 8	44

Table 4.1-4: Result of dielectric characterisation

Free Space technique [14, 15] can also been employed to measure dielectric constant and loss tangent. A layer of dielectric under test of given thickness is placed between two antennas facing each other. Horn/lenses antennas are often used to provide a plane wave at a short range. These antennas permit to avoid diffraction effects on dielectric sample. A calibration before measure permits to remove multiple reflections between the two horns via the surface of the sample. This technique allows to obtain εr and $\tan\delta$ from reflection and transmission measures. For Non magnetic materials, measurement of either the reflection coefficient or transmission coefficient is sufficient to determine the relative complex permittivity.

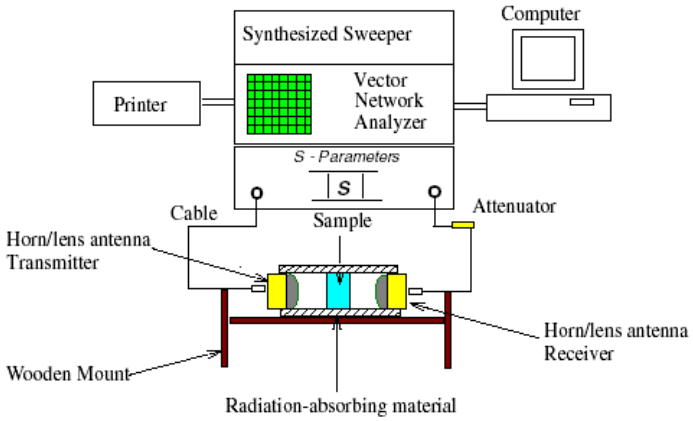


Figure 4.1-17: Free space technique

Thickness of sample have to be important versus wavelength. Then it is easier to characterise thin substrates in MM-Waves.

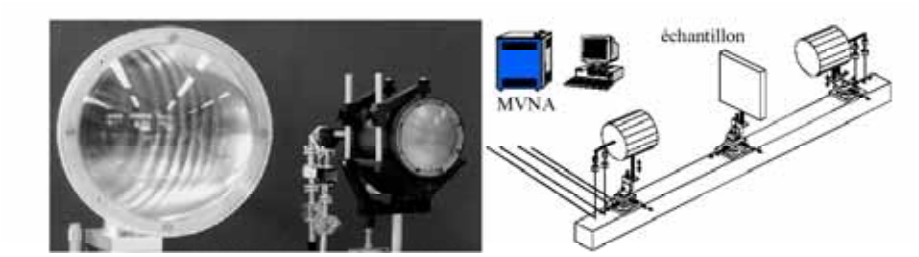
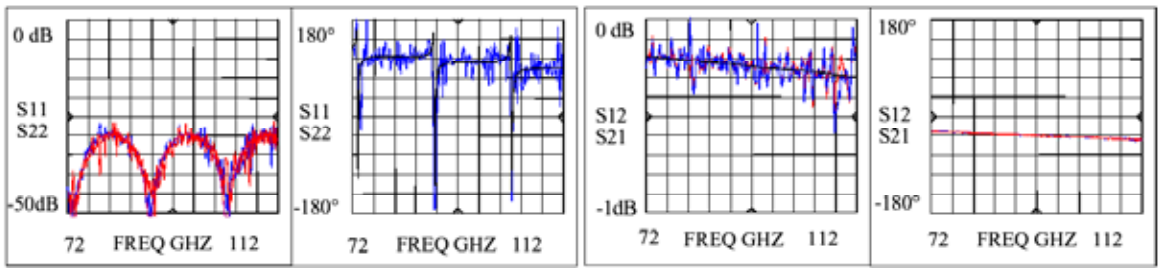


Figure 4.1-18: Free space configuration



Epaisseur 9.93 mm extraction : $\varepsilon r' = 1.069$ (σ=0.001) et $\varepsilon r'' = -0.003$ (σ=0.001) soit $tg\delta = 0.00279$

IETR laboratory has also tested this technique to characterise foam and quartz substrates and results are compared with High Q cavity technique in the followings table:

Fused quartz substrate

Fused Quartz substrate (εr=3.8, h=200µm, tanδ=1.10^{-4} at 10 GHz)
εr =3.8, tanδ=2.10^{-4}, free space εr =3.8, tanδ=2.5.10^{-4}, High Q Fabry Perot Cavity

Foam : closed to air dielectric

Free space	High Q cavity	Manufactor
εr=1.12 tanδ=2.8.0^{-3}	εr =1.126 tanδ=4.3.10^{-3}	εr =1.14 tanδ=1.9.10^{-3}

Table 4.1-5 : Foam and quartz results in free space

Another technique for the measurement of material properties at millimetre wave frequencies is the dispersive Fourier-transform spectroscopic technique (DFTS). This technique is a quasi-optical process and uses a polarisation two-beam interferometer to measure the optical parameters of the specimen. The measured parameters are the absorption coefficient and the refractive index. These quantities are subsequently used to derive the permittivity and loss tangent of the specimen. The DFTS technique has been observed to be more accurate than the other open resonator techniques for millimetre wave measurement [17], [18], [19], [20].

The results obtained from the measurements of various polymers at millimetre wave frequencies are given in [21]. It is observed that Teflon (PTFE) is a very low loss material at millimetre wave frequencies and is applicable for use up to the lower TeraHertz range. However, most PTFE based substrates are composites as mentioned previously, so the result given in [22] does not apply. These composites have only been characterised at X-band and are yet to be characterised at millimetre wave frequencies.

Conclusions

A review of some commonly available commercial substrates and their electrical properties has been given. Factors affecting the choice of substrate, such as dimensional stability, temperature dependence, and water absorption characteristics have been outlined.

Using a microstrip half wave resonator as an example, the importance of various loss mechanisms and the effect of substrate thickness at millimetre wavelengths have been illustrated. Some measured loss parameters for microstrip lines at millimetre wavelengths have been given, and compared against predictions. It is found that at these wavelengths, measured losses are usually considerably higher than predicted.

The effect of beamformer losses on passive millimetre wave array antennas has been described. These losses limit the achievable gain from such antennas. The information available on the open literature on substrate properties has been examined. In particular, it is noted that very little has been published on the properties of commercially available substrates at millimetre wavelengths.

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4.1.2 Dielectric materials (for lens, Dielectric Resonators)

4.1.2.1 Materials for lenses

4.1.2.1.1 Introduction

This section presents and discusses low-loss dielectric materials that can be used for manufacturing millimetre and sub-millimetre wave lenses and dielectric resonators. The materials in most cases are common to the preceding section, but while the previous section focuses on planar substrates, this section addresses bulk volumes involving different requirements in terms of homogeneity and isotropy.

This section presents the most commonly used materials for lens fabrication, its properties, manufacturers and availability, in relation with possible lens manufacturing technologies.

In most cases the electromagnetic characteristic of these materials are specified by the manufacturer for microwave frequencies only, with tolerances that may be incompatible with accurate lens design in stringent applications. This requires in-house evaluation of the electromagnetic characteristics, so a brief discussion is made on commonly used methods.

4.1.2.1.2 Dielectric Materials and Lens Fabrication

Most lens designs at millimetre waves involve homogenous natural dielectrics, either if the lens uses only a single material, or if it uses several materials arranged in a multi-shell configuration [1]-[7]. Homogeneous material lenses usually involve an adequate shaping of the lens surfaces.

In some cases, it is interesting to impose a fixed canonical lens shape (spherical or planar) and obtain the beam shaping by appropriately continuously shaping the lens refractive index profile. One viable and very flexible way to produce these graded refractive index materials is to resort to the concept of artificial dielectrics [8]-[10]. Bulk graded index artificial dielectrics are not commercially available, and are usually produced in the lab in each case. A brief reference is made here to some work in this area.

4.1.2.1.3 Natural dielectrics

The range of permittivities that are interesting for millimetre wave lens applications are roughly in the interval from $\varepsilon_r = 1.2$ to $\varepsilon_r = 11$. Loss factors are desirably better $\tan\delta \approx 5 \times 10^{-3}$, having in mind that lenses are usually large in terms of wavelength.

The very low dielectric constants are commonly used for the outer layers of multiple-shell lenses. Values below $\varepsilon_r = 1.7$ are usually obtained with foam [11] – for instance polyurethane foam. Foam material with controlled permittivity values and loss factors bellow 10^{-3} are available for instance from Emerson & Cuming [12], under the commercial name of ECCOSTOCK SH, for different material densities. They are available in sheets of different thicknesses up to 15 cm. However, due to the foam cell size and overall homogeneity of the material, this may be more appropriate for microwave lenses rather than for millimetre wave ones.

Moderate values of permittivities, in the range ε_r = 1.7 to ε_r = 2.6 are required for beam-shaping lens applications [4]-[7]. There is a good diversity of low-loss materials with these permittivities: ECCOSTOCK LoK (ε_r = 1.7, $\tan\delta < 4 \times 10^{-3}$) [12], TEFLON ($\varepsilon_r \approx 2.1$, $\tan\delta < 4 \times 10^{-4}$), Polyethylene ($\varepsilon_r \approx 2.33$, $\tan\delta < 4 \times 10^{-4}$), Polypropylene ($\varepsilon_r \approx 2.43$), Rexolite ($\varepsilon_r = 2.54$), or Polystyrene ($\varepsilon_r \approx 2.53$, $\tan\delta < 10^{-3}$).

The mechanical characteristics of these materials are generally good for lens manufacturing using milling technology (Figure 4.1-19 to Figure 4.1-22). Teflon is slightly ductile, which makes it less attractive for ultra-precision lens applications. Polyethylene is an attractive low-loss material, but it is very difficult to be glued to other parts. Assembling polyethylene lenses to fixtures usually require screws.

These materials are available in rod or sheet formats with different dimensions, from Emerson & Cumming [12], or from Goodfellow [13]. The respective webpages present on-line characteristics of theese materials and available formats.

Figure 4.1-19: Fabrication of a Teflon lens (Fig. 5) on a milling machine [7]

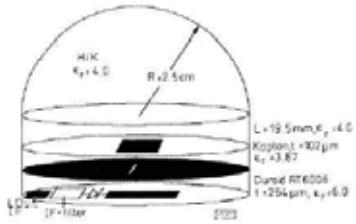

Figure 4.1-20: Extended hemispherical lens antenna at 70 GHz [14]

Figure 4.1-21: Quasi BoR shaped lens antenna at 62.5 GHz [18]

Figure 4.1-22: Optimized 3D shaped lens at 58 GHz [19]

Higher values of permittivities are commonly used in millimetre- and sub-millimetrewave substrate lenses to improve the power coupling into the lens body from single-layer printed feeds [1]. High values of permittivities are obtained for instance from fused quartz (ε_r=3.80) e.g. [1], [2], Kapton (ε_r=3.87) [14], MACOR ($\varepsilon_r \approx 5.5$), different Ceramics ($\varepsilon_r$=6.6) [e.g. [15]], Silicon (ε_r=11.7) e.g. [1],[16] or MgO [17].

All of these high permittivity materials can be obtained for instance from Goodfellow [13] in rod or sheet formats. The limitation sometimes is related to available standard sizes that may limit the lenses dimensions to less than 20 mm diameter.

Emerson & Cuming also produces an agglomerated plastic material Eccostock CK with controlled dielectric constants in the range $\varepsilon_r = 1.7$ to $\varepsilon_r = 15$ with $\tan\delta < 2 \times 10^{-3}$. This material is machineable, and is available in rod and sheet formats. A specified $\pm 3\%$ permittivity tolerance recommends a previous evaluation if this level of inhomogeneity of the material is acceptable for lens production.

The use of high dielectric permittivities for lenses has the drawback of excessive internal reflection at the deielectric/air interface resulting in poor antenna efficiency. One way to minimize this problem is to add a $\lambda/4$ matching layer at the interface [3]. This can be implemented as a coating of a different material, or by introducing corrugations at the lens surface. Due to the resonant nature of this solution, it limits the operation bandwidth of the lens to about 5%.

An alternative solution is proposed in [4] to enhance the bandwidth, where a new shell is added to the lens with a thickness much larger than λ and its shape is appropriately designed together with the shape of the inner lens. In double-shell lenses at mm-waves (or in multiple-shell lenses), when high permittivities are involved, it is important to ensure perfect finish of the common boundaries of the lens shells to avoid air gaps. A liquid cement from Emerson & Cuming with controlled permittivitties in the range $\varepsilon_r = 3$ to $\varepsilon_r = 15$ has been used at IST to fabricate small multi-shell lenses using moulding technique. The obtained results are satisfactory, the main limitation being related to the high dissipation factor of the cement ($\tan\delta = 10^{-2}$).

Injection moulding and castable ceramics are alternative technologies for lens fabrication, which have been discussed elsewhere in this report.

4.1.2.1.4 Artificial dielectrics

Artificial dielectrics are engineered materials formed by a host dielectric medium that is randomly or periodically populated with small ($<<\lambda$) dielectric or metallic inclusions to obtain overall electromagnetic characteristics for the bulk material, which are not directly available form natural dielectrics. By controlling the density of these inclusions it is possible to produce continuously graded effective index profiles according to a specified law. These graded index artificial dielectrics have application in the fabrication of lenses.

Figure 4.1-23 shows an example of a sliced spherical Lüneburg lens, for which a specific distribution of holes fabricated in a Teflon bulk material is used to approximate the ideal Lüneburg index profile [20].

Figure 4.1-23: A sliced spherical Lüneburg lens operating around 30 GHz [20]

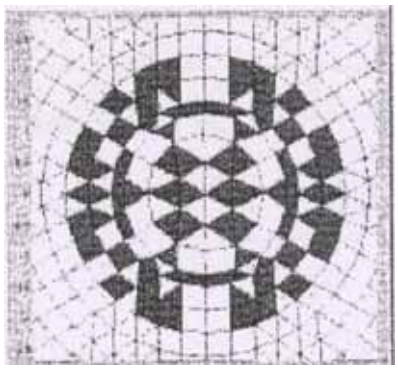

Figure 4.1-23b: Artificial dielectric superstrate

The alternative class of artificial materials with planar metallic inclusions is particularly interesting, because it can be fabricated using planar circuit technology [8], [21]-[22]. A composite material with planar inclusions can be regarded as a stack of dielectric slabs that sustain the metallic elements. These materials however present some anisotropy that must be taken into account in the lens design. Figure 4.1-24 and Figure 4.1-25 show a sample of printed disk media and a mask to be used for fabrication of a planar lens that produces a cosecant square radiation pattern [9], [22]. These engineered materials are not readily available form manufacturers. They are produced in the labs according to own research.

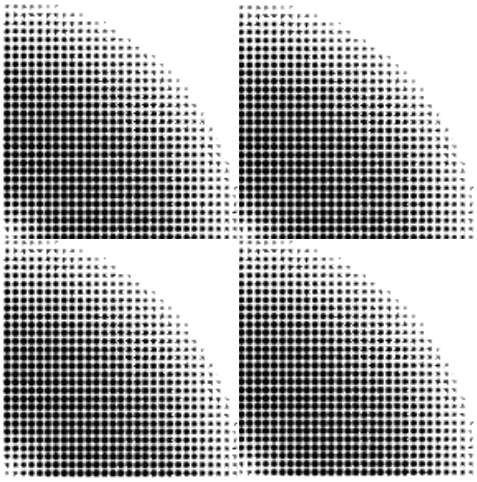

Figure 4.1-24: Sample of printed disk artificial media [9]

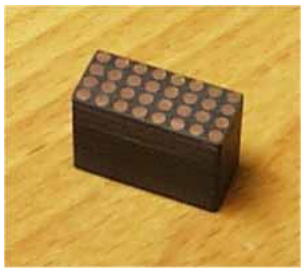

Figure 4.1-25: Mask of one layer of a printed disk artificial lens media [22]

4.1.2.1.5 Dielectric characterization

In most cases dielectric permittivities are specified by the manufacturer only up to microwave frequencies. Although permittivity values do not change significantly with frequency, nevertheless the percentage of change from microwaves to millimetre waves may be enough to compromise some lens designs.

N°	Material	n ±0.5%	$\tan\delta \times 10^3$ ±10%	λ,mm
1	Teflon (unsintered	1.35-1.44	0.23-0.26	0.63
2	Teflon (sintered)	1.43	0.7	1.3
3	Polyethylene	1.53	0.6	0.63
4	Polypropylene	1.51	0.6	0.63
5	TPX	1.44	0.41	1.3
6	Polystyrene	1.59	2.4	0.9
7	Rexolite-1422	1.59	2.4	1.0
8	Duroid-5880	1.48	0.9	3.0
9	Teflon -4MB	1.42	1.2	0.63

N°	Material	n ±0.5%	$\tan\delta \times 10^3$ ±10%	λ,mm
1	SiO_2 (crystal)	n_e =2.45	0.55	2.18
	SiO_2 (crystal)	n_o =2.10	0.56	2.18
2	SiO_2 (fused)	1.95	1.4	0.85
3	SiO_2 (ceramic)	1.92	0.67	1.0
4	Al_2O_3 (ceramic)	3.10	0.26	2.18
5	BeO	2.63	1.2	1.0
6	MgF_2	1.16	0.6	1.2
7	AlN	2.88	0.7	1.4
8	GGG	3.51	1.3	1.15
9	NB	1.72	1.5	0.87
10	$MgAl_2O_4$	2.90	1.0	1.0
11	GaAs ($\rho>10^8$ Ohm·cm)	3.60	0.2	2.24
12	Si ($\rho>25\cdot10^4$ Ohm·cm)	3.42	≤0.01	1.46
13	YIG, Ni-Zn, Li ferrites	3.54-3.95	0.8-1.5	2.0

Figure 4.1-26: Refractive index of different dielectrics at mm-waves [23]

It is possible to find in the literature measured permittivity values for different materials at mm- and sub-mm waves (see e.g. Figure 4.1- 26 from [23], or ref. [24]). Although these results are rigorous still they have only an indicative value, since permittivity values may change from lot to lot (when materials are not pure), with temperature, etc.

Lens design usually requires accurate knowledge of the material permittivity of the specific material block that is used for fabrication. This requires in-house precise evaluation of the permittivity.

A very complete and useful reference on dielectric material characterisation was recently published [25]. Dielectric permittivtiy methods can be generically classified into two major groups: the non-resonant methods and the resonant methods. From the huge diversity of existing methods and variants, this section briefly indicates only three of them which are relevant for millimetre waves and are the most commonly referred. For the following methods, the use of a Vector Network Analyser is most useful.

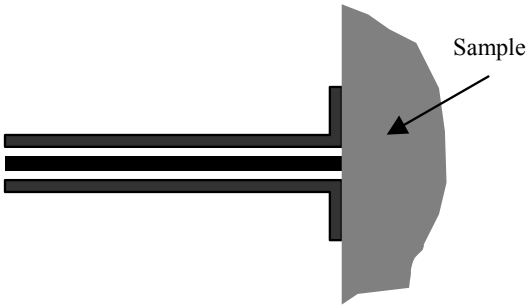

Figure 4.1-27: Open-circuit coaxial probe measurement set-up

Figure 4.1-28: Short-circuited waveguide set-up for permittivity determination

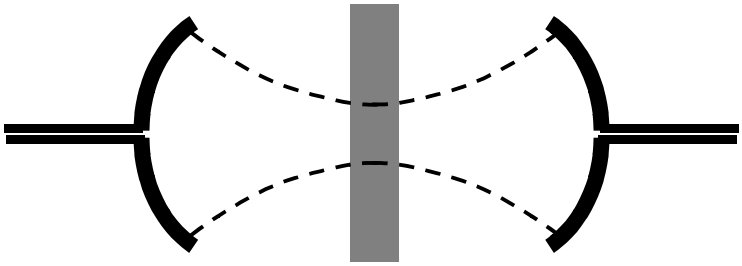

Figure 4.1-29: Open-resonator loaded with dielectric sample

The "coaxial dielectric probe" method falls into the non-resonant method category. A planar, smooth surface sample of the material is positioned (gap-free) at the open-end of a coaxial guide and the permittivity of the material is extracted from the measured reflection coefficient at a given reference plane [25]. A commercial measurement kit of this type and the corresponding deembedding software are available for instance from Agilent (HP85070M) for material characterization from 200 MHz up to 50 GHz [26]. The claimed accuracy on permittivity determination is ±5%, but recommended loss factor of the sample is > 0.05 which is not much attractive for mm-wave lens materials.

A waveguide method has been used quite successfully at IST for mm-wave measurements. The reflection coefficient of a short circuited rectangular metallic waveguide is measured before and after it is filled successively with two dielectric parallelepiped samples of different length that completely fill the waveguide cross-section (Figure 4.1-25). The results from these two measurements can be easily related to the complex permittivity of the sample [25]. This method also falls into the non-resonant category, and allows for material characterization within the waveguide frequency band. The set-up is very easy to be implemented within a lab. One advantage of the method is that it requires very small samples, which allow tracing small inhomogenities of the material block if samples are appropriately taken from different parts of the block. The critical issue for good measurement accuracy are air gaps between sample and metal walls, especially at mm-waves where cross-section dimensions are small and sample surface finish is more difficult to control. This method is not recommended for high dielectric constant materials as the standard waveguide becomes overmoded and degrades the results.

The waveguide method was successfully used at IST to evaluate the permittivity of several samples of printed disk artificial dielectrics, as well as dielectrics with holes [8][9]

Open resonator methods are especially indicated for mm-wave dielectric measurements because they are very accurate and are less sensitive to metallic losses that are the draw-back of closed resonators. The sample is positioned at the minimum waist position of a Gaussian beam formed in the open double-mirror resonating set-up similar to the one represented in Figure 4.1-.29. The complex permittivity of the sample can be extracted from the alteration of the resonant frequency and quality factor of the cavity when it is loaded by the sample [27].

The mechanical set-up for this method requires high fabrication accuracy in the mirrors positioning, alignment and its surface finish. The required sample dimensions are larger than what is required for the waveguide method, so eventual inhomogeneities pf the material are averaged. These measurements are extremely narrowband.

It is up to the user to choose the most appropriate method for its needs balancing the arguments of required accuracy, availability of equipments and skills for measurement set-up preparation.

4.1.2.2 Technologies for Dielectric resonators

Dielectric Resonator Antennas (DRA) are well known for their interesting electrical properties (wide band, low losses, small size, wide range of resonant modes, ...) as well as their compatibility with existing feeding techniques up to the millimetric band.

Involved technologies

The technologies involved in the realisation of dielectric resonators vary with the permittivity range, feeding technique and application. Dielectric constants ε_r ranging from 3 up to 260 can be found associated mainly with two classes of materials, ceramics and plastics:

- Ceramic-based materials rely on several fabrication processes. A good example is Low Temperature Co-fired Ceramic (LTCC) for which permittivities are limited (ε_r < 10) but that allows printed metallizations throughout the different layers. On the other hand, alumina offers higher permittivity ranges, with metals on surface applied by serigraphy using conducting inks. For these materials, thicknesses available on the market do not exceed 5 mm, which can be a limitation for DRAs topologies at a few GHz.
- Plastic-based dielectrics are available on the market with dielectric constants up to 14. Moulding techniques can conveniently be applied to shape resonators. However, metallisations are difficult to realise.

The permittivity used for the dielectric resonator sets a tradeoff between bandwidth and size (i.e. higher permittivities enable size reduction at the expense of antenna bandwidth). In practice, permittivities found in the literature range from $\varepsilon r \sim 6$ up to $\varepsilon r \sim 40$, depending on the application.

4.1.2.3 References

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4.2 SURVEY OF EXISTING MANUFACTURING TECHNOLOGIES

4.2.1 Injection moulding

4.2.1.1 Introduction

Injection moulding is an attractive manufacturing process for large volumes [1]. At frequencies below 10 GHz antenna requirements can usually be fulfilled with printed circuit based antennas. At higher frequencies reflector, lens, or waveguide based antenna solutions have to be used [2]. Plastic injection moulding together with metal plating is a low cost alternative for large volume manufacturing of complex array antennas, while conventional manufacturing techniques such as machining and casting are not cost-effective [2]. Technology can be used for antenna applications including mm-wave point-to-point links, Ka-band satellite ground terminals, Automotive Intelligent Cruise Control (AICC) Radar and Microwave Video Distribution Systems [2]. In this presentation, a brief overview of the injection moulding is given, materials and manufacturers are presented, and some applications of in microwave and millimetre wave devices are described.

4.2.1.2 Injection moulding

For micro- and millimetrewave antennas of large production volumes, injection moulding is an attractive manufacturing process. It enables manufacturing of parts with complex geometry and gives a good surface and dimensional quality. A dimensional accuracy of 20 microns has been reported in [3]. Injection moulding is process which moulds plastic through heat and pressure by injecting molten plastic into the desired mould. Granular plastic or plastic pellets are melted by friction of a rotating screw and actual heating, and then injected into the mould. Design and optimisation of the mould for the manufacturing process is one of the key issues in the process [3]. Injection moulding requires a substantial capital investment, but it becomes economically viable in mass production and gives a very low unit production cost.

4.2.1.3 Plastics in injection moulding

Usually thermoplastics are used, but also fibre reinforced thermoplastics or thermosettings can be used. The plastics that are used in injection moulding include, e.g., polythene, low density polyethylene (LDPE), high density polyethylene (HDPE), polystyrene (PS), high impact polystyrene (HIPS), polypropylene (PP) and acrylonitrilebutadienestyrene (ABS). According to [2], the mostly used plastic is ABS. The plastics used for special applications are the knowledge of the manufacturing companies. The reported plastics used in microwave or millimeterwave applications are listed in Table 4.2-1.

Plastic	Reference	Trade name
Liquid Crystal Polymer (LCP)	[3]	
Polyphenylene oxide – modified (PPO-M)	[4]	NORYL
Polyetherimide (PEI)	[4]	ULTEM

Poly-ether-ether-ketone 450	[4]	PEEK

Table 4.2-1: Reported plastics used in injection moulding.

4.2.1.4 Metal plating

To achieve good electrical properties for the devices the surface of the plastic has to be plated with metal. The thickness of the metal should be large enough compared to skin depth (at least 5 times). Also, the surface roughness should be small, however, injection moulding gives adequate quality for the surface. The plating can be done first applying thin metal with electroless plating and then thickening the metal layer with electrolytic process. The metal layer can be coated with thin high-conductive and anticorrosive metal layers. Methods for metal plating include electroplating, electroless plating, metal spraying, and vacuum metallisation. The plating material and method depend on the physical properties and composition of the material that is going to be plated. Metals used for metallisation include, e.g., nickel, copper, and aluminium.

4.2.1.5 Manufacturers

The injection moulding is use for very broad variety of products. Therefore, there are very large amount of manufacturers. The manufacturers found on the micro- and millimetrewave applications are Philips Microwave of Stockport England [1], Thomson-Thorn Missile Electronics Ltd, Hayes, Middlesex, England [4], and EADS, Microwave Factory, formerly DaimlerGhrysler Aerospace AG, Germany [7,5].

Low-profile link antenna operating at 58 GHz is reported in [5] and [6]. The design was made at the Radio Laboratory, Helsinki University of Technology [6], and the antenna manufacturing was developed in DaimlerChrysler Aerospace AG [5]. The antenna has a waveguide feedernet and 256 boxhorns as radiating elements. Antenna consists of four metal plated parts. Feedernet consists of two parts, one forms the waveguide structure and the other is the backplate acting as a wall for the waveguides. Two parts forms the radiating elements. The metal plated plastic antenna is about 230 mm × 180 mm × 25 mm in size and it weights about 400 g [5].

ESTEC and Thomson-Thorn have carried out R&D program for development of plastic filters for space applications using injection moulding and metal plating technologies [4]. The demonstrator filter was a four-pole rectangular waveguide passband filter with centre frequency of 12.47 GHz [4]. In addition to three plastic filters (see Table 4.2-1), an aluminium filter was manufactured for comparison of RF performance. In the study the filters were milled avoiding the fabrication of the expensive mould. The used plastics were reinforced with 30 % glass for ensuring milling properties. The metal plating was in three phases: 1) thin electroless copper plating 0.5 □m, 2) thickening with electrolytic copper, and 3) gold flash for corrosion protection. The total metallization thickness was 12 □m. The measured results of the RF were similar in all plastic and aluminium filters.

A waveguide filter based on cavity-resonators coupled mutually by inductive irises for 20 GHz is described in [3]. Copper plating was used and thin nickel plating was added for anticorrosive. The performance of the realised filter is equivalent to the metal filters. Other applications include surface mountable filter having pass-band at 42 GHz [7], a waveguide based diplexer designed for 28 GHz [8], dual orthogonal linearly polarised 20/30 GHz antenna array [2], television receive only antenna for Ku-band (10.7–12.75 GHz) [2], demonstration of automotive collision avoidance radar at 94 GHz [1,9,10,11].

Suppliers for injection molding materials specified in Table 4.1-6

Liquid Crystal Polymer (LCP)

-Solvay Advanced Polymers, Brussels, Belgium, http://www.solvayadvancedpolymers.com/products

-Trademark: XYDAR

- Kuraray America, Inc, http://www.vectranfiber.com,

-Trademark Vectra

Polyphenylene oxide – modified (PPO-M)

-GE Plastics, USA, http://www.geplastics.com

- Trademark: Noryl

-RTP Co., USA, http://www.rtpcompany.com/

-Basf plc, UK, http://www.basf-plc.co.uk

-Luxus Ltd, UK, http://www.luxus.co.uk/Homepage.htm

Polyetherimide (PEI)

-GE Plastics, USA, http://www.geplastics.com

-Trademark: Ultem

-Goodfellow Cambridge Limited, UK, Goodfellow GmbH, Germany, Goodfellow SARL, France, http://www.goodfellow.com

Poly-ether-ether-ketone 450

-GEBA, Germany, http://www.geba-ennigerloh.de

-Trade name PEEK

-Gharda Chemicals, India

-Trade name PEEK

-Victrex, UK, http://www.victrex.com

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4.2.1.6 References

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4.2.2 3D Technology

4.2.2.1 Multilayer technology with interconnections

Nowadays, organic multilayer PCB - Printed Circuit Board – is a developed technology for a Beam Forming Network or integrated radiating elements.

Microwave printed circuit boards are interconnected by specific vertical interconnections. Fuzz-button transition is one of them.

It has been measured and characterised in the 2–20 GHz band.

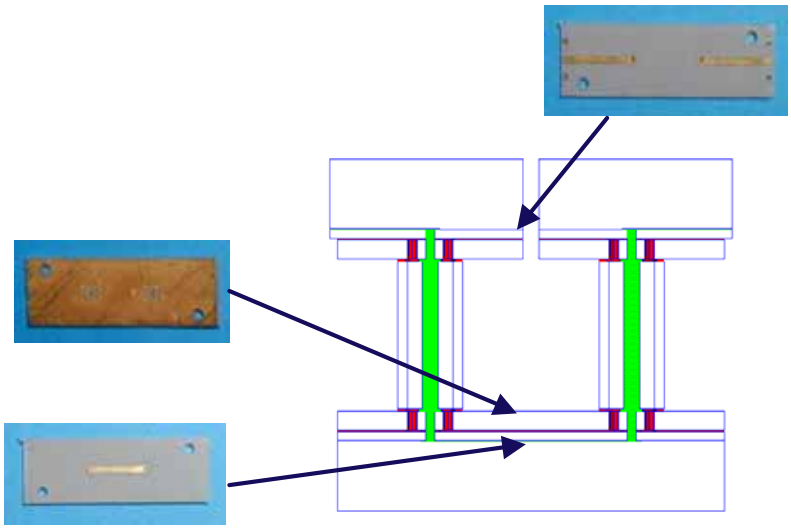


Figure 4.2-1: Fuzz button moke up

A 3D coplanar interconnection by flex is also a potential solution. The following picture shows the flex before the assembly on the substrates. the RF flex is made up of a 50 µm thick Kapton on which a 17 µm thickness of copper has been metallised.

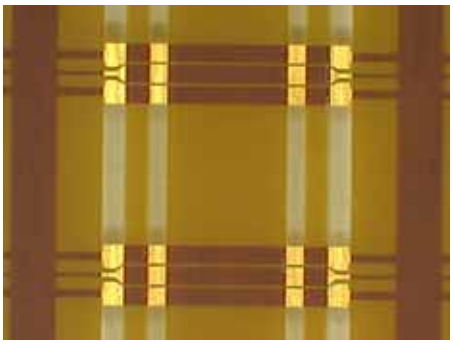


Figure 4.2-2: Coplanar flex interconnection

But such a technology experiences limitations :

- when working frequency exceeds 20 GHz, RF multilayer interconnections state of the art, (of metallized via holes, for example), reaches its limit ;
- for chip integration inside BFN itself, as multilayer PCB realization process (lamination, pressure, thermofusion) is usually incompatible with component insertion in multilayer.

4.2.2.2 The 3D Technology

The 3D technology – also called MCM-V - is based on the full encapsulation in a resin, with an interconnection system etched on the surface of the "cube". The main steps are :

- manufacturing of the individual levels made on printed circuit board populated with passive and bare components (1),
- stacking in a mold with spacers (2),
- molding in an epoxy resin and polymerization (3),
- machining to the final size (4),
- plating and etching (laser routing) to define the interconnection between all the levels of the stack (5).

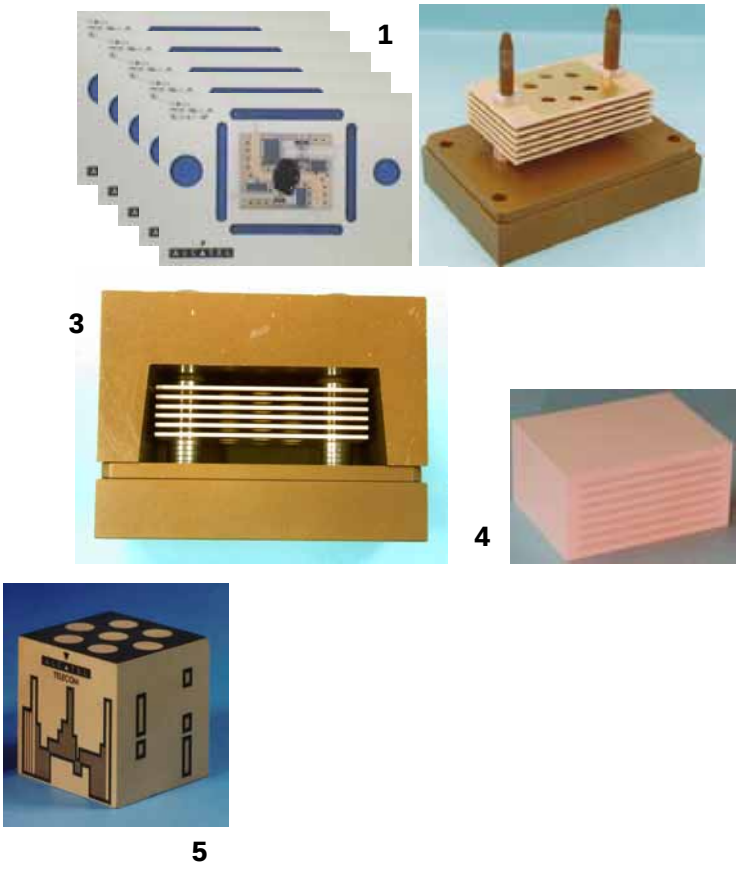


Figure 4.2-3: Detailed process of the 3D technology

The 3D technology has been developed initially for digital processing and transposed for microwave application. Ultra wide band vertical interconnections, which could operate up to 60 GHz, were designed through shielded homogeneous coplanar lines with a 90° vertical structure as shown on Figure 4.2-4.

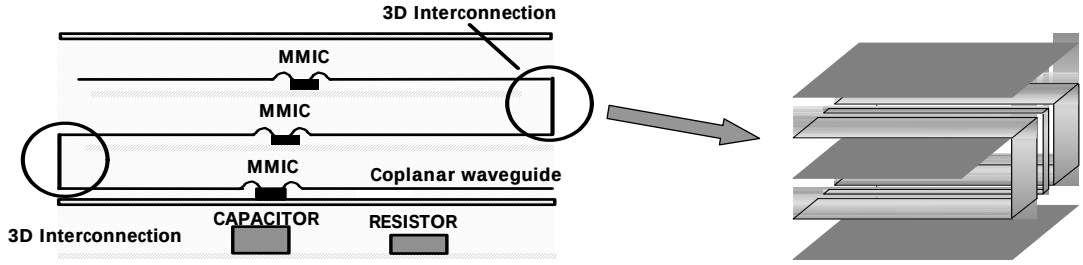


Figure 4.2-4: RF vertical interconnection

The organic boards are based on specific materials traditionally used in the field of microwave printed Circuit Boards. A specific attention has been given to the resin which could be compliant both with the expected level of losses and with the bare MMICs which will be included in the final MCM-V.

A new concept of partly "throw away " mold enables us to reach a very good layer positioning (less than ± 50 µm in x and y directions and ± 25 µm in z axis).

The shielding of the final module could be made with an overmolding completed by a full metallisation.

Suppliers for 3D technologies :

3D PLUS

3D PLUS is the leading company for the 3-D electronics packaging in Europe and is recognized as a high performance innovator in the design and manufacturing of miniaturized 3-D modules for Active, Passive, Opto-electronics and MEMS/MOEMS components packaging.

4.2.2.3 Reference

[1] : P. Monfraix et al “3D microwave modules for space applications”, Microwave Symposium Digest, IEEE MTT-S International , June 1998, pp 1289 - 1292

4.2.3 Laser patterning

4.2.3.1 General comments

Laser beams can expose photo resists and several laser-driven reactions such as photo-ablation, material deposition or surface treatment. They are attractive because they are easily and precisely imaged, focused and scanned over large areas that need not be flat.

Laser patterning has been addressed in the frame of a european project TRILAP, involving a manufacturer of laser systems (EXITECH), a supplier of CAD software (CAE) which will produce and promote respectively the system and the CAD tool, a technological institute specialised in automation and laser systems (RTM), several industrial companies and SME involved in the above applications), and a laser application centre (IREPA Laser).

The project addressed the following developments :

1. Development of 3-D laser patterning systems having the following characteristics:
    - laser sources chosen from generic types of laser (Excimer, CO_2 and Nd:YAG) that appear the most promising for patterning and structuring processes.
    - computer controlled work-piece and/or beam handling
    - beam forming and image plane/focal point position control on 3-D shaped device surfaces
    - process viewing and monitoring
    - CAD interface of laser machines
2. Development of software interfaces between :
    - electrical and mechanical tool packages enabling 3-D circuits layout and visualisation
    - 3-D mechanical CAD package and the CNC (Computer Numerical Controller) for the robot of the 3-D multi-axis machines.

   Appropriate laser-based processes and laser system have been developed and 3 prototype systems have been fabricated, and are currently validated on several application test devices to be designed, processed and characterised within this project :
    - 3-D printed circuits (multi-layer interconnections and moulded circuits), using two low fluence laser system prototypes (6 and 5-axis)
    - metal foil structures (aerofoils), using one high fluence 4-axis system prototype

Note : the Laser fluence is the Quantity of energy applied by a laser beam on a work-piece per square centimer

4.2.3.2 Multilayer process

Two different processes have been applied to obtain the required patterns and the choice of process is determined by the area coverage of the copper tracks. In an antenna with a beam forming network, we must distinguish the signal layer from the patch layer. For signal layers, for which the copper tracks of the circuitry occupy less than 50% of the total area, the process is the following :

1. plasma cleaning and copper metalisation
2. electrophoretic resist coating
3. laser ablation of the insulating tracks
4. chemical etching of copper
5. resist removal

For the RF layer (with patches and a significant amount of metal), an inverse process has been developed, optimising the time required for laser processing

1. plasma cleaning and copper metalisation
2. electrophoretic resist coating
3. laser ablation of copper tracks and via pads
4. electrolytic SnPb coating on exposed copper and inside via holes
5. resist removal
6. chemical etching of copper
7. chemical etching of SnPb

The ablation process for both processes are based on mask projection. The performances of two lasers, with a different wavelength, were investigated. The comparison is reported in Table 4.2-2.

	KrF excimer laser (248 nm wavelength)	TEA CO_2 laser (10.6 µm wavelength)
Ablation conditions	1.5 J/cm^2 < fluence < 4.0 J/cm^2 5 < number of pulses < 10	2.0 J/cm^2 < fluence < 3.0 J/cm^2 2 < number of pulses < 3
Line quality	Good, with excellent width control	Irregular, especially for narrow lines
Accuracy on narrow lines	-1/+3 µm on 60 µm line width	-5/-10 µm on 100 µm line width; irregular
Cleanliness	excellent	post cleaning required (plasma), with effects on final feature size
Process speed	acceptable	2-3 times faster than with KrF excimer laser

Table 4.2-2: Excimer laser (KrF) and TEA CO_2 laser processing trial results for electrophoretic resist ablation in conductor processes 1 and 2

It appeared that the KrF excimer laser gave superior results because of better cleanliness, accuracy and line quality. The CO_2 laser ablation process invariably produced residues, both on the exposed copper and on the remaining resist which could only be removed by plasma cleaning. This has the undesirable side-effect of broadening the ablated lines slightly, since the plasma process also removes some of the resist.

4.2.3.3 Feasibility of via drilling with laser

Again, the KrF excimer laser gave superior results for via drilling, as compared to the CO_2 laser. The latter produced conical holes and too much debris that stuck to the surface and walls of the hole. The excimer laser produced holes of acceptable quality at a fluence of 1.8 J/cm^2, but required of the order of 10^4 shots to drill a single through hole, and 200 shots to drill a 100 µm interconnect hole. This represents a processing time of approximately 2 seconds for an interconnect hole, and 50 seconds for a through hole.

In view of these results it was decided to drill the interconnect holes with the excimer laser but to use a mechanical drill to produce the through holes, at a drilling time of approximately 1 second with the mechanical drill.

Figure 4.2-5 shows the via drilling and plating technology developed during the TRILAP project. Shown are a plated through hole and an interconnect via between two adjacent layers. The through in this figure was not mechanically drilled but by excimer laser. The slightly tapered profile so produced is advantageous for the plating process. The interconnect via were also drilled by excimer laser.

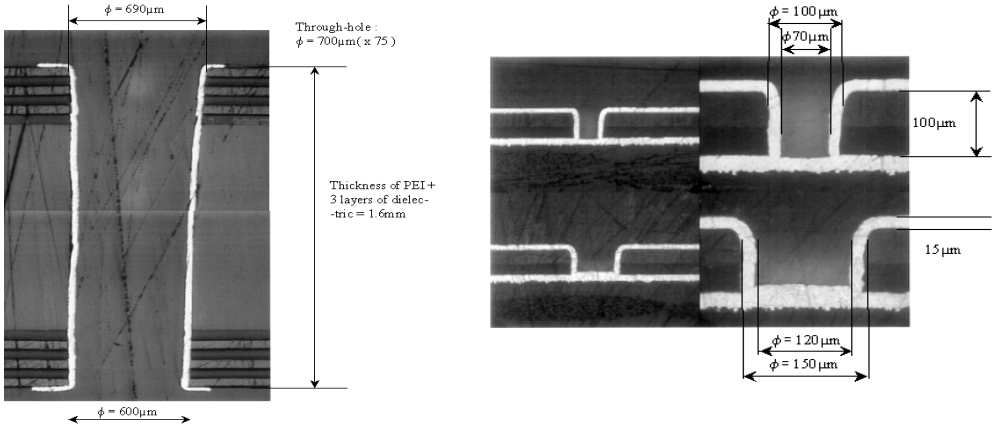


Figure 4.2-5: Excimer laser drilled copper-plated through hole (left) and interconnect via (right).

4.2.3.4 Summary

We presented here a process for which a laser was used to ablate the resin. Chemical etching remains used. The accuracy is imposed by the chemical etching process.

The main interest of this process is for etching non planar surfaces :

- Conformal surfaces (developable or not) ;
- 3D objects ;

It is required to have the laser normal to the surface to pattern. Either the object or the laser (or both) shall have degrees of freedom (translation, rotation). This process is necessary for non planar objects not compatible with lithographic processes, or for non developable curve surfaces.

4.2.4 Conformal PCB

Patterning and structuring on 3-dimensional shaped surfaces is a critical process when high precision is required. Traditional mechanical methods such as moulding, printing and machining have limited capability to produce very small features together with high positional accuracy.

On the other hand, high definition lithographic processes that are widely used in the printed circuit board industry have the capability to deliver the required small feature size and positional accuracy, but not the ability to be extended for use on non-flat surfaces by nature of the pattern transfer method. Subsequent shaping of flat, patterned surfaces into the required shape is possible, but this will distort the pattern geometry and can therefore not be used for the production of surfaces with predictable properties.

For simple boards (one layer, no via holes) conformed to a curve surface with limited deformation, this is achievable. When the board includes large deformations or many layers, this is not possible

A specific process is presented in this section, which leads to a much higher accuracy than the assembly of a PCB on a conformal surface.

Patterning on conformal substrates has been addressed in the frame of a european project TRILAP, involving Thales Research and Technology, Exitech (see previous section for more informations). The objectives were to investigate :

1. accurate form shaping of the antenna substrate
2. 3-dimensional lamination technology
3. development of software tools to convert 2-dimensional circuitry designs in Gerber file format into the 3-dimensional shape of the antenna substrate

The typical following multilayer approach is requested for the antenna.

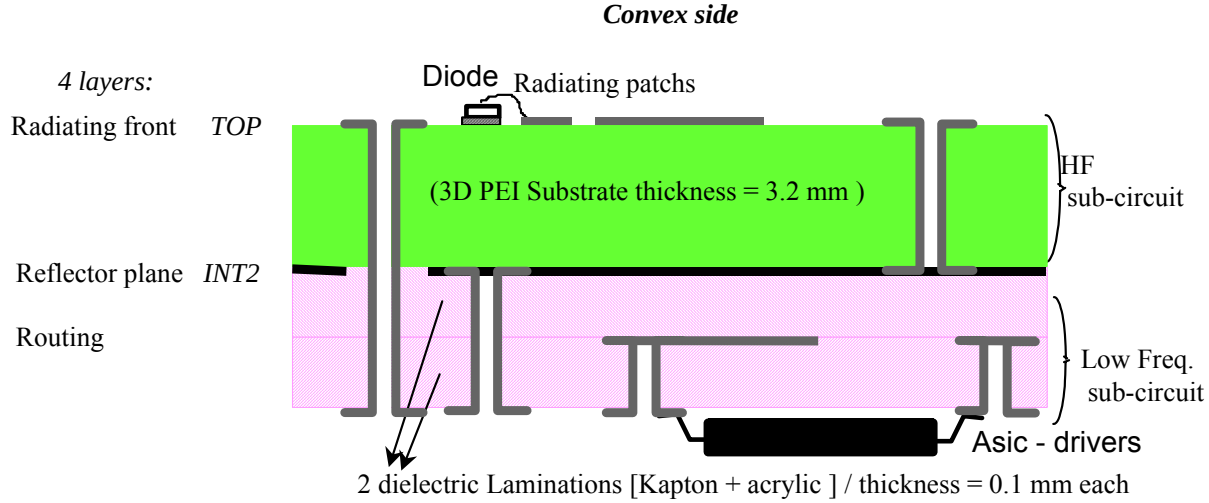


Figure 4.2-6

The key points are :

- The ability to shape a typical soft surface ;
- The ability to mount ASIC in a conformal surface ;
- The ability to metallise signal tracks, via holes and patches.

The process presented in XXX is a potential response to this problem.

The antenna substrate is manufactured by the following operations:

1. form the antenna shape by thermal pressing
2. Mechanically drill the through holes from the concave layer INT2 to the convex side layer TOP
3. Copper plate both sides and the drilled holes (15 µm copper)
4. Apply process no 1 to concave layer INT2
5. Apply the first dielectric layer, 50 µm Kapton and 50 µm acrylic, onto layer INT2 by means of a lamination process
6. Apply process no 2 (negative) to concave layer INT3
7. Apply the second dielectric layer (50 µm Kapton and 50 µm acrylic) onto layer INT3
8. Laser drill the required blind via between the concave layers (using copper pads as stops), and mechanically drill through via from the concave to the convex side
9. Apply copper plating to both sides, to form layer BOTTOM on the concave side and layer TOP on the convex side. The plating also effects the connections through the via and holes produced in the previous step.
10. Apply process no 2 to the TOP and BOTTOM layers

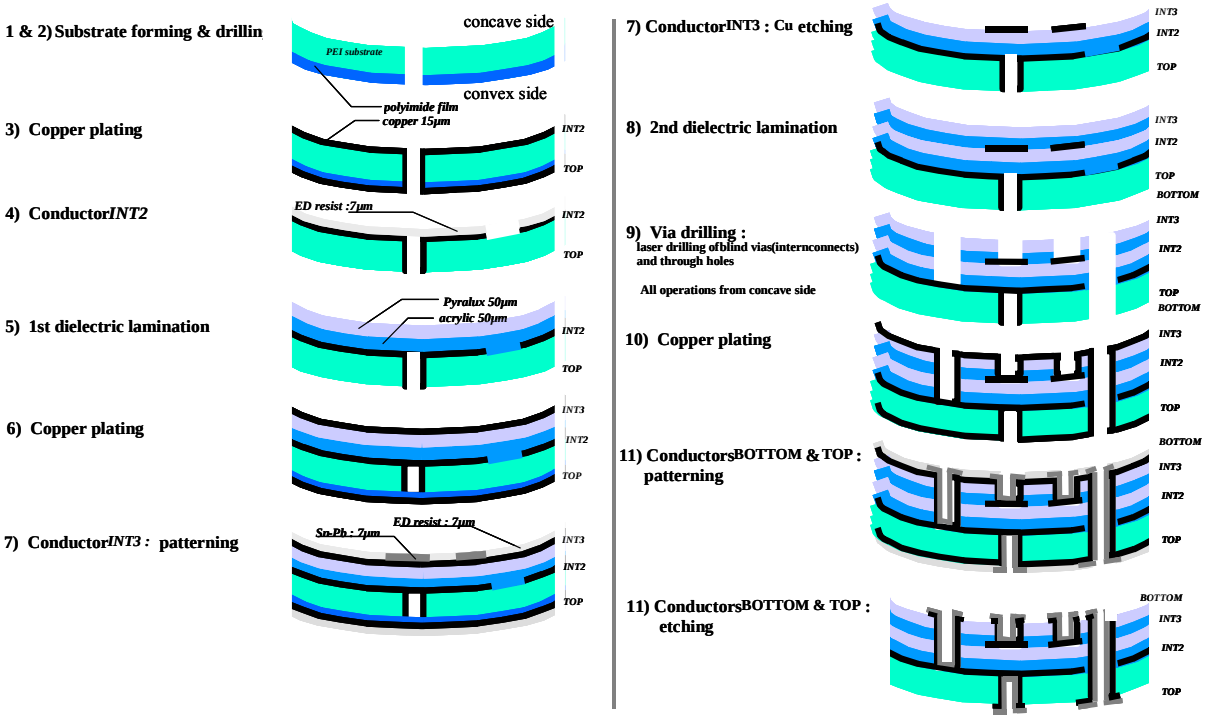


Figure 4.2-7: Process for a conformal active antenna

Figure 4.2-8 shows the first layer that was produced on the concave side (INT2). The copper that was deposited for this layer also metalises the insides of the through holes. This layer carries the power and ground connections of the antenna. The through holes connect the convex side, which carries only one layer (TOP) that hold the active microwave devices, with the power/ground layer.

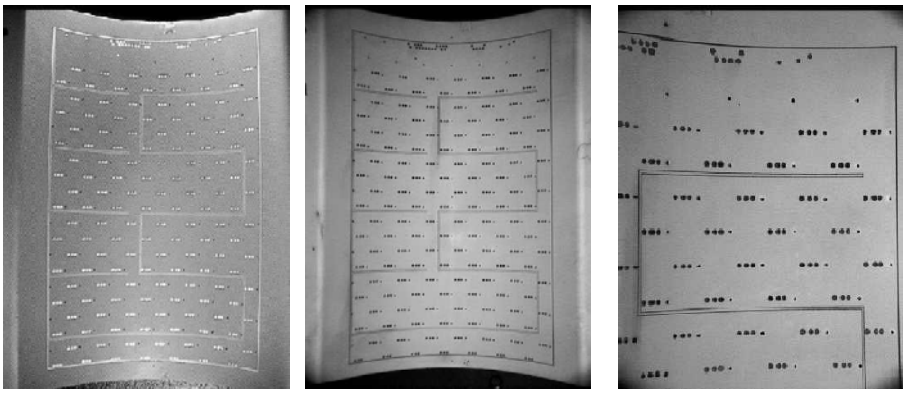


Figure 4.2-8: Power/ground plane INT2, laser patterning (left), copper etched (middle) and pattern detail (right).

Figure 4.2-9 shows the next layer, INT3, that is put on top of INT2. The dielectric layer, applied by 3-D lamination technology, is transparent and visible in the photograph are the underlying holes through the substrate, some laser drilled interconnect via between INT3 and INT2 and some of the features of INT2. These are the dark features in the close up on the right-hand side of the figure. As an indication of the scale, the large circular insulation inside INT plane have a diameter of 2 mm.

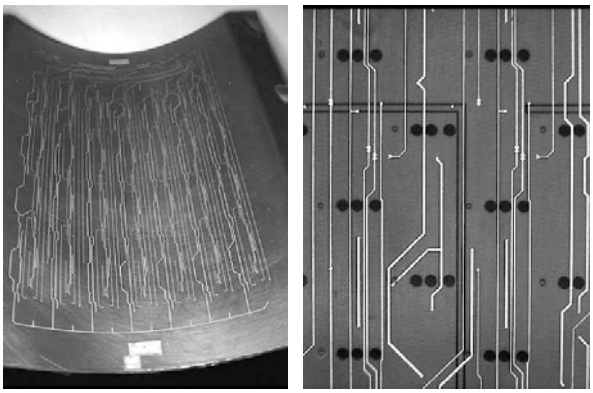


Figure 4.2-9: Electrolytic SnPb coating after laser patterning of signal layer (left) and detail (right)

4.2.5 Foam and Metal deposit for 3D antennas

4.2.5.1 Introduction

Most of applications require conformal antennas, curved surface and so curved metallization. Low weight, low cost and user-friendly are the other ones. As a solution the laboratory has developed a new technology based on metallized foam [1]. The structure is foam manufactured and then directly chemistry metallized. The deposed metal can be gold, silver or even copper. This technique offers several advantages such as the possibility to metallize 2D and 3D conformal antennas. Moreover the technique is compatible with holes and component import directly solded on the foam.This process has been optimise by industry.

4.2.5.2 Technological and design aspects

The used foam is a PVC closed cells material. It dielectric constant changes from 1.05 to 1.55, as a function of its density, and can support temperature from -200°C to 80°C without exceeding one hour time of exposition at 90°C. Low tanδ and low permittivity allow envisaging the metallized foam material in a large panel of applications including antennas.

All the used foams have been characterized up to 110 GHz by two techniques: Free space and High Q cavity. One example is given in Table 4.2-3. Dielectric constant and loss tangent values are compared to manufactor ones. Results prove the possibility to use this technology in millimetre waves range. However limitations appear for very high frequency due to the size cell of the foam.

Free space	High Q cavity	Manufactor
εr=1.12	εr =1.126	εr =1.14
tgδ=2.8.10^{-3}	tgδ=4.3.10^{-3}	tgδ=1.9.10^{-3}

Table 4.2-3: Metallized foam

The structure is foam manufactured and then directly metallized thanks to classical metal deposit process.

Price of a foam plate : It depends on dielectric permittivity and thickness but the price is included between 160 and 600 euros.

4.2.5.3 Temperature and power tests

A lot tests have been done concerning temperature, power… Five printed antenna arrays (4 patches) have been manufactured and put in different tests conditions. All different conditions are described as follow :

Cold temperature : -55°C during 16h
Heat dries : 70°C during 16h
Temperature cycles : 5 stages of temperature from –40°C to 70°C, with 2h per stage.
Weat heat : From 5% to 95% during 6 days

For each test, VSWR, S11 and resonant frequency are measured before and after tests. All the results are presented on the following tables. Generally, measures show that the metallized has a good behaviour during these tests. S11 magnitude and frequency shifts are very low.

Cold Temperature

	VSWR (form)	F_0 before test	F_0 after test	S_{11} before test	S_{11} after test
Ant n°1	Unchanged	3,19 GHz	3,18 GHz	- 21 dB	-20,4 dB
Ant n°3	Unchanged	3,17 GHz	3,18 GHz	-19 dB	-20,7 dB

Dies Heat

	VSWR (form)	F_0 before test	F_0 after test	S_{11} before test	S_{11} after test
Ant n°5	Unchanged	3,17 GHz	3,18 GHz	- 30 dB	-34,5dB
Ant n°3	Unchanged	3,19 GHz	3,19 GHz	-17,3 dB	-18,6 dB

Temperature cycles

	VSWR (form)	F_0 before test	F_0 after test	S_{11} before test	S_{11} after test
Ant n°2	Unchanged	3,16 GHz	3,18 GHz	- 17,9 dB	-16,8dB
Ant n°3	Unchanged	3,16 GHz	3,18 GHz	-18,3 dB	-17,1 dB

Weat heat

	VSWR (form)	F_0 before test	F_0 after test	S_{11} before test	S_{11} after test
Ant n°4	Unchanged	3,18 GHz	3,17 GHz	- 18,6 dB	-32 dB
Ant n°3	Unchanged	3,18 GHz	3,15 GHz	-17,1 dB	-22 dB

Table 4.2-4 : tests results

To finish, a power characterisation has been done. A HF generator has been connected to a power amplifier and the output is connected both to a spectrum analyser and to a foam metallised waveguide. The power level sent in the waveguide is 10W CW. Observation concerns the temperature increasing versus time for this waveguide (Figure 4.2-10 and Figure 4.2-11). The emission power causes the temperature increasing (4°C in 4s). But after, the temperature will increase up to 30°C only. Moreover, this test has been done with a continuous wave but it will not true for all applications.

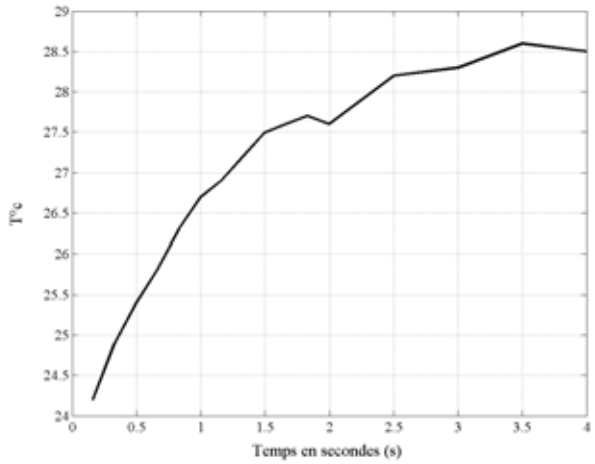


Figure 4.2-10: Waveguide temperature between
0 and 4s

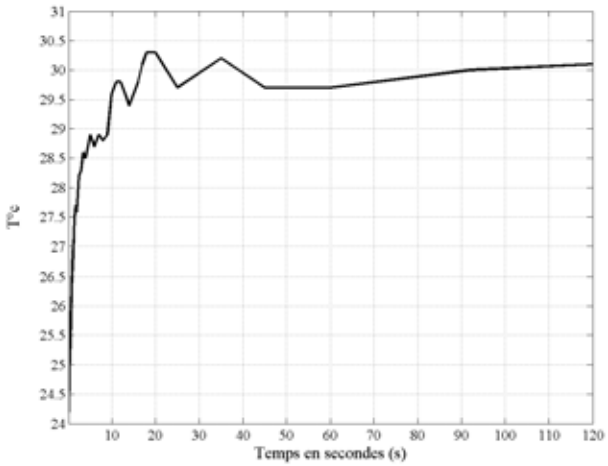


Figure 4.2-11: Waveguide temperature between
0 and 120s

[1] brevet, M. Himdi, J.P. Daniel. "Procédé de revêtement de mousse pour la fabrication d'éléments d'antennes"

4.3 POSSIBLE ANTENNA APPLICATIONS

4.3.1 Multilayer printed antennas

4.3.1.1 Soft substrates applications

With the multilayer printed antennas technology (TPX substrate and thick ground plane), a lot of passive and active antennas have been realised up to 60 GHz [1, 2, 3]. Moreover, this technology allows to have engraved slot in ground plane, metalised holes, …We give on Figure 4.3-1 an example of active antenna array with two mixers and metalised holes. The objective was to reduce frequency from 40 GHz to 5.7 GHz. These elements permit to realise antenna excited by electromagnetic coupling. It become easier to separate active layer and feeding line from radiating elements. This technology has also been tested to realise high gain printed antenna array. Indeed, some 256 aperture coupled patch antenna array have been optimised and manufactured at 60 GHz with this technology.

Figure 4.3-1: Active antenna with mixers

Another application is to use this multilayer technology to separate feeding line network to radiating elements. It allows to reduce spurious radiation due to feeding lines. It is particularly necessary when feeding line network is important in term of lines length. An example is given on Figure 4.3-2 with printed Butler matrix in 60 GHz band [4, 5]. This design permits to obtain multibeam antennas. This optimised antenna allows to have 4 beams (Figure 4.3-3) and a relatively good efficiency is shown (40%). This antenna has been manufactured on Glass Teflon substrate.

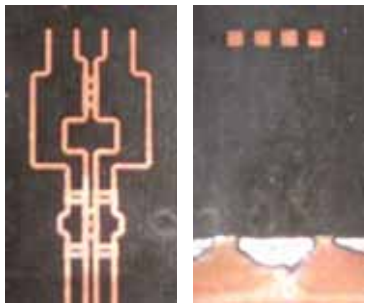


Figure 4.3-2 : Butler matrix and multilayer technology

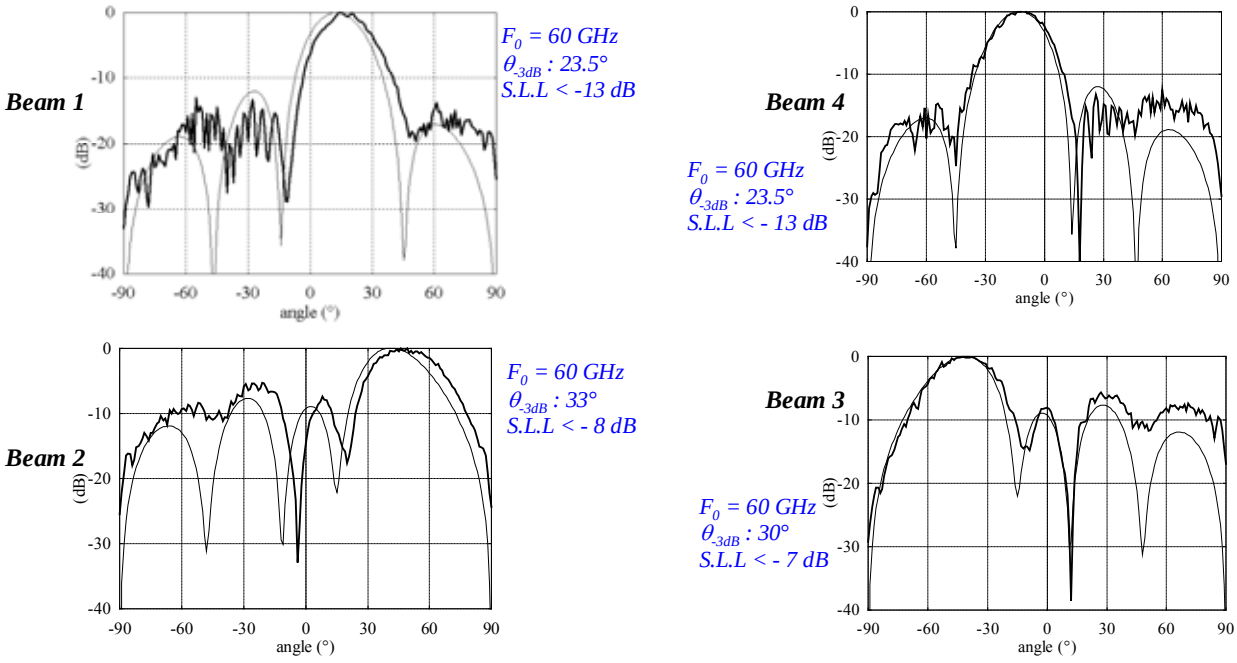


Figure 4.3-3: Radiating patterns for 4 beams

[1] : M. El Haj Sleimen, 'Etude et réseaux d'antennes imprimées en millimétrique', Thèse de l'Université de Rennes 1, soutenue le 2 mars 1999.

[2] : OLIVIER LAFOND, 'Conception et technologies d'antennes imprimées multicouches à 60 GHz', Thèse de l'Université de Rennes 1, soutenue le 04 décembre 2000.

[3] : O. LAFOND, M. HIMDI, J.P. DANIEL, "Thick slot coupled printed antennas arrays for a 60 GHz indoor communication system", Microwave and Optical Technology Letters, Volume 25 / Number 2, pp. 105-108, 20th January 2001.

[4] : J.BUTLER and al., 'Beam-forming matrix simplifies design of electrically scanned antennas', Electronic Design, vol. 9, pp. 170 – 173, Apr. 1961.

[5] : O. LAFOND, M. HIMDI, ''Multibeam antenna in millimeter waves'', the 32nd European Microwave Conference (EuMC), 23 – 27 septembre 2002, Milan.

4.3.1.2 Rigid Multilayer technologies

Figure 4.3-4 shows an example of aperture-coupled 4 elements antenna array printed on fused quartz substrates. Numerical simulations and measurements have confirmed that the proposed wafer bonding techniques have a negligible influence on the input impedance and gain, compared to the effects of residual air gaps.

(a) (b)

Figure 4.3-4: Front (a) and rear (b) view of an aperture-coupled microstrip patch antenna array printed on 150µm-thick fused quartz substrates

4.3.2 Dielectric resonators antenna

4.3.2.1 Features of dielectric resonators

Dielectric resonator antennas have received much attention from numerous researchers for use as radiating element in spatial, mobile and intra-muros communication systems. Indeed, they present a better alternative to microstrip patch antennas, since they offer a great ability of coupling to commonly used feeding scheme and possibility to obtain different radiation patterns using various modes. Furthermore, they presents some advantages such as relatively large bandwidth and compact size. Another attractive feature they propose is a high radiation due to their no inherent conductor loss, since there is no metallic part.

4.3.2.2 Feeding technologies

The coaxial probe is a feeding technique that usually leads to drill the resonator (Figure 4.3-5). This technology may introduce an air gap between the probe and the resonator. This gap have to be reduced or controlled in order not to alter the feed.

In some case, the perforation is not required and the probe can be set outside the resonator.

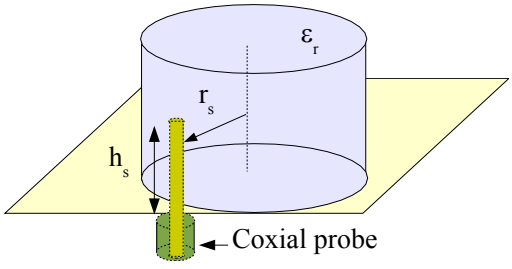


Figure 4.3-5: Geometry of the coaxial probe fed

Another technology used is the slot coupling with a feeding line (Figure 4.3-6). Since the dielectric resonator permittivity is high (over 20), we choose a substrate with an almost high permittivity (9,8) in order to concentrate the energy inside the material. The main advantage of this technique is that is not necessary to perforate the resonator.

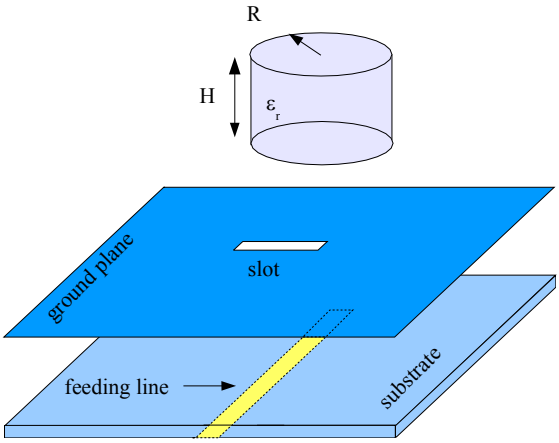


Figure 4.3-6: Geometry of the slot coupling fed

As the quality of the the feed is very sensible to the position of the resonator on the ground plane, a high precision is necessary. To correctly set the resonator, some marker points are printed on the ground plane.

For simple device (one single resonator), the resonator is fixed to the ground plane with four sips of glue (Figure 4.3-7) without creating an air gap between the resonator and the ground plane.

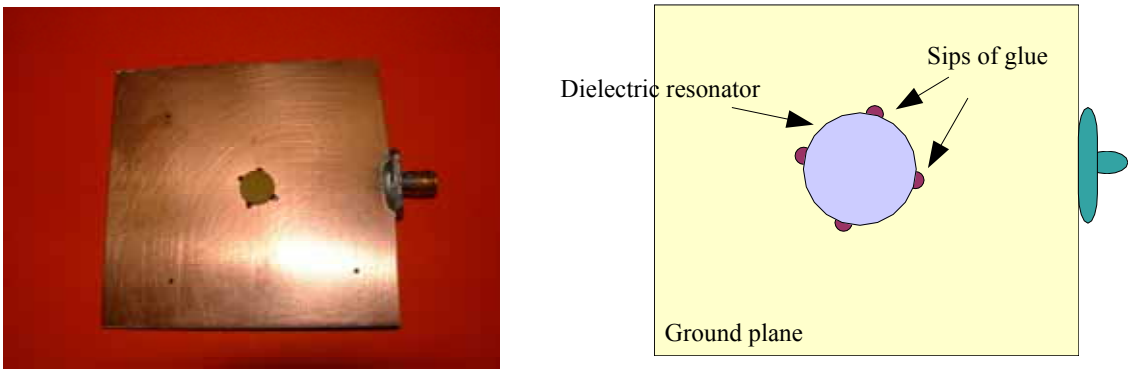


Figure 4.3-7: Resonator fixation

For complex structure (arrangement of few resonators), a foam is used. Its dielectric constant has been chosen close to 1 in order to prevent perturbations on the radiating structure.

This foam can be used to recover resonators or in layer, placed between two resonators, to make an air gap. Figure 4.3-8 shows the geometry of a multifrequency dielectric resonator antenna fed by a slot coupling.

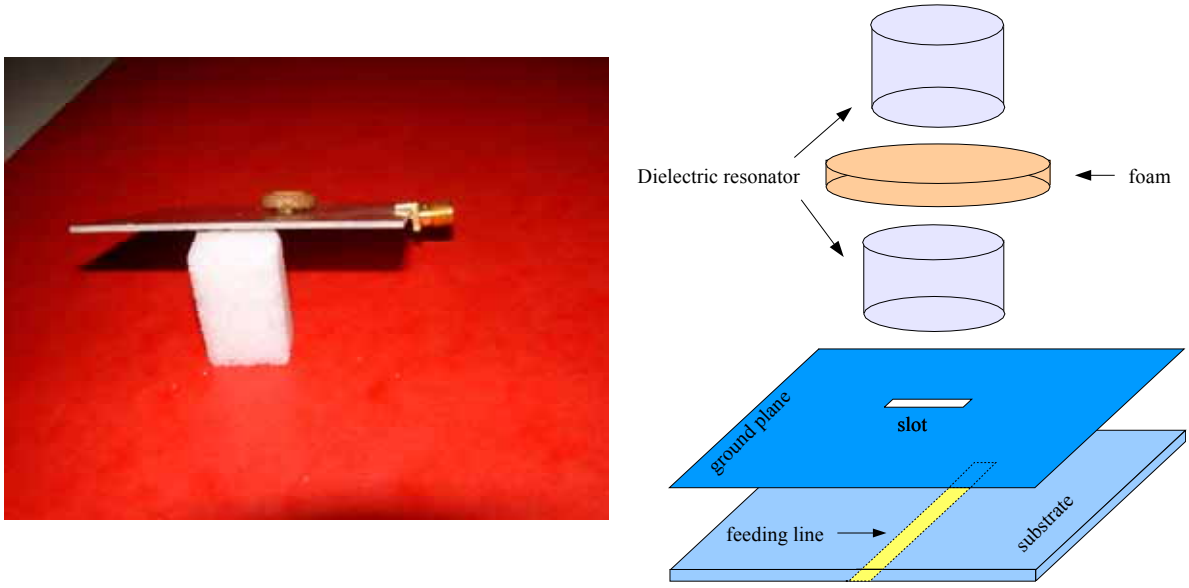


Figure 4.3-8: Geometry of a multifrequency dielectric resonator antenna

The whole structure is fixed with two thin nylon strings (Figure 4.3-9).

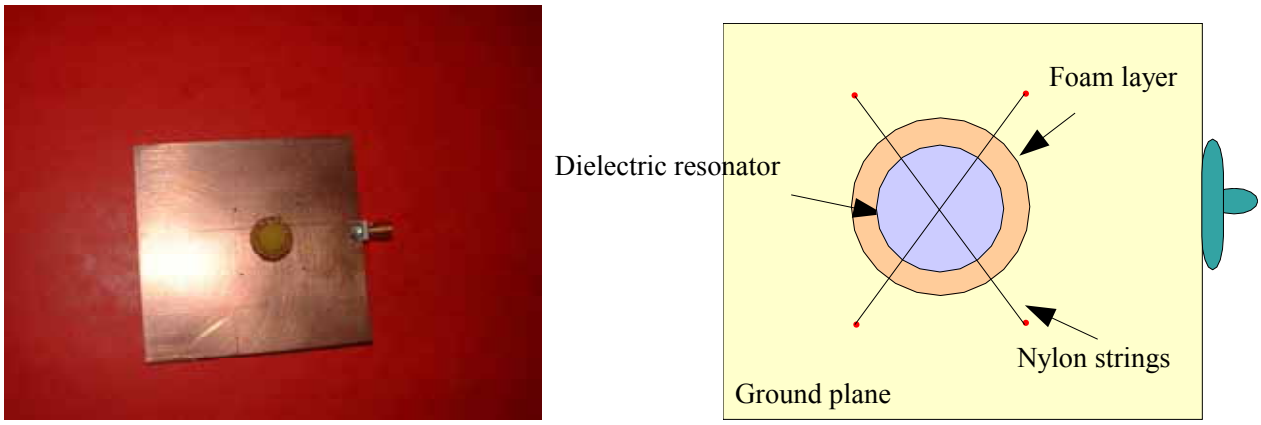


Figure 4.3-9: Technology of the multifrequency dielectric resonator antenna

4.3.2.3 Drilled dielectric resonator

The « Laboratoire d'Electronique Antennes et télécommunications »(LEAT) works on dielectric resonator conception. The interest is related to the realization of multifrequency antennas and on structures allowing increase of the bandwidth. For instance, new topologies of resonators based on cylindrical forms is holding our attention so to obtain a modification of the resonant frequency, an increase in the bandwidth, a reduction of size or a multifrequency behavior. Furthermore, the creation of a circular polarization is carried out using a structure obtained by drilling holes in a cylindrical resonator. In order to realize good prototypes, the dielectric resonator have to be machined with precision and all the elements of the antenna have to be properly arranged and fixed.

Tekelec Temex produces dielectric resonators of standard form but currently only in industrial quantity. Emerson & Cuming manufactures rod, bar, sheet of low loss dielectric material. They also offer possibility to manufacture resonators of standard or more complex form on request. The company produces dielectric material with a minimum permittivity of 30. Figure 4.3-10 and Figure 4.3-11 show the geometry of a circularly polarized dielectric resonator antenna. The resonator presents five drilled holes including one for the antenna feed.

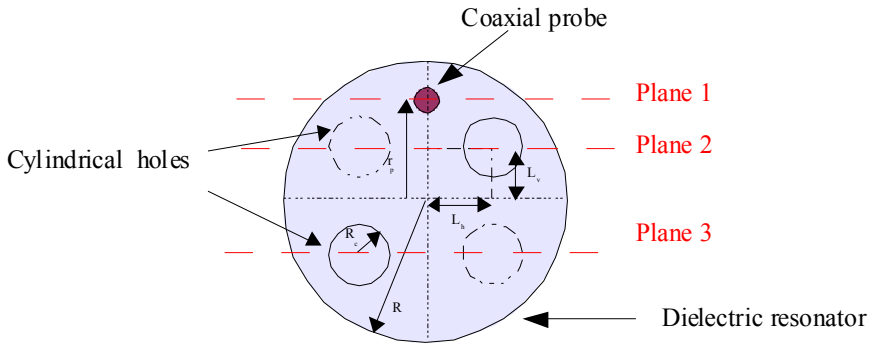


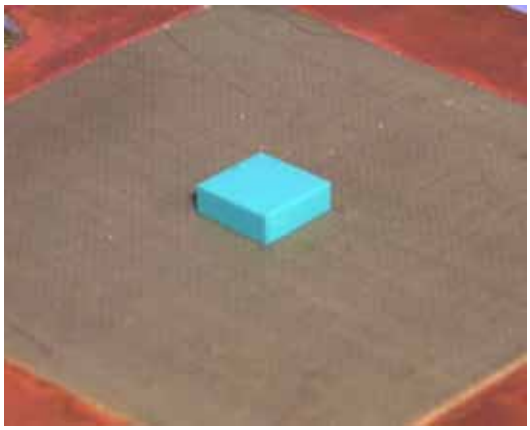
Figure 4.3-10: Geometry of a circularly polarized dielectric resonator antenna. Top view

4.3.2.4 Multiple telecommunication applications of dielectric Resonators

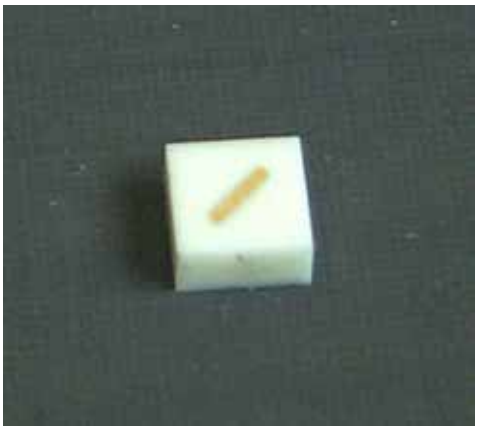
Several designs and technologies have been investigated for Ku band satellite communications. Figure 4.3-11 presents a linearly polarised slot fed LTCC DRA. The resonator is glued on top of an intermediate substrate made of duroïd [1] for better design robustness. Figure 4.3-11(b) presents a slot fed circularly polarised alumina DRA. A metallic strip is printed on top of the resonator to excite two orthogonal modes in phase quadrature. This structure has conveniently been implemented in a 4 element sequential rotation array [2,3]. For these structures, losses below 0.5 dB have been measured at 15 GHz, with bandwidths up to 30%.

DRAs have also been validated as radiating elements for WLAN applications (Hiperlan2 and IEEE802.11.a , 5.15GHz - 5.35GHz) [4,5,6]. For compactness, electric plates have been placed at the electric walls of the fundamental mode of the DRA to reduce its dimensions. These DRAs also proved compatible with Surface Mount Technology (SMT).

DRAs have also been demonstrated at 5 GHz as compact radiating sources suitable for active arrays [7]. For this particular design, the ceramic resonator is fed through a coupling aperture in the ground plane. An slotline orthogonal to the ground plane is used to couple energy to the dielectric resonator, while allowing space for active circuitry.



(a) LTCC resonator



(b) Alumina resonator with metallic strip

Figure 4.3-11: Examples of DRAs.

A mobile phoned antenna was developed by MCL. It is a ceramic based antenna used in mobility devices, such as mobile phones or GPS handsets.

It comprises of a ceramic cylinder with a through hole (for co-axial connection). The outer surface of the cylinder is plated with copper and coated with ED resist.

The ED resist is then laser ablated three dimensionally in a negative pattern, using RTM's 5 axis laser prototype, thus exposing the under layer of copper. This exposed copper is then etched away via a conventional PCB etching process. The non-ablated ED resist is then stripped off, thereby exposing the finished copper circuit positive pattern. The component is finished with electro less deposited nickel and gold.

Figure 4.3-12: Mobile Phone antenna on a ceramic

4.3.2.5 Reference

[1] A. Laisné, R. Gillard and G. Piton, « A robust slot fed Dielectric Resonator Antenna (DRA) using an intermediate substrate », *Electronics Letters*, Vol. 37, n° 25, pp. 1497-1498, December 2001.

[2] A. Laisné, R. Gillard, G. Piton, "Circularly polarised Dielectric Resonator Antenna with metallic strip", *Electronics Letters*, Vol. 38 no. 3, pp. 103-107, January 2002.

[3] A. Laisné and R. Gillard, « Antenne à résonateur diélectrique polarisée circulairement », *European patent*, n° 0111248 (F), August 2001.

[4] D. Cormos, A. Laisné, R. Gillard, F. Le Bolzer, C. Nicolas, « Compact Dielectric Resonator Antenna for WLAN applications », *Electronics Letters,* Vol. 39, n° 7, pp. 588-590, April 2003.

[5] F. Le Bolzer, C. Nicolas, D. Cormos, R. Gillard and A. Laisné, « Antenne à résonateur diélectrique large bande », *French patent,* n° 0210429, August 2002.

[6] F. Le Bolzer, C. Nicolas, D. Cormos, R. Gillard and A. Laisné, « Antenne compacte à résonateur diélectrique large bande », *French patent,* n° 0211114, September 2002.

[7] G. Lathière, R. Gillard and H. Legay, « Dielectric Resonator Antenna with orthogonal slotline feed », *Electronics Letters*, Vol. 40, n° 12, pp. 715-716, June 2004.

4.3.3 Metallized foam

This original and low cost technology allows to realise 3D antennas and circuits up to 40 GHz. Moreover, this technology is compatible with active components report and some processes have been optimised to reduce foam roughness. This metallized foam can also been used to realise conformal antennas and complex 3D structures.

In military applications, waveguide technology are often preferred to microstrip antennas. Then, metallized foam could be used to realise slotted waveguides antennas, harmonic absorption filters for this application.

Some examples are given below (Figure 4.3-13, Figure 4.3-14 and Figure 4.3-15). First, this technology allows to realise 3D antennas, such as a 3D dipole symmetrically fed by slot located in the ground plane (Figure 4.3-13). The electrical connection between the slot and the V dipole is accomplish thanks to 2 metallized holes realized in the same time of the rest of the antenna.

Moreover this technology permits to associate active components directly solded on the foam. A example of active array for beam scanning is represented on Figure 4.3-14.

A last example is shown using this technology at 35 GHz. This example deals with a transversal slot waveguide antenna (Figure 4.3-15). Slot are tilted and excited by the waveguide. An angle scanning is possible thanks to a frequency scanning around 30 GHz. A matched load is realized at the end of waveguide with graphite insertion.

Figure 4.3-13: 3D V dipole antenna

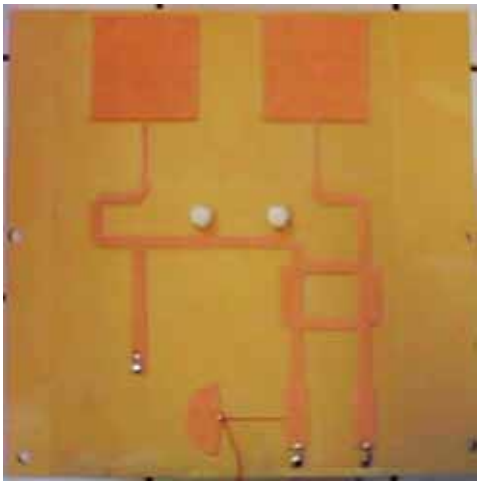


Figure 4.3-14: Beam scanning antenna

Figure 4.3-15: Transversal slot waveguide antenna

4.3.4 Gaussian Beam Antenna

4.3.4.1 State of the art

The enhancement of the directivity of any primary source using Fabry-Perot (FP) cavities [e.g. 1-4], EBG radomes [e.g. 5-8] or superstrates [e.g. 9] is a well-known principle.

Introduction:

This sub-section briefly presents the characteristics of low-profile directive antennas operating in the 60 GHz band and providing low side lobe radiation patterns. In these structures, the FP resonators are generally plano-convex. This kind of antennas is usually named “Gaussian Beam Antennas (GBAs)” [10], by analogy with dielectric loaded compact open resonators, because their radiation patterns have a very low side lobe level.

The typical geometry of GBAs is represented in Figure 4.3-16 and Figure 4.3-17. In the first case, the FP cavity is illuminated by a guided source, whereas it is fed by a printed antenna in the second one. The partially reflecting mirrors are generally 1D or 2D periodic metallic gratings.

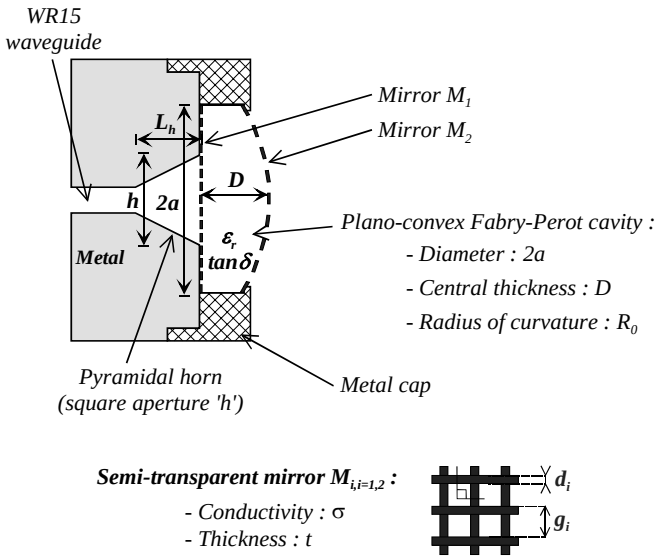


Figure 4.3-16: Plano-convex FP cavity fed by a horn antenna.

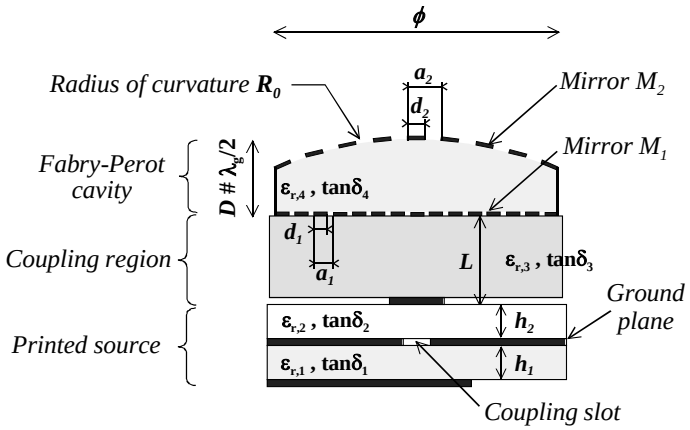


Figure 4.3-17: Plano-convex FP cavity fed by an aperture-coupled microstrip patch antenna.

4.3.4.2 Advanced development

The optimum design of GBAs requires (a) an accurate knowledge of the quasi-optical characteristics of FP cavities, as well as (b) the mutual coupling between the feed and the cavity.

(a) The analysis of FP cavities illuminated by a plane wave is quite straightforward because the same tools as those developed for FSS modeling can be implemented. Some papers describe modeling tools of FP cavities based on the Finite-Difference Time-Domain technique [11] or the transmission line matrix method [12]. The latter approach requires precise impedance models of periodic patterns, like inductive or capacitive metallic grids [13,14]. The overall performance of FP resonators around 60 GHz are given in [15].

Figure 4.3-18: Examples of FP cavities with inductive patterns

From a technological viewpoint, the typical dimensions of the grid patterns and substrate thickness are conventional values for millimeter-wave structures. Thin film processes are usually required to achieve an accuracy of several micrometers. The main issue probably deals with the uniform photolithography of rigid substrates with a plano-convex shape, and/or with a diameter of several inches.

(b) The mutual coupling between printed primary sources and multi-layer periodic superstrates has been investigated in several papers [e.g. 16-18] as a function of (*i*) the topology primary source (printed or guided technology), (*ii*) the radius of curvature of the FP cavity, (*iii*) the thickness *L* of the dielectric coupling region, and finally (*iv*) the *Q*-factor of the cavity. An example of GBA is represented in Figure 4.3-19; its measured radiation pattern is given in Figure 4.3-20. The resonator is fed by 2×2 aperture-coupled linearly-polarized microstrip antenna array.

Figure 4.3-19: a GBA with its measurement setup at 60 GHz

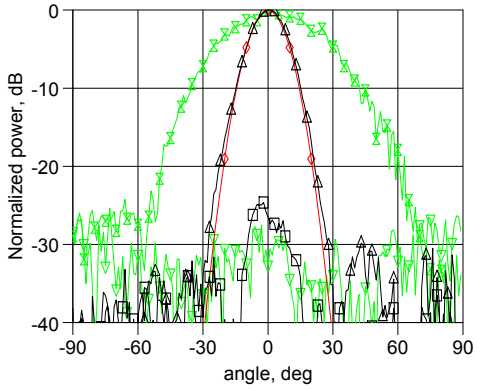


Figure 4.3-20: Theoretical and experimental radiation patterns at 56.75 GHz (theory: red line; measurement: black line; primary source: green line)

The overall radiation performance is as follows:

- The theoretical directivity varies between 15dBi and 25dBi depending on the radius of curvature of the FP resonator,
- The radiation efficiency is comprised between 20% and 70%, depending on the *Q*-factor of the cavity,
- The side lobe level is generally lower than –20dB and –25dB for FP cavities fed by printed sources and guided sources, respectively.

Moreover, to optimize the mutual coupling conditions between the cavity and the primary source, the thickness of the dielectric coupling region should be close to $\lambda/2$ (this corresponds to the opening of a defect mode inside the photonic crystal comprising the actual FP cavity and its electrical image with respect to the ground plane of the primary radiator).

Periodic reflecting mirrors behave as equiphase surfaces, as predicted by Gaussian optics. It has been demonstrated that the use of *plane-parallel* FP cavities with *non-uniform grids* (Figure 4.3-21) enables to generate a Gaussian radiation pattern (Figure 4.3-22).

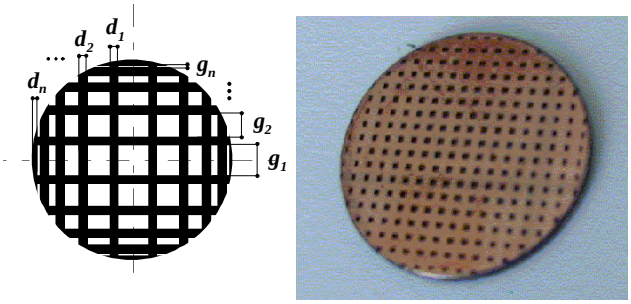


Figure 4.3-21: Non-uniform grid mirror at 57.6 GHz.

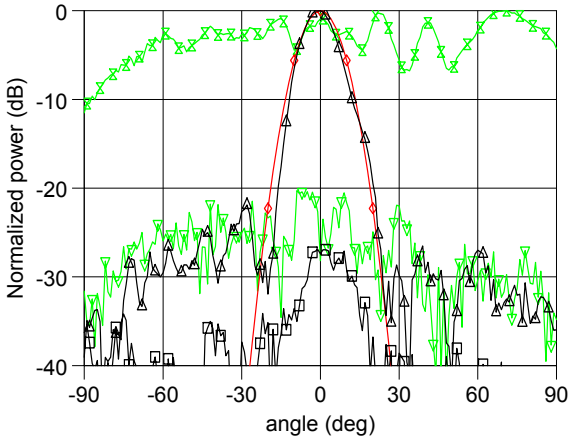


Figure 4.3-22: Theoretical and experimental radiation pattern in E-plane at 57.6 GHz. (theory: red line; measurement: black line; primary source = microstrip patch antenna: blue line)

More generally, the optimization of non-periodic structures appears very attractive for the design of innovative radiating structures (leaky wave antennas, zone-plate lenses, EBG and metamaterials radomes, meta-substrates and meta thin films, …).

4.3.4.3 References

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4.3.5 Integrated feed array

One of the main topics of R&D activities is the development of “low cost” active phased array antennas. An active array is made of radiating elements, connected to a filtering section, an amplifier as close as possible to the radiating source in order to efficiently compensate for losses in the transmission lines (including the Beam Forming Network).

As operational frequencies are increasing steadily over the year (up to more than 40 GHz for space applications, for example), the inter-element spacing in a phased array is decreasing accordingly. The accommodation of such RF equipments in a reduced lattice is then an issue.

Moreover, in the next future, it will be desired to process microwave signal as close as possible from its source and to remove all microwave paths within the system). This means that analog/digital conversion will be processed at the radiating element level, resulting in an additional requirement to implement Emission/reception modules within the array lattice. This challenging issue will lead to high packaging densities but also to highly compact and attractive designs.

Examples of integrated elements developed by EADS, Thales or Alcatel Space are given in the following sections.

The first examples are Integrated TR Modules which include different layers :

- Control ASIC chip level,
- Low power level components (LNAs)
- RF power components (HPA, driver)

The several layers are manufactured on soft substrates. The power components are attached on a layer directly in contact with the cooling system of the antenna. The command part is on the top layer : transitions between the command part and the RF levels are performed through bump connections.

Different module architectures are investigated to realise the assembly. They differ each other from technologies and interconnections required to realise the T/R module.

4.3.5.1 MCM-V concept

The first architecture is based upon a multi-chip module vertical (MCM-V) technology. It uses the 3D technology, presented in Chapter precedent. The first Different layers are molded with a resin, the module is then fully metallised and finally the face of the modules are etched in order to achieve vertical interconnections between the levels. The transitions with the antenna are made with subminiature connectors and flex.

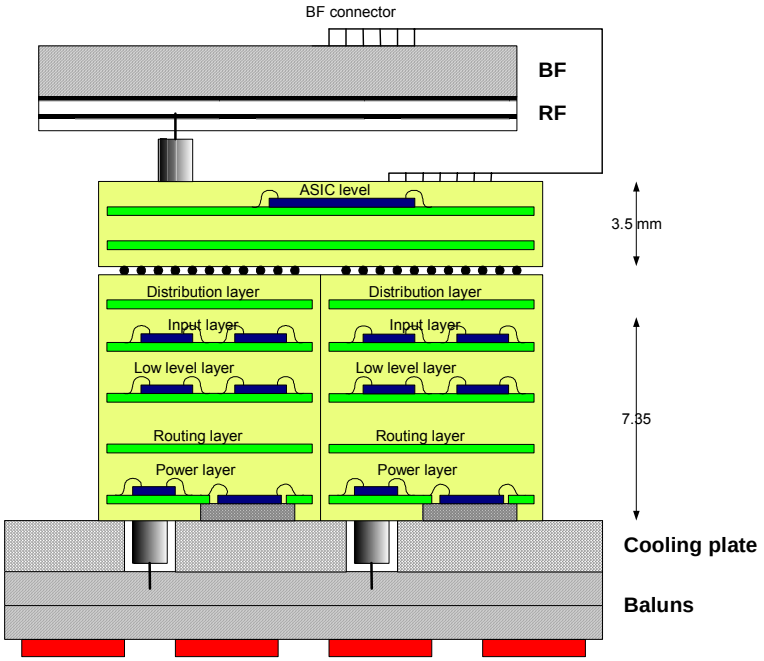

Figure 4.3-23: Integrated radiating element with a TR module [1-2]

4.3.5.2 MCM-D concept

The second architecture is based upon the MCM-D (deposited multi-layers) technology. The several RF levels are achieved on soft substrates or on aluminium baseplate (power level), these high integrated levels are manufactured with a multi-layers thin films technology, using BCB dielectric. The power components are attached on the bottom layer directly in contact with the cooling system of the antenna.

Fuzz buttons and elastomeric connectors connect the different levels. The transitions with the antenna are made with subminiature connectors and flex.

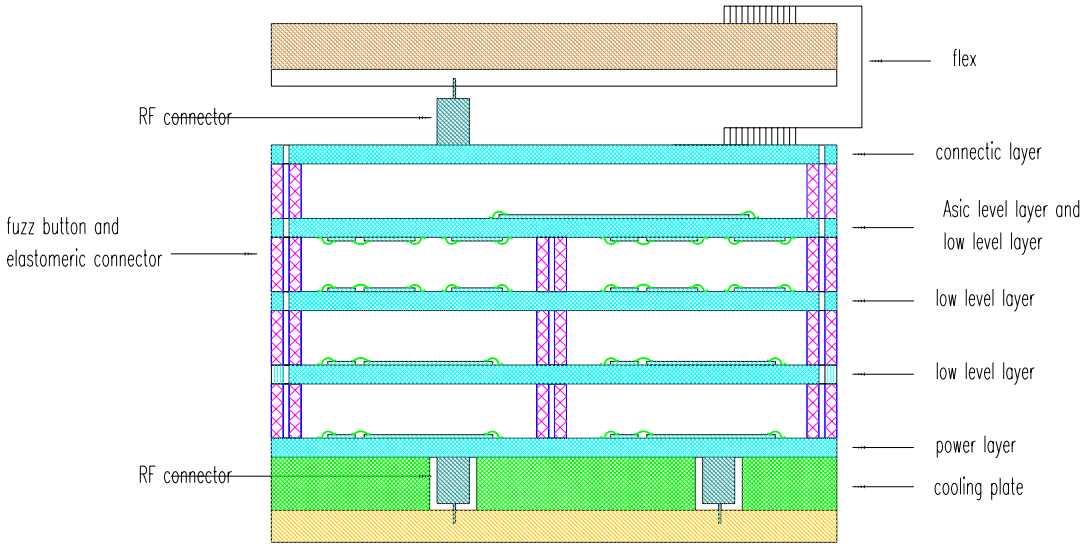

Figure 4.3-24: Integrated radiating element with a TR module [1-2]

4.3.5.3 Stacked Design

A similar concept is presented in Figure 4.3-25. The radiating element are microstrip patches and coupled through a thick brass plate to the Ka-band part of the electronic circuitry. The brass plate provides mechanical rigidity for the module and works as a heat spreader to remove heat from the active circuitry.

A spacer frame provides cavities for the chips and separates the frontend substrate from a distribution manifold board,which routes DC supply power, LO signals, and IF signals to or from the frontend circuits. The frame accepts vertical interconnectors, such as elastomeric connectors or fuzz buttons to provide a solderless interconnection suitable for DC as well as for microwave signals. These connectors will allow the module to be disassembled for rework or repair.

The IF boards are mounted perpendicularly with respect to the antenna surface and frontend substrate. The interconnection of the distribution manifold with the IF boards is established over the edges of the IF boards by solderless connectors inserted in a spacer.

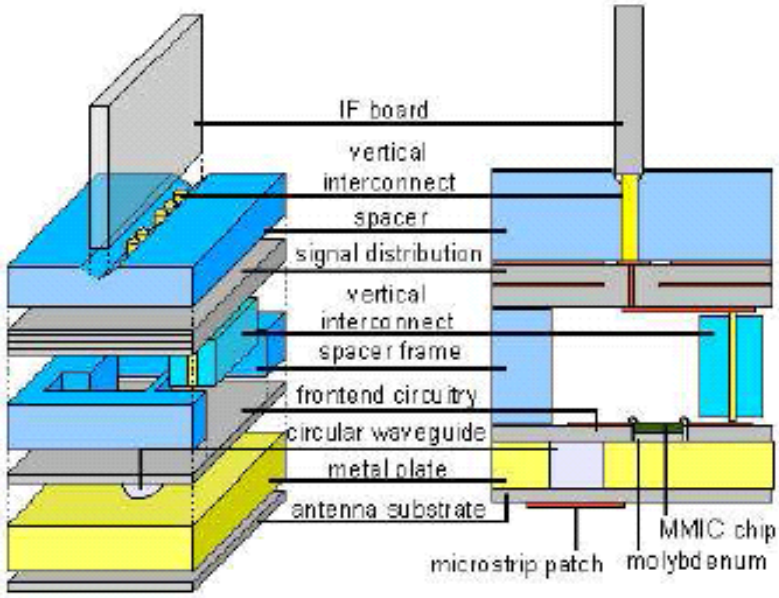

Figure 4.3-25: Integrated feed with digital processing [3]

4.3.5.4 Orthogonal Feeding Design

Orthogonal feeding of the radiating element provides an attractive solution for compact integrated elements. It consists in using a feeding line that is orthogonal to the radiating surface. As the line lies perpendicularly to the radiating element, active circuits (amplifier or phase shifter) can be integrated very close to it without increasing the inter-element spacing.

If the coupling is performed through an aperture coupling excitation, the horizontal ground plane naturally separates the antenna from the feed circuitry. This prevents from parasitic feed radiation and also permits to select adequate substrates for each functionality.

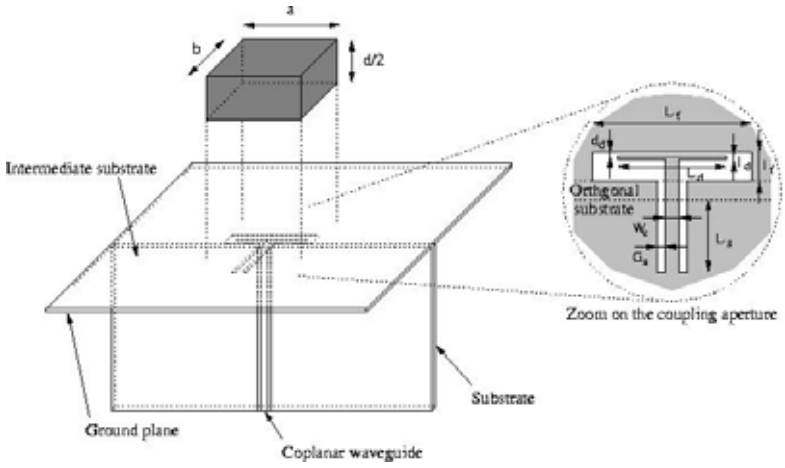

Figure 4.3-26: Dielectric resonator antenna orthogonally coupled with a coplanar waveguide [4]

Such an orthogonal feeding solution has been developed by IETR / ALCATEL, in the case of a Dielectric resonator operating in C band. The feeding line, here a coplanar waveguide on which MMIC circuits or MEMS commands may be implemented, is printed on a vertical substrate that is perpendicular to the horizontal DRA ground plane.

In this development, the dielectric resonator is a rectangular block of Eccostock HIK500 ceramic (Emerson&Cuming) with a 10.0 estimated dielectric constant at the operating frequency (5 GHz). A thick intermediate substrate with a low dielectric constant (ε_r=2.2) is introduced between the ground plane and the resonator. This both enlarges the bandwidth and improves the robustness of the performances in regards to fabrication tolerances.

The orthogonal coplanar line is printed on a vertical 0.635 mm thick alumina substrate (ε_r=9.9). Air-bridges are used along the CPW section to prevent from the slot mode excitation.

This orthogonal feeding preserve a wide bandwidth. The theoretical and measured return loss plots are presented on , indicating a bandwidth of approximately 18 %. The measured radiation pattern is also satisfactory, with a low cross polarisation radiation. Ripple is observed on the E plane plot, due to a small ground plane.

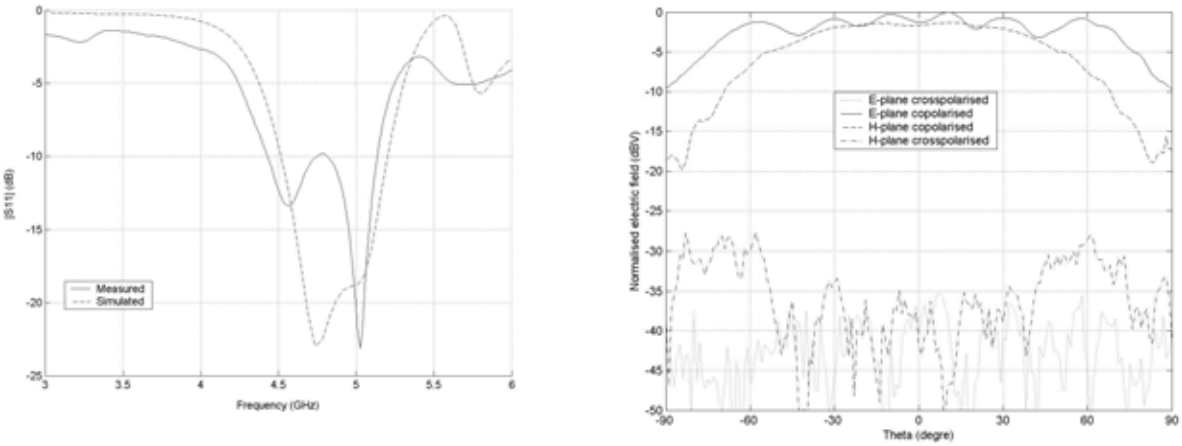

Figure 4.3-27: Theoretical and Experimental Return loss and Measured radiation pattern

Such a radiating element is very interesting for an implementation in an array. A specific technological process is to be identified to make an integrated radiating element, robust to manufacturing errors.

4.3.5.5 References

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4.3.6 Conformal array

There is a particularly strong need to introduce 3-dimensional laser patterning in the printed circuit board industry, widening to applications in aerospace, telecommunications and aviation.

The foreseen application is for instance a conformal microwave antenna for use on board aeroplanes for in-flight communication through satellites, see Figure 4.3-28. This type of antenna is an active microwave reflector, consisting of several layers of circuitry comprising power planes, analogue microwave dipole array circuits, internal routing tracks and an external active digital layer that comprises mounted drivers for the dipole elements on a copper circuit.

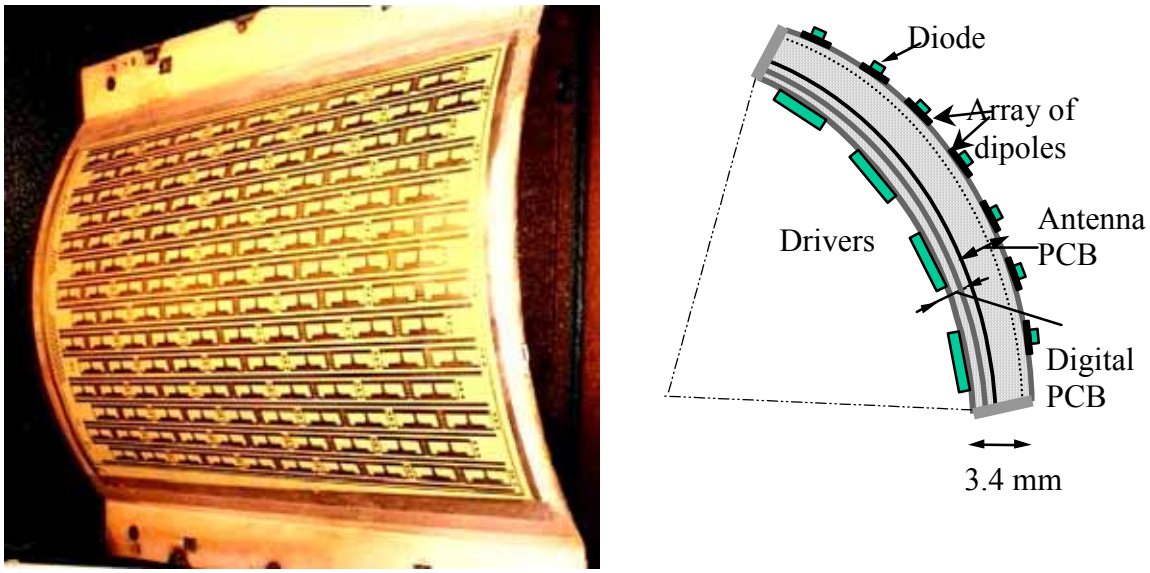


Figure 4.3-28: Typical shape of an active phased array on a aeroplane surface

4.3.7 Homogeneous lens

4.3.7.1 Main features

Dielectric lenses are of particular interest at millimetre- and sub-millimeter wave frequencies. Possible applications are: Mm wave point-to-point and point-to-multipoints links, ACC (Automotive Cruise Control) radars in V-and W-bands, Automotive and train communication systems, Ground stations for LEO satellites, High-platforms altitude communication systems, Imaging systems, Maritime communications in *Ku* band, Satellite multimedia communicatins in Q-band, Inter-satellites links, 4th generation Mobile Broadband Systems, etc.

The flow chart given in Figure 4.3-29 summarizes the different categories of lenses that can be found in literature.

In particular, within the family of lens antennas and substrate lenses, two sub-categories can be distinguished: homogeneous *and* non-homogeneous lenses. In the first case, axis-symmetric, quasi-axis-symmetric or even arbitrarily shaped lenses have been reported. In most configurations, the dimensions of the structures are usually large compared to the free-space wavelength λ_0 (diameter $\geq 6\lambda_0$). A few papers deal with the size reduction of lenses [e.g. 1,8,9,19,22]. The electromagnetic optimisation has been considered recently [7].

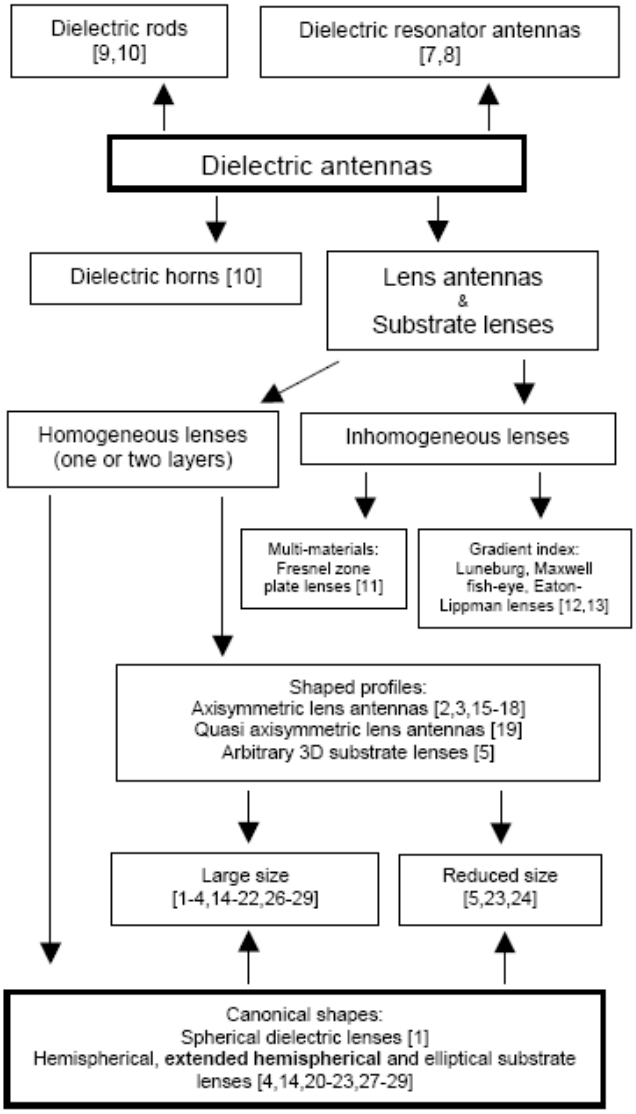


Figure 4.3-29: Dielectric lens technologies (references of this flow chart are given in [1])

In the non-homogenous lens category we can distinguish between multi-material homogeneous lenses and graded index lenses. Research Units (IST, IETR) are currently working on double-shell shaped lenses. IST has been also involved in the design and characterization of planar artificial dielectric lenses [10-13]. This study is motivated by the desire to obtain highly shaped beam integrated lenses totally fabricated with planar integrated circuits technology. LTCC technology could be appropriate for the fabrication of this type of lenses.

4.3.7.2 GO based Lens Synthesis

Geometrical Optics formulation has been used to obtain a first design of lens profiles that are intended to satisfy given radiation pattern specifications. This formulation has been applied to the following type of shaped-beam lenses:

- Single material homogeneous lenses, subject to amplitude pattern template; this includes axial-symmetric, almost-axial-symmetric lenses [2-5,14,15,19] and 3D structures [6,19,21];
- Double-shell lenses, fixed beam, subject to a combination of two design specifications, as for instance far-field template + power transfer efficiency, etc [18];
- Double-shell imaging lenses or scanning beam lenses;
- Graded index artificial dielectric planar lenses, subject to amplitude pattern template [10-13,24].

4.3.7.2.1 Lens Analysis Methods

The solutions coming out from GO formulation are in general used as the initial solution for an optimization process. One key step in the optimization process is the EM analysis of a given lens. The following analysis methods are used:

- Hybrid GO/PO approach, either full 3D or 2D (axial-symmetric), used for large to moderate size lenses compared to λ_0;
- Spectrum decomposition method, specialized for axial symmetric lenses for faster computation times; this method is intended for small lenses [8,9];
- Modal decomposition techniques (plane wave and spherical wave spectrum) for general 3D problems [19];
- Global EM methods, e.g. [1,22].

4.3.7.2.2 Optimization

The Genetic Algorithm global optimization method is being used at IST and IETR for the optimization of single and double shell homogeneous lenses, as well as for arbitrarily shaped lenses. Local techniques, based on the Conjugate Gradient Method, are also available [19].

4.3.7.2.3 Primary Sources

Several kinds of primary sources of lens antennas and substrate lenses have been reported : (1) open ended waveguides, (2) horn antennas and arrays of horns, (3) planar radiating structures (single element or arrays) in coplanar waveguide or microstrip technologies, with broadside or endfire radiation patterns, and with narrow or broad bandwidth, or single layer antennas like double-slots (4) 3D antennas (e.g. helix structure). The prototypes operate in linear or circular polarization.

4.3.7.2.4 Lens materials and lens manufacturing

In the open literature, several kinds of materials have been reported for the fabrication of homogeneous dielectric lenses: foam technology, low permittivity materials such as Teflon ($\varepsilon_r \approx 2.1$), Rexolite ($\varepsilon_r = 2.54$), Plexiglas ($\varepsilon_r \approx 2.53$), polyurethane, polyethylene ($\varepsilon_r \approx 2.33$) materials, fused quartz substrates ($\varepsilon_r = 3.80$), Hi-K ($\varepsilon_r = 4.0$) and Kapton ($\varepsilon_r = 3.87$) materials. The use of higher permittivity substrates (high-ε ceramic ($\varepsilon_r = 6.6$), silicon ($\varepsilon_r = 11.7$) or MgO is also reported. From a fabrication view-point, injection molding techniques, CNC milling, or multi-layer / multi-shell assembly techniques are possible.

4.3.7.3 Advanced Development

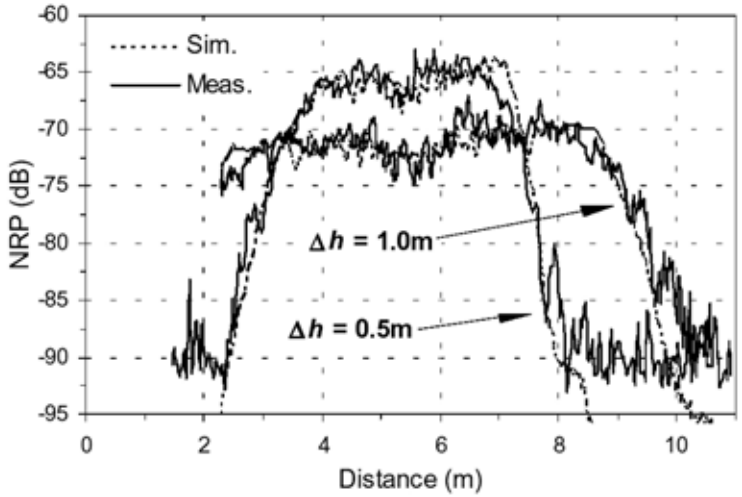
4.3.7.3.1 Axial symmetric lens for mm-wave LAN

Figure 4.3-30a shows an example of an acrylic ($\varepsilon_r = 2.53 - j0.0118$) axial-symmetric shaped lens working at 62.5 GHz to produce a constant flux illumination in a wide room. One characteristic of this antenna concept is that besides producing a constant flux illumination (Figure 4.3-30c) the boundaries of the constant flux region are very sharp, thus avoiding unnecessary illumination beyond the cell limits. The radius of the illuminated region is adjusted just by changing the antenna installation height. This is seen in Figure 4.3-30c for two antenna heights. The lens measured power pattern (Figure 4.3-30d) follows very closely the target radiation pattern [3,4,16].

a)

b)

c)



d)

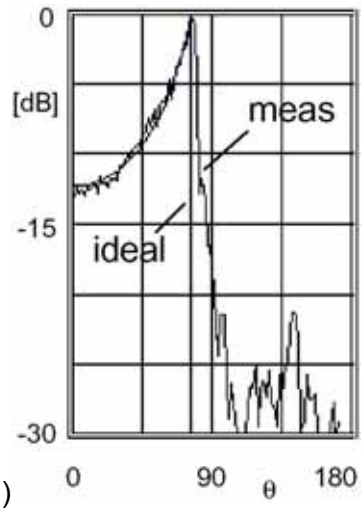


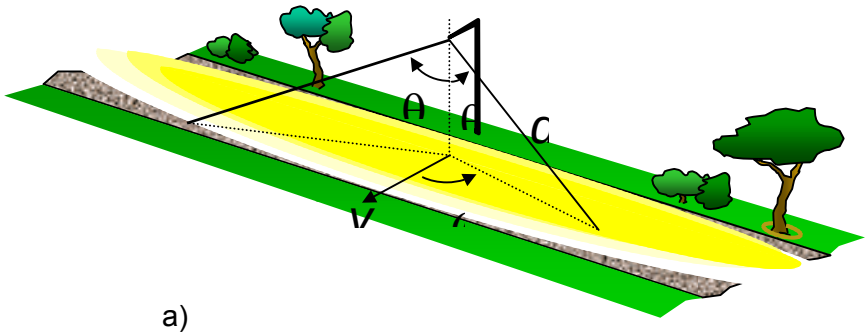
Figure 4.3-30: Axial symmetric acrylic shaped dielectric lens ; a) Lens prototype; b) Lens hanging from a hoist for coverage tests in real environment; c) Coverage results for two lens antenna installation heights. d) Measured lens power pattern superimposed on the target [3,4,16].

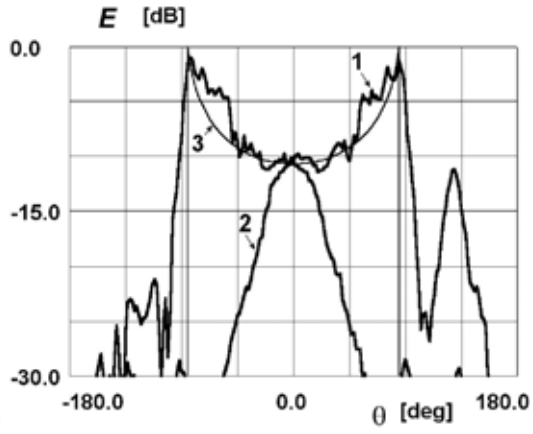
Similar approaches have been applied to design nearly-symmetrical lenses [5] and switched sectored-beam constant-flux lenses [3,16].

4.3.7.3.2 Lenses for coverage of extremely asymmetrical cells

In one of the possible scenarios studied for Mobile Broadband Systems at the 60 GHz band, the base station antenna is required to produce a highly shaped constant flux beam to cover a long section of a narrow street, extending about 100 m at each side of the antenna, with little spillover outside the street limits (Figure 4.3-31a). This is accomplished with the polystyrene lens presented in Figure 4.3-31b. This lens is designed using an approximate method based in axial symmetric lens formulations [2,17,23]. Spatial diversity with two equal lenses is used at the receive channel in order to combat multipath fading.

Figure 4.3-31c shows the measured radiation pattern in the principal planes and Figure 4.3-31d shows the corresponding normalized received power distribution over a 200m section of a street confirming the constant flux characteristic with relatively sharp boundaries.





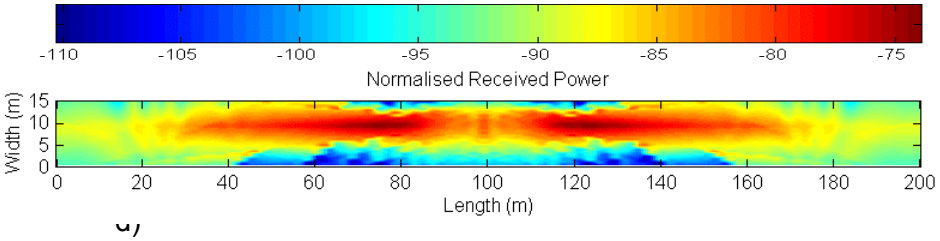


Figure 4.3-31: Shaped dielectric lens antennas for Mobile Broadband Communication Systems. ACTS-SAMBA Project, 42.5-46.5 GHz [2,17,23].

4.3.7.3.3 Arbitrarily-shaped reduced-size lenses for Q-band satellite primary sources

Figure 4.3-32 shows an arbitrarily shaped Teflon lens antenna operating at 49 GHz. The lens has been designed in two steps: (i) design of an approximate lens profile using 3D GO methods [6,19], (ii) local optimization of the resulting profile using PO technique combined with a multidimensional Conjugate Gradient Method [7,19]. The lens is fed by an aperture-coupled microstrip patch antenna and radiates a quasi axis-symmetric beam over the frequency band 47.2-50.2 GHz. The theoretical radiation patterns are given in Figure 4.3-33. They are in good agreement with experimental results [19], as shown in Figure 4.3-33.

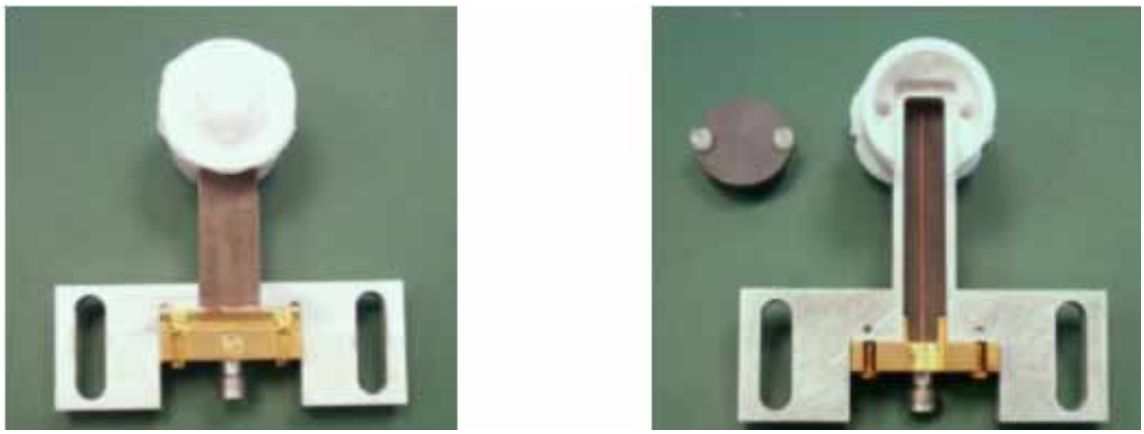
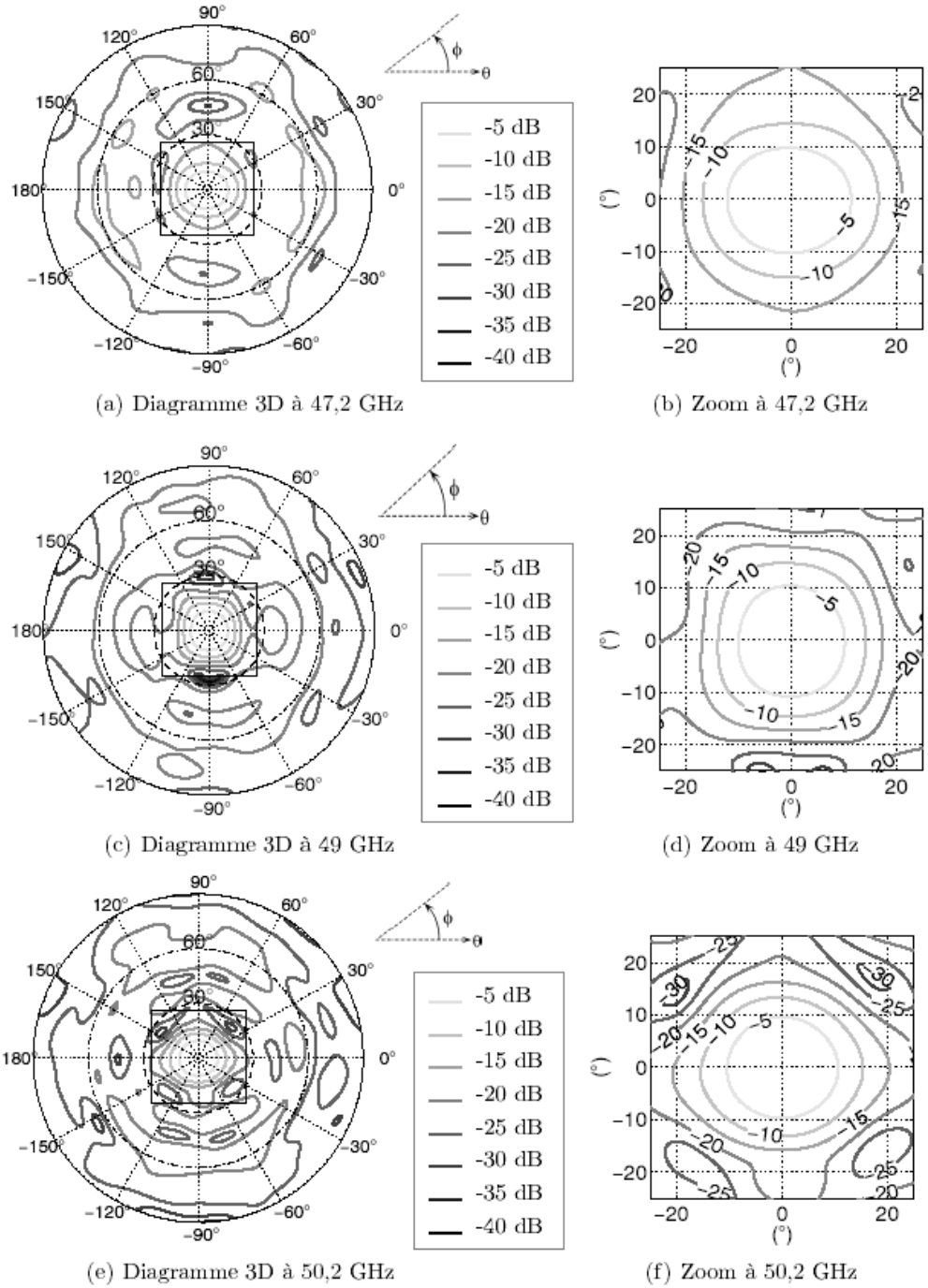


Figure 4.3-32: Arbitrarily shaped lens in Q-band. Lens diameter equals $4.6\times\lambda_0$. Surface efficiency equals 46% [7,19].



(a) Diagramme 3D à 47,2 GHz (b) Zoom à 47,2 GHz

(c) Diagramme 3D à 49 GHz (d) Zoom à 49 GHz

(e) Diagramme 3D à 50,2 GHz (f) Zoom à 50,2 GHz

Figure 4.3-33: Theoretical radiation patterns of the lens antenna represented in [7,19].

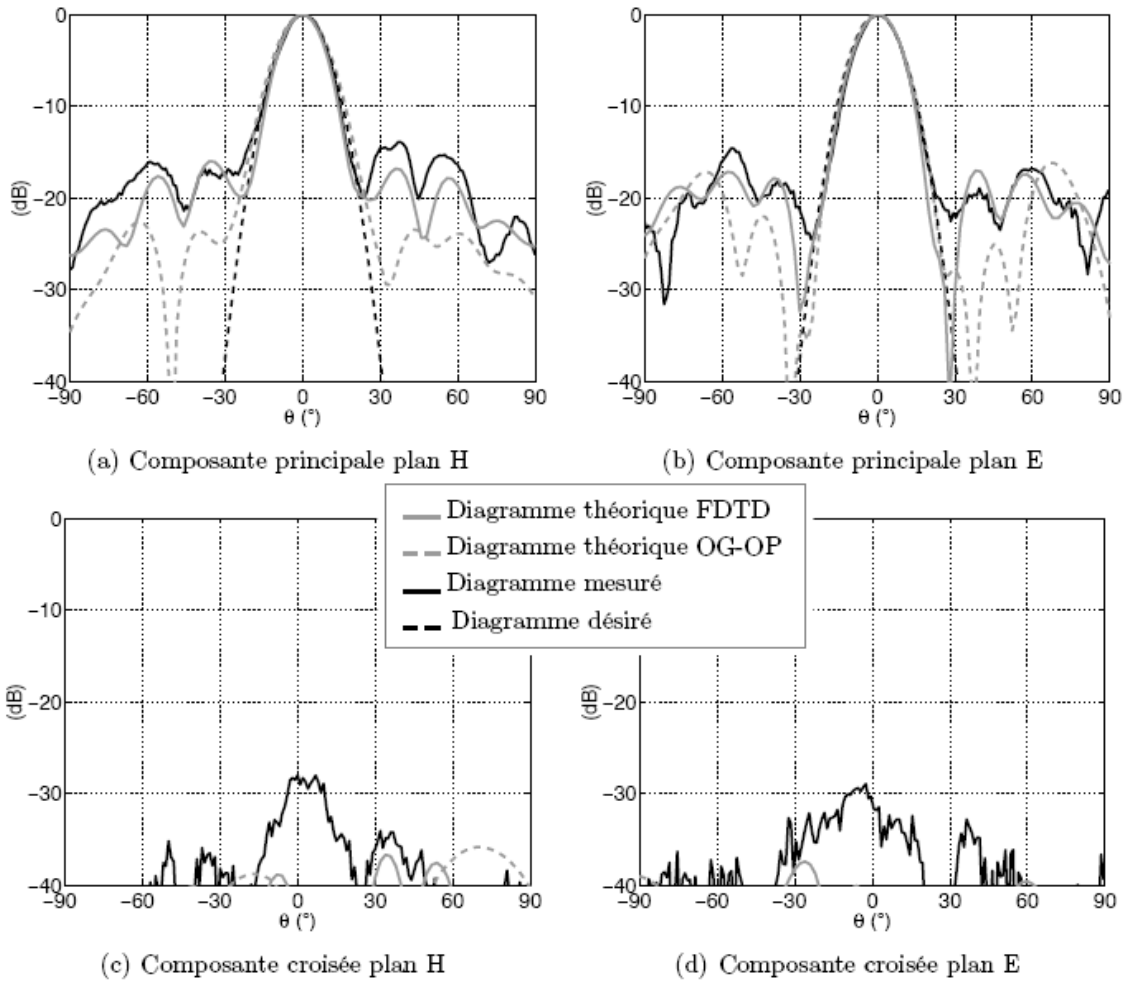


Figure 4.3-34: Comparison between theoretical and measured radiation patterns of the lens antenna represented in [7,19].

4.3.7.4 Future Trends

Size reduction and optimization of lenses (single / double shell structures and non homogeneous metamaterial-based lenses) are currently investigated at IST and IETR. Various optimization criteria are considered: surface efficiency, power transfer transfer efficiency, bandwidth, etc.

Figure 4.3-35 and Figure 4.3-36 show preliminary results on an ultra-wideband focused beam lens (this is a preliminary test for subsequent work on double shell lenses) and a very-high surface efficiency lens, respectively.

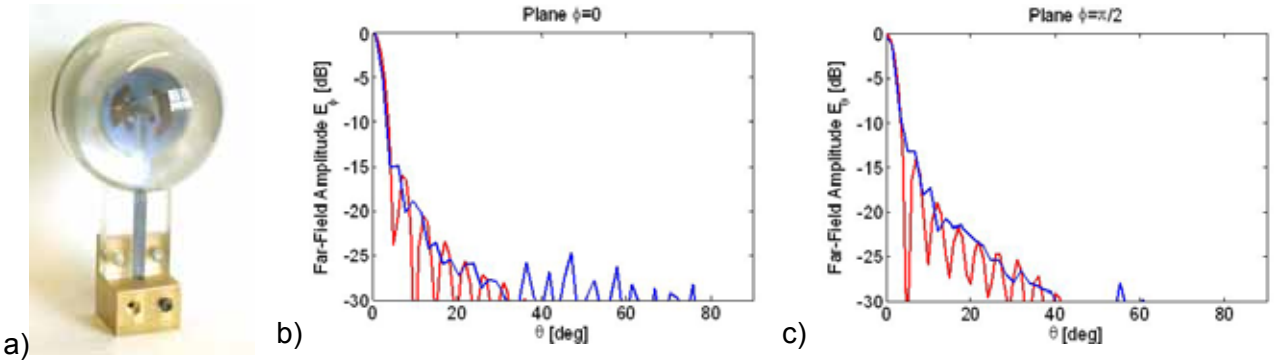


Figure 4.3-35: Elliptical acrylic lens fed by a 1:3 bandwidth log-periodic printed antenna centred at 43 GHz ; a) Antenna prototype; b) E_φ component, φ = 0 plane; c) E_θ component, φ = 90º plane. (blue – measured at 43 GHz, red – simulated with ILASH using GO/PO).

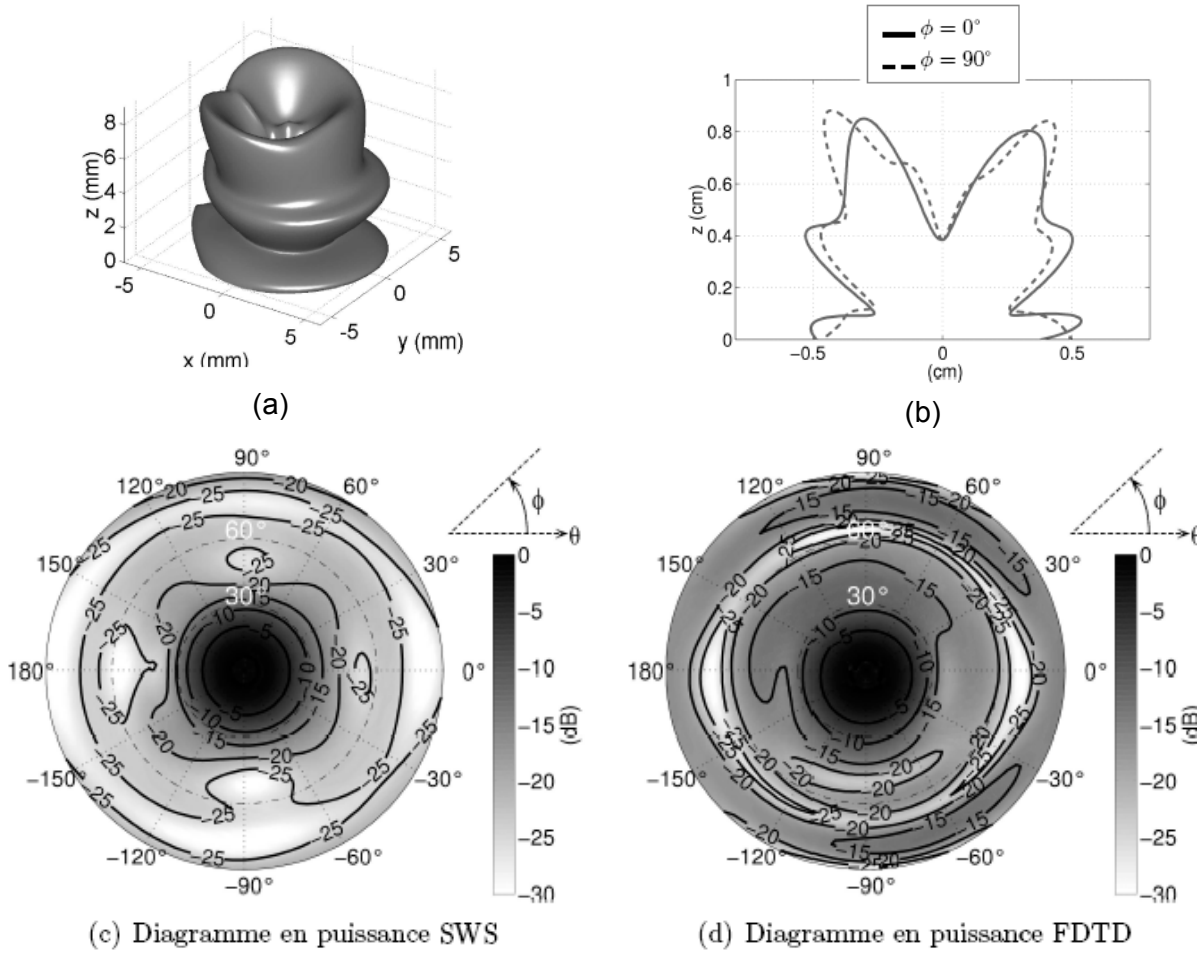


Figure 4.3-36: (a,b) Compact 3D Teflon lens (diameter = $2\times\lambda_0$): (a) 3D profile, (b) Profiles in two cut planes. (c) Comparison between theoretical radiation patterns computed by Spherical Wave (SWS) decomposition and FDTD [19].

4.3.7.5 References

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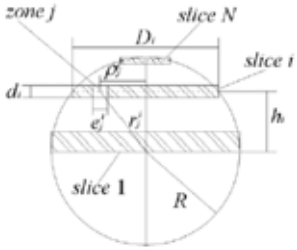
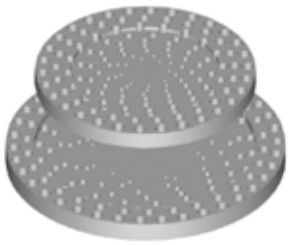
4.3.8 Non Homogeneous lens

The Lüneburg lens represents a very attractive candidate for many applications such as multibeam antennas, multifrequency scanning and spatial scanning, due its peculiar focusing properties. The refractive index n follows the following radial distribution: $n^2 = 2 - r^2$, where r is the normalized radial position. Practically, these lenses are usually manufactured using a finite number of concentric shells. To make easier the fabrication process, the lens can also be divided in parallel slices with a specific distribution of holes to approximate the ideal distribution $n(r)$. The sphere discretization and the consecutive slices are represented in Figure 4.3-37 and Figure 4.3-38, respectively. Figure 4.3-39a and Figure 4.3-39b show the calculating lens assembling, and a photograph of the prototype fabricated in Teflon, respectively.

In [15], authors had the idea of drilling radial holes in a homogeneous dielectric sphere in such their radii change with their position in the sphere in order to produce an approximation of the continuous Lüneburg distribution. The drawback of that is that manufacturer of such lens has to use a tool which can drill in 3D and can change the drilling tool radius. This can be achieved but in terms of complexity, equipment and manufacturing time, the idea has to be changed. A new lens design technique is then described in [15]. The lens is composed of a pile of homogeneous dielectric co-axial cylinders which approximate a sphere as shown on Figure 4.3-38. For a fixed number 2N of cylinders or slices, the radius and the height of each slice are determined by the least mean square method in terms of volume. Now the sphere is completely discretized.





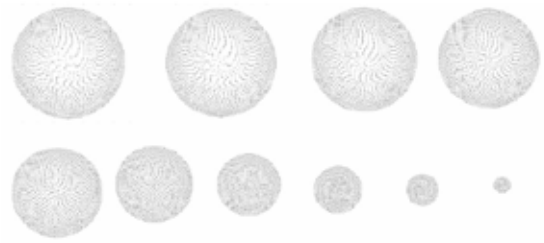


Figure 4.3-37

Figure 4.3-38

Dielectric materials are considered to manufacture the lens and IETR often works with Emerson &Cuming to obtain different kind of dielectric materials.

(a) (b)

Figure 4.3-39: (a) Lens assembling. (b) Fabricated prototype.

A 150 mm radius lens had been built. For simplicity, it comprises 19 Teflon slices with a total number of 23047 drilled holes. The lens radius equals 150mm and the drilled hole have a diameter of 1mm. The obtained drilled hole distribution for each slice is given as follow:

slice index	1	2	3	4	5	6	7	8	9	10	total
drilled hole number	2033	2000	1933	1804	1596	1299	932	579	281	83	23047

During the characterization process, the lens is illuminated by an open-ended WR28 waveguide but could be illuminated too by printed antennas for example. The first step is to optimize the position of the feed respectively to the lens surface. This phenomenon has been checked by measurements. Acoording to Figure 4.3-40, it appears that the termination of the wave guide has to be 21mm far from the lens. The maximum transmitted power occurs at 27.5 GHz. The gain is stable in a wide frequency band (Figure 4.3-41).

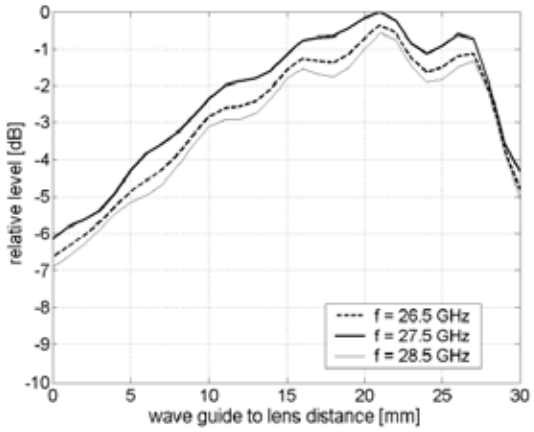


Figure 4.3-40: Relative power versus waveguide to lens distance.

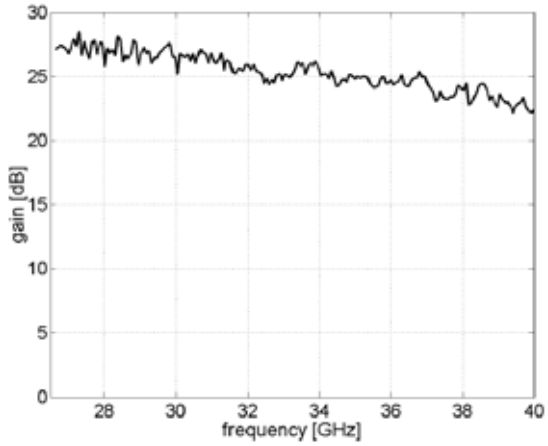


Figure 4.3-41: Power gain

The far field patterns had been measured at 27 and 32 GHz (Figure 4.3-42). It appears that the global shape of the pattern doesn't change significantly.

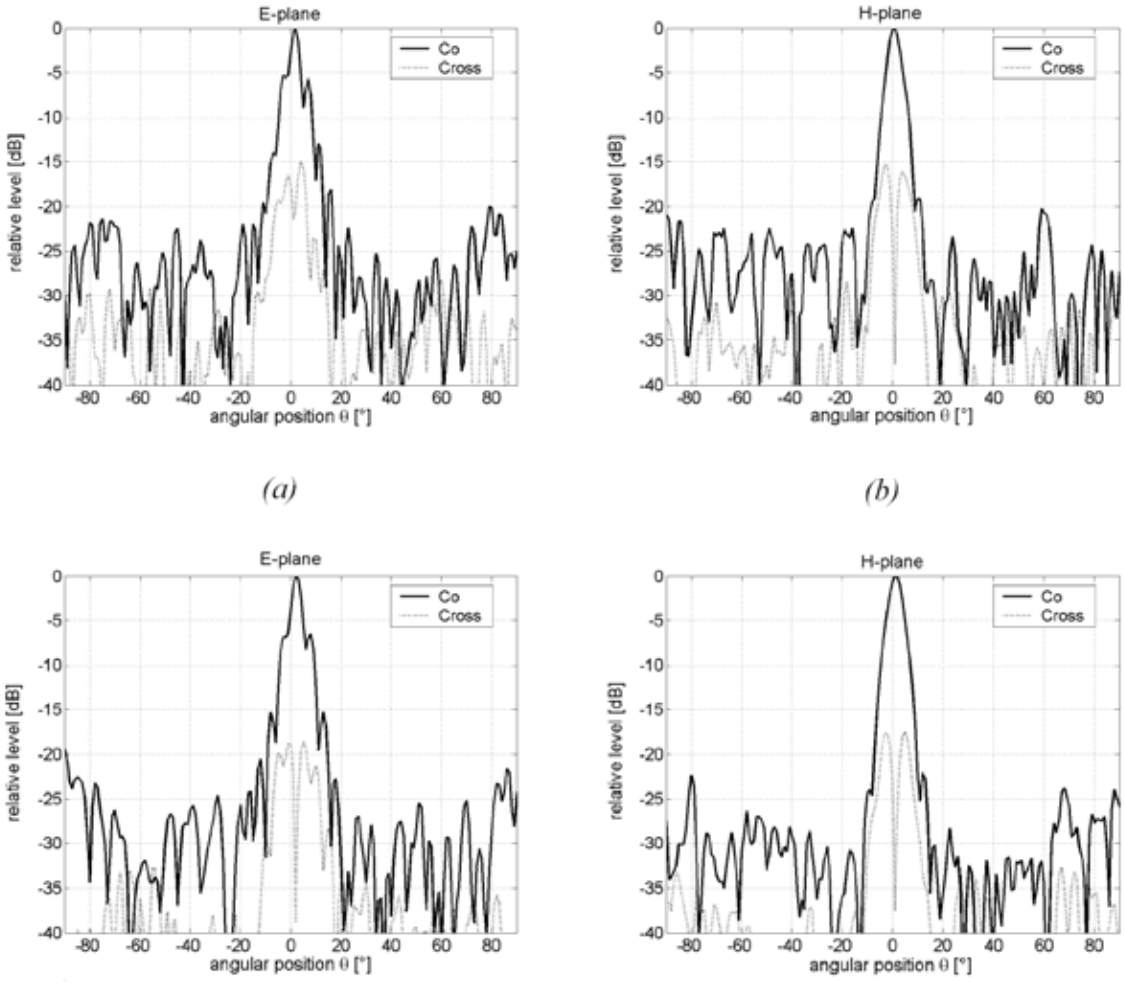


Figure 4.3-42: Far field patterns

The objective could be to use this kind of Non Homogeneous lens to realize multibeam antennas in millimeter waves and particularly for automotive radar application at 77 GHz.

In this case, horn antenna, open ended waveguides or printed antenna can be used to illuminate the Luneburg lens.

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CHAPTER 5

MEMS

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TABLE 5.1-4 : SYNTHESIS OF RF CAPACITIVE RELAYS PUBLISHED IN LITERATURE 8

5. MEMS

MEMS (Microelectromechanical Systems) technology plays a key role in the on-going miniaturization of electronic modules and systems in future telecommunications systems, but also automotive and consumer electronics subsystems. While MEMS operating in the low-frequency region are currently being employed e. g. as acceleration sensors in automotive applications, the field of RF (radio frequency) MEMS is still in a state of research and early development mainly in US and Asia (Radant, Magfusion, OMRON,Hitachi…). RF MEMS switches exhibit excellent RF properties as low power consumption, high linearity, low loss and high isolation. In addition, MEMS can very straightforwardly be integrated into RF subsystems to achieve a higher degree of functionality, for example in active antenna. In the following paragraph, we will describe the technological and design aspects of RF MEMS switches, as well as their potentialities for antenna applications.

5.1 Technological & Design Aspects

5.1.1 RF MEMS

5.1.1.1 Introduction

The different architectures of RF MEMS switches can be classified as in Table 5.1-1. Switches can be either resistive or capacitive and in series or in parallel mode.

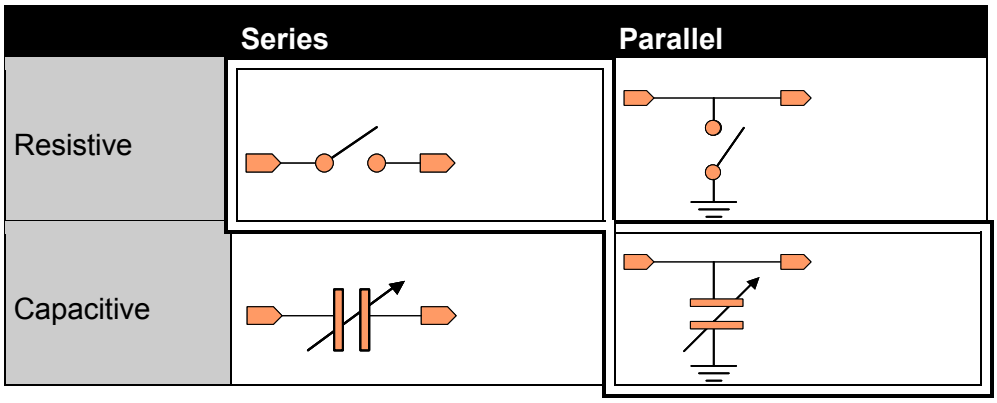

Table 5.1-1 : RF-MEMS switches categories

The two main configurations that are encountered are capacitive shunt switches and series resistive switches. The following paragraphs will detail architectures, give advantages and drawbacks and list typical performances of MEMS switches in those configurations.

5.1.1.2 Principle of Resistive serieS switches and main technology providers

A typical resistive series switch is illustrated in Figure 5.1-1. A cantilever beam is electrostatically attracted to the substrate and closes an open signal line.

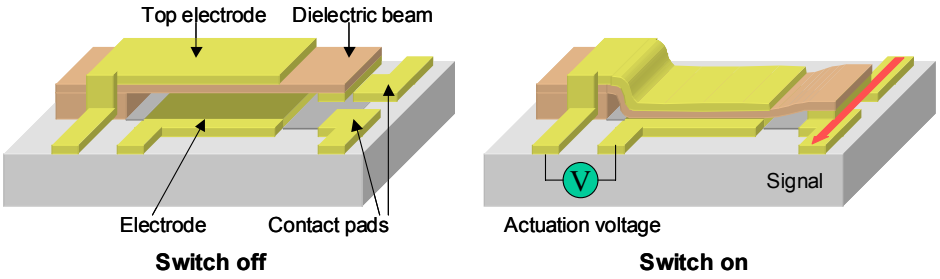

Figure 5.1-1: Principle of a series resistive switch (dielectric beam)

Only this family of switch is able to commute DC to several gigahertz signals. Nevertheless metallic contacts are known to exhibit high adherence energies. High restoring forces are needed to unstick them so beams are generally stiff and high pull-in voltages are necessary. Reliability issues drive to lifetimes in the range of few billion cycles. This switch family has the best electrical performances (very low insertion loss combined with high isolation) and the use of other contact materials is expected to increase the lifetime significantly.

Most designs use composite beams. To date, two main principles are implemented : dielectric beams and metallic beams. Figure 1 illustrates one of them. The beam frame is dielectric and an actuation area is deposited on top of the beam. A contact area is patterned underneath. This principle is used in particular by Rockwell **[CHAN95]**, Hughes Research Laboratories **[HYMA99]** and University of Michigan **[CAI00].**

The advantage of this configuration is the use of a dielectric layer. Generally dielectric stresses are quite controlled but a bilamina effect may occur with temperature due to the difference in thermal expansion coefficient between top electrode and dielectric beam. To cope with this problem, the Hughes Research Laboratory in particular has studied the deposition of an other level of dielectric on top of the metallic electrode. Thus, stress and thermal elongation are compensated. The second advantage of this configuration is that the dielectric is generally stiffer than metals. In consequence the dynamic properties of these switches are generally better than for metallic ones. The main drawback is a relatively high actuation voltage. As the dielectric beam is at least 1µm thick, the actuation voltage will always be higher than in a configuration where a thin dielectric is deposited directly on the bottom electrode.

The other principle, illustrated by Figure 5.1-2, is based on a metallic beam (or conductive beam). The contact area are electrically isolated with a thin dielectric pattern. This particular beam shape is used by Analog Devices and is based on a technology originally developed at NorthEastern University. This principle is also used by others laboratories like NEC **[SUZU99]** and KAIST **[HAH00].**

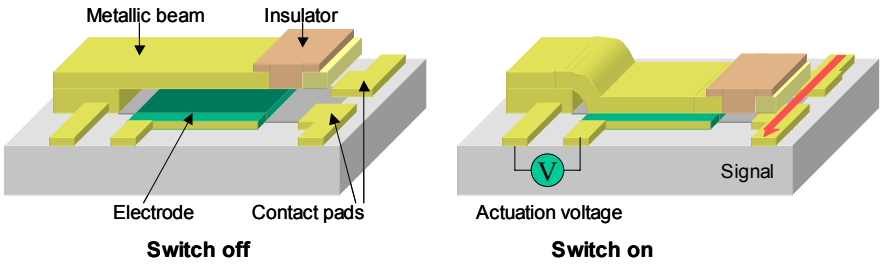

Figure 5.1-2: Principle of a series resistive switch with a metallic beam

The processing of metallic beam switches is generally simpler than the one of dielectric beam switches. Nevertheless, as metals are less stiff than dielectric, the thickness is generally increased up to 1.5-2µm or more and stress gradient problems may occur. Stress is more difficult to control in metals than in dielectric and these structures are more sensitive to creep. However, the actuation voltage can be optimized more easily and, in some cases, process temperatures are IC-compatible (for monolithic integration).

These two principles can also be the basis of membrane resistive switches. For example the resistive switch from Samsung is based on the metallic beam principle illustrated in Figure 5.1-3.

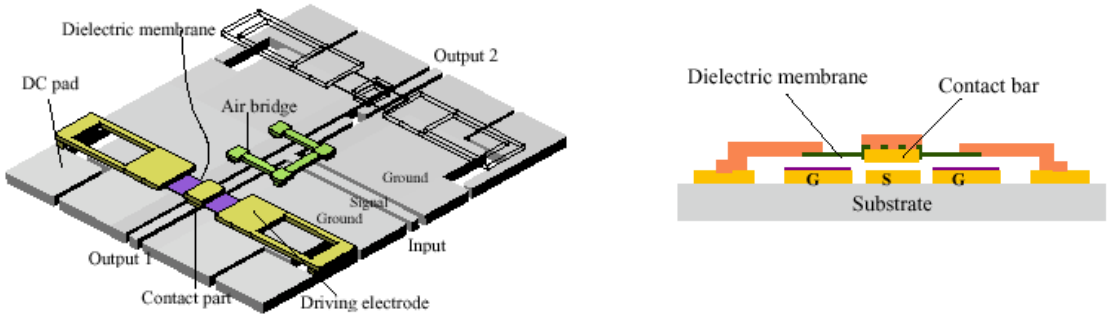

Figure 5.1-3: Schematic view and cross sectional view of the Samsung switch

This principle is also used by Infineon **[INFI01]**, University of Michigan **[MULD00]**, NTT **[HIRA99]**, Omron **[SAKA99]**, Institute of micro-technology of Neuchatel **[GRET94]**, **[FULL98]**, and others.

The main concern in metal-based based membrane resistive switches is mechanical stress. As the dimensions are large, stress problems (intrinsic and gradient) are often reported. An other drawback is the process complexity. Most of the time, more than 10 masks are used (up to 18) and the processing cost is too expensive compared to existing technologies. In the last five years, several consortium and research projects aborted because of this matter, even if performances were amongst the best ever published. Current trends tend to simplify the processes and optimize the working conditions. Recently, research laboratories have started work dealing with the resistive switch principle because only resistive switches are able to commute DC-2GHz signals.

Table 5.1-2 reports performances and characteristics of some RF series resistive switches.

Laboratory	Year +Refs	Principle	Insertion loss	Isolation	Switching speed	Others
CEA-LETI	2003	Electrostatic	0.2 Db	< 25 Db @ 40GHz	< 1µs	DC-90 GHz operation
Samsung Adv. Inst. of Tech. (SAIT)	2000 [SAIT01]	Electrostatic composite membrane	0.09Db @2GHz	46Db @2GHz	N/A	V_{bias}=3V Frequency range = DC-10GHz
Infineon	2000 [INFI01]	Electrostatic polysilicon membrane	<0.5Db @1GHz	>15Db @1GHz	N/A	V_{bias}=10-23V Frequency range: DC-6GHz
Korea Adv. Inst. of Sc. and Tech. (KAIST)	2000 [HAH00]	Electrostatic composite torsional beam	<2Db @?	>28Db @?	N/A	V_{bias}=5-25V freq range = [DC-4GHz]
Radiation lab, university of Michigan	2000 [MULD00]	Electrostatic metal membrane	~0.5Db	>30Db @30GHz	N/A	V_{bias}=15-25V Frequency range = 30GHz
Hughes Research Labs	1999 [HYMA99]	Electrostatic composite beam	0,2Db @DC-40GHz	50Db @DC-40GHz	20µs	V_{bias}=30V mechanical lifetime: 10^9 cycles electrical: 10^6 cycles
NEC	1999 [SUZU99]	Electrostatic composite beam	<0.2Db @30GHz	>13Db @30GHz	N/A	V_{bias}=50-100V
Radiation lab, university of Michigan	1999 [CAI00]	Electrostatic composite cantilever	<0.4Db @2GHz	>38Db @5GHz	N/A	V_{bias} = 20V (simulated) Frequency range = DC-40GHz
Rockwell Science Center	1995 [CHAN95]	Electrostatic composite cantilever	0,1Db @40GHz	50Db @40GHz	30µs	V_{bias} >28V, E=1.4 µW R_{on}=0,22 mΩ $>10^{10}$ mechanical cycles

Table 5.1-2 : Synthesis of RF resistive relays published in literature

Table 5.1-3 reports performances and characteristics of some DC series resistive switches.

Laboratory	Year +Refs	Principle	Contact resistance	Commutation time	Bias voltage	Others
IRCOM, U of Limoges	2004	Electrostatic	0.5 Ω	5-20 µs	40-60 V	Process available on various substrate
Radant Inc.	2003	Electrostatic	0.5 Ω	+10-20 µs	40-60 V	Up 10^{10} cycles Up to 1 W CW hot switching
Magfusion	2003	Electromagnetic		500 µs	5V-100 Ma pulsed	10^9 cycles
NorthEastern university –Analog Devices	2000 [AD01] [MAJU98] [MAJU97]	Electrostatic resistive cantilever	0,5 Ω	6 µs	20-60V (in 1997)	P=0,3Mw C_{off}=50Ff V_{arc}=150V 10^9 cycles price=$16
CRONOS	2000 [CRON00]	Electrothermal resistive	0,4 Ω	8 ms	6 V	P=150Mw I_{max}=50Ma $Freq_{max}$=30Hz Contacts : or-nickel V_{arc}>1500V >10^6 electrical cycles
Omron	1999 [SAKA99]	Electrostatic silicon membrane	N/A	0.3ms	24V	Lifetime: 10^6 cycles
NTT	1999 [HIRA99]	Electrostatic metallic membrane	5 Ω	2 µs	15V	P=75 µW $Freq_{max}$=10kHz Contacts Au
CSEM CP CLARE IMEC SPEA ARITECH	1998 [FULL98]	Electromagnetic membrane	0,4 Ω	2 ms	1,9 V	P=16Mw V_{arc}=200V $Freq_{max}$=500Hz >10^6 mechanical cycles
TELEDYNE – Georgia Institute of Technology	1998 [TAYL98a] [TAYL98b] [ALLE98]	Electromagnetic membrane	< 50 mΩ	2,5 ms	180Ma	P=33Mw $F_{contact}$=2,5Mn gap=10µm I_{max}=1,2A >10^6 electrical cycles
Fraunhofer Institute	1998 [SHIE98]	Electrostatic cantilever	10…80 Ω	2,6-20µs	20-100V	P=1–4,5µW I_{max}=1Ma
New Jersey Institute of Technology	1998 [SUN97]	Electro-thermal and electrostatic composite beam	2,1…35 Ω	0,5 ms	–	P=12Mw+10Mw V_{arc}=400V 10^5 cycles
Siemens	1997 [SCHL97]	Electostatic cantilever	0,02…1 Ω	0,2ms	12-24V	P=7µW $F_{contact}$=1Mn V_{arc}>300V I_{max}=100Ma shocks > 1000g >10^8 mechanical cycles

Table 5.1-3 : Synthesis of DC resistive relays published in literature

5.1.1.3 Principle of Capacitive shunt switches and main technology providers

Unlike DC signals, RF signals can be commuted with a mobile ground plane. Indeed, if a ground plane is attracted close enough to the signal line (typically few tenths of micrometers), the signal is shunted to the ground and the transmission is interrupted.

To realize such a switch, two architectures are suitable. The first introduced is the airbridge switch (see Figure 5.1-4). The airbridge relies electrically two ground planes over the signal line. The bridge pull-down is obtained by combining a bias voltage with the RF signal. The bias voltage creates an electrostatic force that pulls down the bridge to the signal line. A dielectric layer deposited on the signal line, prevents any DC electrical short-circuit between signal line and bridge.

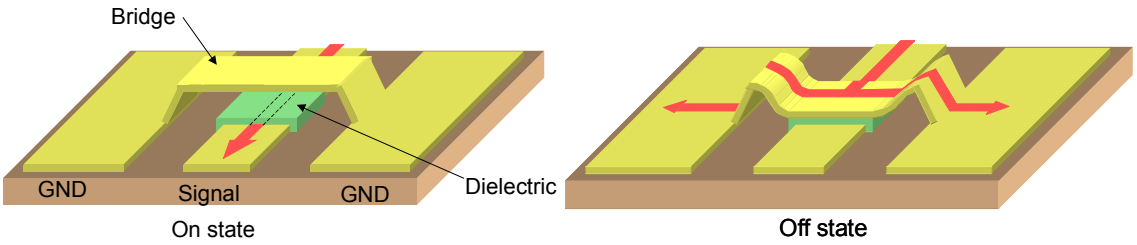

Figure 5.1-4: Principle of the electrostatic capacitive bridge

The advantage of the air bridge configuration is the relatively small size of the suspended part (200 to 400µm long). Stress is then easier to control compared to other configurations. The second advantage is a simpler process flow than the other families of RF-switches (cost advantage). Generally not more than 5 masks are used.

The main drawback of this switch is the relatively high actuation voltage which results from the relatively small attraction area of the membrane. Typically, actuation voltages below 35-40V are difficult to reach. If the bridge is not stiff enough then stiction at the release step may occur.

The second configuration uses a membrane instead of a bridge (see Figure 5.1-5). In this case, the membrane is not connected to the ground. The membrane covers a larger area and generally overhangs all the transmission lines (grounds lines and signal line). In this configuration, the bias voltage is directly applied on the membrane. The electrostatic force is created between the membrane and the entire overhung CPW (the two ground lines and the signal line). As previously, a thin dielectric prevents short circuit between membrane and lines.

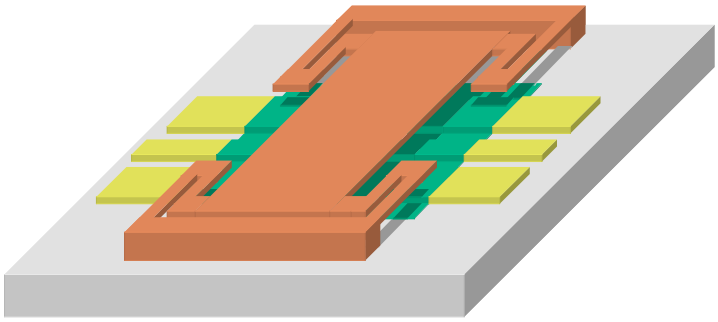

Figure 5.1-5: Principle of the electrostatic capacitive membrane

In this configuration, the membrane is generally designed stiff and flexure joints are used. Those switches have the lowest actuation voltages reported (15V). Moreover, the bias drive is separated from the signal line.

A drawback of this configuration is the stress control in the membrane. This one is difficult to stabilize over such scales (from 500 up to 700µm). A stiff membrane means also additional layers on top (additional masks) or a longer processing time (increased layer thickness) that will conduct in both cases to an increased sensitivity to inertial and thermal issues.

From a global view, capacitive parallel switches, when stiff enough, are less sensitive to stiction compared to resistive ones. Processes are generally more simple (no need for a contact mold or composite membranes). Nevertheless, because they are capacitive, performances are suitable for frequencies greater than several tens of GHz but power capability has not been demonstrated yet. Moreover, oxide trapping and oxide lifetime are the important concerns in this family.

Table 5.1-4 reports performances and characteristics of some RF capacitive shunt switches.

Laboratory	Year +Refs	Principle	Insertion loss	Isolation	Comm. time	Others
LAAS CNRS	2003	Metallic bridge	0.1-0.2 Db @30 GHz	15 Db @30 GHz	N/A	Very low loss technology on dielectric membrane
IMEC	2003	Electrostatic bridge	0.5 Db @ 20 GHz	40 Db @ 20 GHz	-	Metal contact switch with metal floating electrode V_{bias}=20-40V
BOSCH	2001 [BOSC01]	Electrostatic metallic bridge	0.3Db @94GHz	33Db @94GHz	40-100 µs	V_{bias}=24V
LG	2000 [PARK00a] [PARK00b]	Electrostatic metallic membrane	<0.1Db @10GHz	>40Db @5GHz	N/A	V_{bias}=8V Frequency range >4GHz
Raytheon	1999 [YAO99] [GOLD98]	Electrostatic bridge	0.14Db @20GHz 0.25Db @40GHz	24Db @20GHz 35Db @40GHz	6µs 4µs	V_{bias}=50V E=10Nj C_{on}/C_{off}=100 C_{on}=3-4Pf FoM=9THz
Technische univ. München	1999 [VIET99]	Electrostatic bridge	0.1Db @20GHz 0.25Db @40GHz	25Db @20GHz 35Db @40GHz	–	–
University of Michigan	2000 [TAN00]	Electrostatic metallic bridges	0.8-1Db @30GHz	>25-30Db @30GHz	N/A	V_{bias}=25-30V
	1999 [MULD99]	Electrostatic bridge	0.6Db @22-38GHz	40Db @20GHz 50Db @40GHz	–	V_{bias}=15-20V C_{off}/C_{on}=22 C_{on}=1.1Pf C_{off}=0.05Pf
	1998 [BARK98] [PACH98]	Electrostatic metallic bridge	0.2Db @2GHz	30Db @40GHz	–	V_{bias} =14-16V
University of Illinois	1999 [SHEN99]	Electrostatic metallic membrane	0.5Db @40GHz	27Db @40GHz	–	V_{bias}=14-17V $R_{on\ eq.}$=0.3Ω C_{off}=90Ff
Rockwell Science Center	1998 [BROW97]	Electrostatic membrane	0.4Db @1GHz 1Db @40GHz	50Db @1GHz 25Db @40GHz	–	–

Table 5.1-4 : Synthesis of RF capacitive relays published in literature

5.1.1.4 Other Architectures of Switches

Others families of switches are resistive parallel switches and capacitive series switches. They are both rarely implemented because they offer lower electrical performances than the previous configurations and sometimes architectures are more complex.

An interesting architecture is the one proposed by Berkeley using both series and parallel resistive principles. The switch is based on a torsional beam. The combination of both principles offers good isolation (>40 Db) and insertion loss (< 0.12Db) in a large frequency range (DC – 40GHz). The implementation of the device is illustrated in Figure 5.1-6.

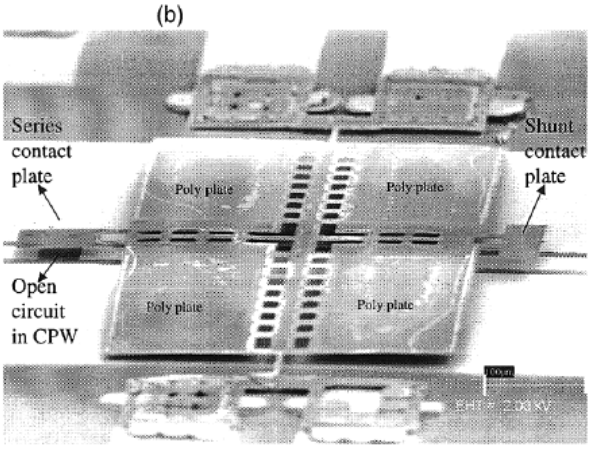

Figure 5.1-6: SEM view of the series-shunt switch of Berkeley

Even though the principle is interesting, the process is quite complicated (membrane is flip-chipped), the gaps are not totally reproducible and a high stress gradient is observed.

An example of a capacitive series switch was reported by Chuck Goldsmith in 1995 [**GOLD95**]. Cross-section and top-view of the switch are illustrated in Figure 5.1-7. The membrane is connected to the RF signal input line. An electrical field applied between the membrane and the actuation pads actuates the membrane and provides a capacitive coupling between the RF-input and the RF-output. The actuation voltage is determined by the size of the membrane.

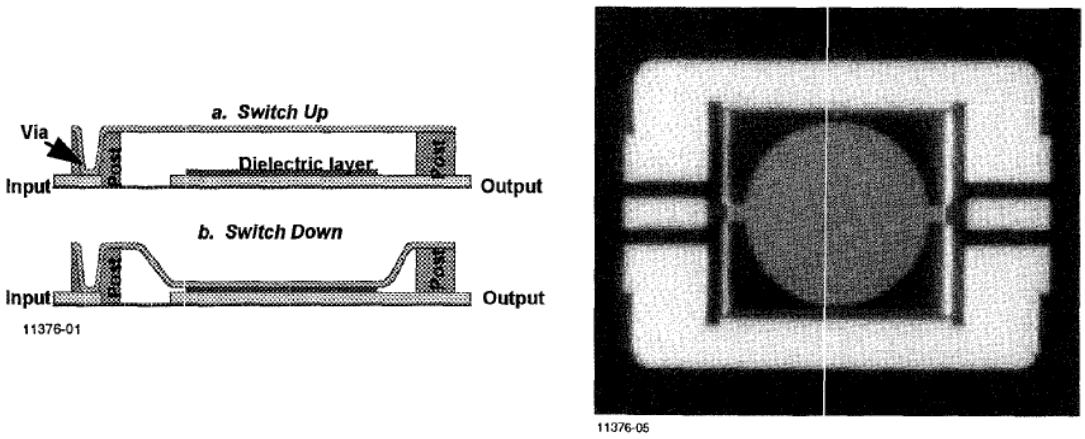

Figure 5.1-7: Cross-section and top view of the series capacitive switch of Texas Instrument

Performances were rather low :

Frequency range:	0.2-20GHz
Actuation voltage:	7-70V depending on membrane size
Isolation:	~15 Db @ 10 GHz
Insertion loss :	0.3-0.5 Db @ 10 GHz
Switching speed :	6 μs

According to our knowledge, this configuration has not been reused.

5.1.1.5 Synthesis

Several configurations of switches exist for the RF signals switching. RF-switches can be resistive or capacitive and series or parallel. Published switches are mostly resistive series or capacitive parallel. The first family is dedicated to the DC-5GHz frequency range whereas capacitive shunt switches are dedicated to higher frequencies (more than 10GHz). Even if the figure of merit of resistive switches is better, capacitive ones exhibit better reliability figures.

Capacitive switches can be divided in two sub-families : bridge and membrane switches. Air-bridge switches are smaller than membrane ones. They are easier to stabilize and are, at this time the more mature switch family. They offer good performances (in terms of electrical losses and lifetime) and process flows are of the simplest.

5.1.2 Type of actuation

5.1.2.1 Introduction

In the MEMS world, several principles exist for actuation at micro-scale. Between them, we can distinguish electrostatic, electromagnetic, electrothermal and piezoelectric actuators. Each of them has its own strengths and weaknesses.
This chapter aims at presenting the performance criteria of an actuator for resistive or capacitive switches. Then, we will present the principle of each family of actuator.

5.1.2.2 Performance criteria

Actuation plays an important role in the switch cycle. In one hand, it drives the dynamical performances (switching speed, power consumption, mechanical lifetime, etc.) and on the other hand, it affects the contact performance. Parameters such as contact and restoring force are directly actuator dependant.

In resistive switches the contact area depends on the applied force. Asperities of contact are deformed by the mechanical force. In consequence, the more the asperities are deformed, the lower is the contact resistance (i.e. the insertion loss). In particular, it has been demonstrated that forces in the range of Mn are needed to deform the asperities plastically.

In capacitive switches, deformation of asperities in contact is not required. Nevertheless, E. K. Chan showed that, in electrostatic membranes, actuation voltages greater than the pull-in voltage increase significantly the deformation of the membrane and thus the capacitance (see Figure 5.1-8). As a thumb rule, voltages 6-7V greater than the pull-in voltage guaranty a good mechanical contact [**GOLD01**].

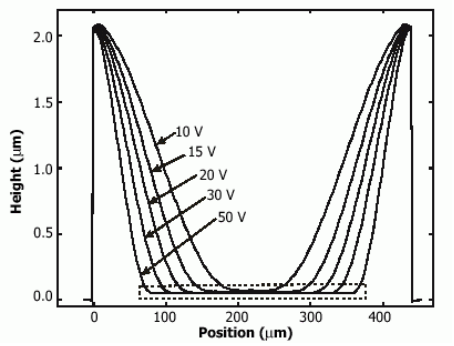

Figure 5.1-8: Surface profile measurements of 440μm long bridge at different actuation voltages

The restoring force is also an important parameter in resistive switches. In metallic contacts, because of high adhesion energies and micro-welding of asperities, high restoring forces are needed to separate the contact surfaces. In macro-relays, this force is usually two to three times greater than the contact force.

In capacitive switches, the contact stiction phenomenon is different. Most of the time, it is due to charge trapping in the dielectric. Trapped charges create a parasitical electrostatic field. This phenomenon is time dependent (from few seconds to several hours or days). Experimental results are reported in [**GOLD01**]. An other issue is the stiction due to capillary forces of surface condensed water. The adhesion energy induced by those parasitical films is dependent on material and environmental conditions. Several methods are published to quantify them.

Regarding performances directly related to the actuator design and technology, the switching speed is an important issue for Telecommunication applications. In order to compete with solid state switches, commutation times have to be as short as possible, typically in the range of tenths of microseconds. Existing micro-electromechanical systems does not reach such a speed requirement. In literature, the fastest switches which are based on electrostatic actuation offer a speed in the range of 10μs.

Finally bias power for telecommunication applications has to be as low as possible. In particular for mobile applications, the actuation voltage should be at best 3V and not greater than 10-11V. At this time, only electromagnetic actuators can withstand such specifications. Electrostatic actuators with actuation voltages below 15V can be affected by stiction and inertial issues.

5.1.2.3 Electromagnetic actuators

While electromagnetic actuators are the basis of macroscopic electromagnetic relays, they are sparsely used in MEMS. The main reason is that electromagnetic material is not used in classic microelectronic processes. The first actuators were derived from hard drive technologies. Although only few research centers mastered the technology, most of manufactured electromagnetic relays exhibited good performances in terms of electrical losses and dynamical behavior. Several configurations will stay prototypes because of their high processing and assembling cost. However recently, DowKey announced the first MEMS switch for RF applications, and Teledyne and Micromachine are still potential providers of MEMS switches based on electromagnetic actuation.

Today, two elementary electromagnetic actuators have been reported. The first one produces a vertical or out of plane displacement, the other one, a horizontal or in-plane one.

The first actuator principle is illustrated in Figure 5.1-9. A planar inductor provides an electromagnetic field that pulls a ferromagnetic membrane down.

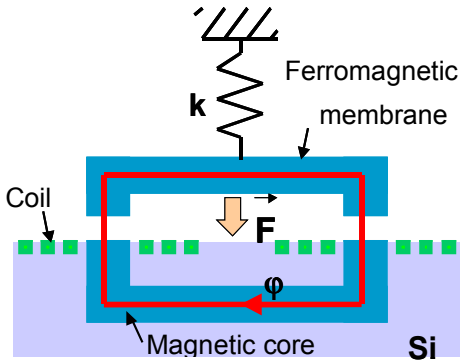

Figure 5.1-9: Principle of the vertical electromagnetic actuator

Actuators based on this principle are able to produce contact forces in the range of few milli-Newtons [**TAYL98b**]. However the use of these specific structural materials needs new characterization in particular for the modeling of restoring forces.

The second type of actuators is the integration of the well known electromagnetic coil (see Figure 5.1-10). A conducting wire is wrapped round a magnetic core. The created magnetic flux is larger than the one obtained with planar inductors. An arm of the core is bent and tends to close the magnetic circuit. This actuator should produce higher forces than the previous configuration but, from our knowledge, this principle has not been implemented for signal switching.

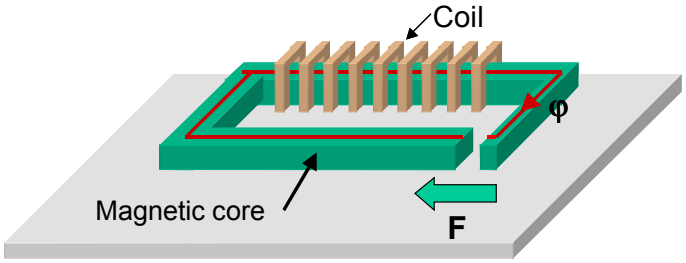

Figure 5.1-10: Principle of the horizontal electromagnetic actuator

In conclusion, despite complex manufacturing processes, magnetic actuators are suitable for DC or RF signal switching.

5.1.2.4 Electrostatic actuators

Historically, the first implemented relay was based on an electrostatic actuation. As for the electromagnetic actuator, also here two types exist. The first one is for out of plane displacements, the second one for in-plane displacements.

The first one (used mostly in MEMS switching) is described in Figure 5.1-11.

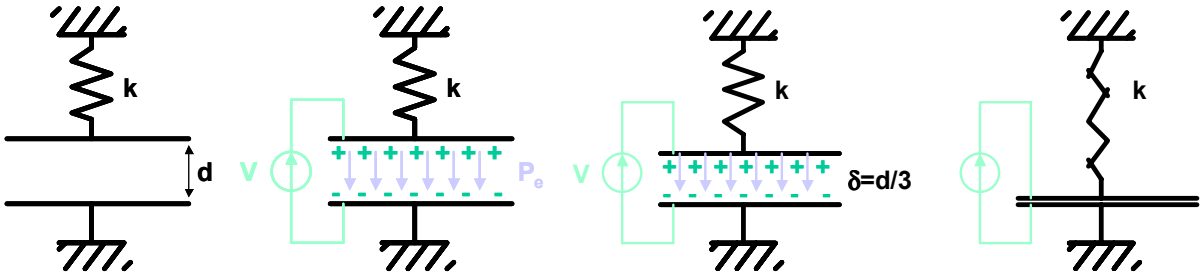

Figure 5.1-11: Principle of the vertical electrostatic actuator

The system is composed of two capacitive plates. One is fixed, the other is mobile. When they are biased, electrical charges create an electrostatic field that pulls down the mobile plate. As the mobile electrode is pulled down to the bottom electrode, the gap is reduced and the pull-down force on the switch increases. On the other hand there is a pull-up force due to the spring constant of the switch. This behavior is linear up to the third of the gap (d/3). When the gap is lower than d/3, the closing force increases more rapidly than the restoring force which leads to a sudden collapse of the switch to the down-state position.

This particular mode is well suited for switches: the contact force is maximum at the end of displacement. Moreover this instability offers fast a switching time (typically few tens of microseconds).

The power consumption of this actuator is very low when an electrode is passivated with a thin dielectric layer. The power consumption is then due to the charging and discharging of electrodes (at transient states).

The second type of actuator is used for in-plane displacements. The principle is illustrated in Figure 5.1-12.

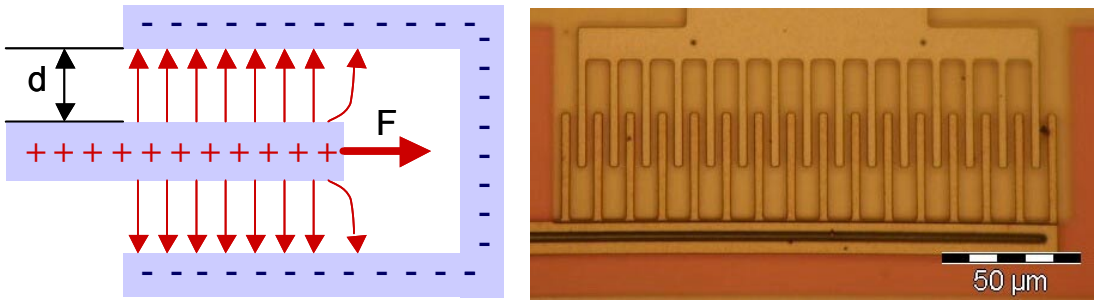

Figure 5.1-12: Principle and optical view of an electrostatic combdrive actuator

As force is exerted only at the beam extremity, this one is relatively low. This actuator produces typically several tens of micro-Newton, hundreds at best. Nevertheless travel distance is important (up to several tens of micrometer). Finally this actuator is well suited for technology with thick structural layers such as SOI and has not been used for signal switching.

5.1.2.5 Electrothermal actuators

The electrothermal actuator is based on the thermal elongation difference between two different materials or different geometries of a single material. In MEMS, both principles are used. The first one is illustrated in Figure 5.1-13.

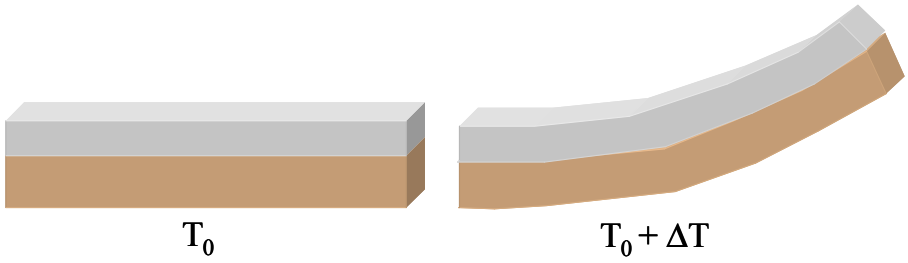

Figure 5.1-13: Principle of the bilamina thermal actuator

When the bilamina is heated, if materials have a different coefficient of thermal expansion (CTE) then the bilamina bends. The vertical deflection resulting from this bending is greater than the elongation of a single lamina.

The second principle is based on the difference of geometry of a material. A typical bimorphic thermal actuator is illustrated in Figure 5.1-14. When biased, the difference of geometry leads to a difference in current density and thus to a difference in temperature. In the thin arm, the current density is greater than in the large one. So the thin arm is more heated and dilates more than the large arm. The actuator bends to the left handside.

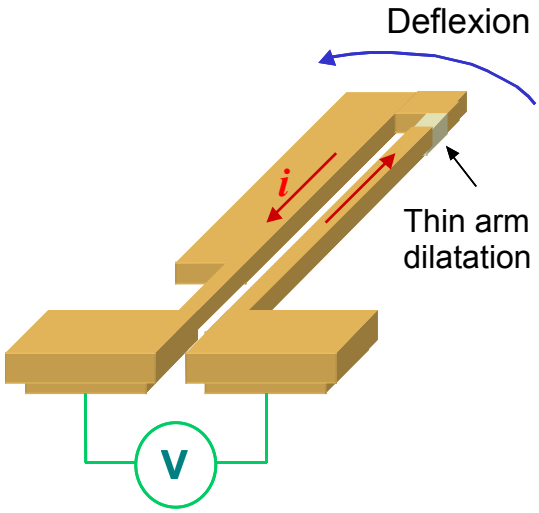

Figure 5.1-14: Principle of the bimorphic electrothermal actuator

From a MEMS point of view, the process is simpler than other actuator families. They also exhibit higher restoring forces than contact forces. But unlike electrostatic actuators, they provide low contact forces at the end of the displacement. Moreover, it has been shown that contact forces are in the range of a few micro-newtons which is too low for switching applications.
The driving powers are relatively low, typically few micro-Watts and the actuation voltage fits telecommunication requirements (5-6V for polysilicon actuator).

The benefice of a low actuation voltage has been used recently as a start actuator in an electrostatic RF switch. The switch is actuated with a bilamic electrothermal actuator and is held in the "on" position by the electrostatic actuator. The combination of both actuators allows a very low actuation voltage (<3V) with a reasonable switching speed (<300µs).

5.1.2.6 Piezoelectric actuators

Used for accurate displacement or precision measurements, the piezo electric actuator is based on electrical and mechanical properties of some crystals. When an electrical signal is applied between two sides of a piezo-electric material, this one is mechanically deformed. In a same way, if the material is deformed mechanically, an electrical potential is created. Figure 5.1-15 illustrates a typical piezoelectric actuator.

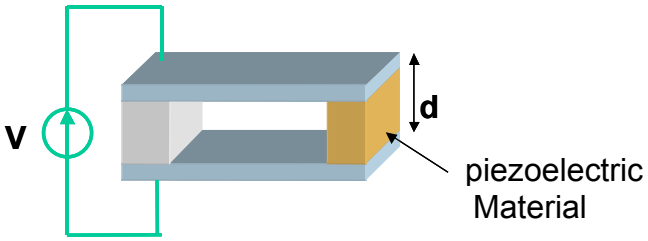

Figure 5.1-15: Principle of the piezoelectric actuator

The mechanical deformation provided by a piezo-electric material is lower than 1µm. In consequence, this actuator cannot be used in MEMS switches.

5.1.3 True time delay lines

5.1.3.1 Introduction

This document examines True-Time Delay Lines (TTDL) electronically reconfigurable by means of Micro-ElectroMechanical Systems (MEMS) and aimed at phased arrays applications.

A TTDL is a device which produces the delay of an RF-signal between its input and its output independently of the signal frequency. From this point of view, a simple transmission line is a TTDL, but it does not allow controlling the delay. It is noticeable that the term 'true time' arise form the fact that such a device produces a time delay due the propagation of the electromagnetic wave through a path of finite length, hence a 'true' delay from a causality point of view. In terms of phase, a TTDL is a phase shifter with linear phase variation with frequency. This result from the fact for a constant phase velocity, the wave number is proportional to the frequency. The next graphs illustrate this matter:

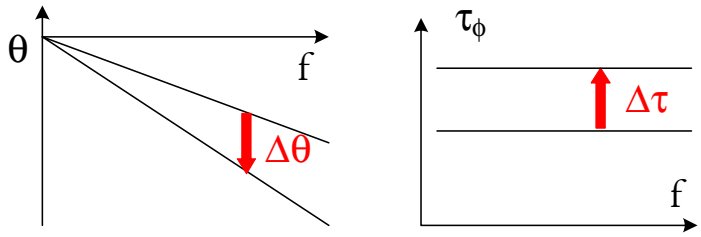

Figure 5.1-16: Phase shift and delay

Note: A clear naming of the phase shifters with regard to their phase to frequency behaviour is necessary for clear discussions involving such devices. Therefore, we will use the following naming here:

- phase shifter : Any device producing a phase shift
- constant-phase shifte' : phase shifter whose phase shift is constant with frequency
- TTDL : True-Time Delay Line: phase shifter whose phase shift is proportional to the frequency

5.1.3.2 MEMS-based V-TTDL technology : description

There is a significant amount of publications dealing with MEMS-based delay lines topologies. In this section, we extract and describe the main features of the most popular configurations, so as a non-exhaustive number of references for each topology:

- Switched type.
- Reflection type.
- Distributed type.

Finally, a table summarizing the performances of some TTDL of each type is presented.

5.1.3.2.1 Switched type

The *switched type* is based on different length transmission lines which are switched to produce different delays. It has an excellent performance over a large bandwidth but the size of this device is its major drawback. Typically this is overcome using folded lines with meander or fractal shapes such that the effective length is reduce although the performance is deteriorated. The bandwidth is not limited by the dispersion in the line but rather by the quality of the switching devices. Results for this type of TTDL are to be found in [1-3]. A performing device using microstrip technology and based on the switched lines principle is presented in [1], and is depicted in the next figure:

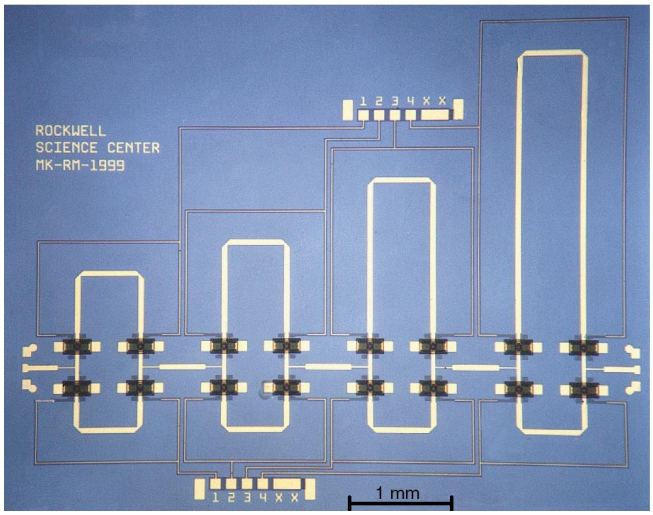

Figure 5.1-17: Switched TTDL

5.1.3.2.2 Reflection type

For applications where space saving is a major issue, a sensible choice is the *reflection type* which reduces the length of the lines by two by taking advantage of the reflected wave. From this point of view, the *reflection type* is rather an evolution of the *switched type* than a completely new topology. The limitation on this device is also fixed by the switches but even more significantly the 3-Db coupler needed at the input which will limit the bandwidth performance of the device. The problem is usually addressed using a Lange coupler which guarantees an acceptable bandwidth. However, this type of design is still not suitable if wide bandwidth is a strong specification. A good example of design of a 4-bit reflection type delay line is found in [4].

5.1.3.2.3 Distributed type

The aforementioned types both use the “space” to produce a change in the “time“ while the “velocity” is kept constant. In contrast, the *distributed type* delay lines take advantage of the possibility to control the wave velocity, while keeping the length of the propagation path constant. This approach is obviously the most performing in terms of space but also provides a very wide bandwidth. In this type, both the “velocity” and “space” parameters can be modified in order to produce different “time” delays. Regarding these advantages, the *distributed type* delay lines have been the most widely studied and many results can be found in the literature [5-15], when compared to the *switched* and *reflection types*. On average, the *distributed type* is most performing in the highest frequencies (above 20GHz), when compared with the other types.

The *distributed type* delay line takes advantage of the fact that the wave velocity depends on the line distributed capacitance value. Consequently, such a design is a transmission line whose line distributed capacitance can be controlled. Usually, the capacitance control is made by means of MEMS variable capacitor connected periodically in parallel with the line. Most designs have been done on CPW lines [5-13], but it is also possible to realize microstrip distributed TTDL [14]:

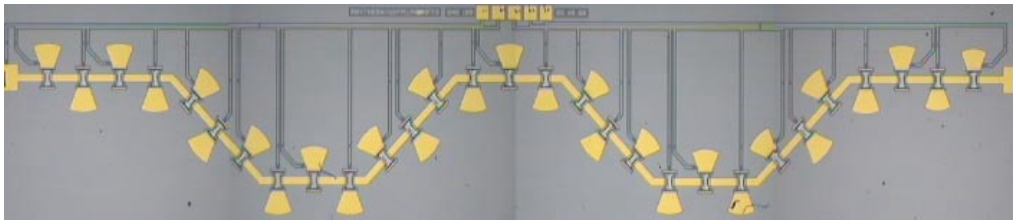

Figure 5.1-18: Distributed TTDL

Another kind of distributed delay line is presented in [15]. In this case, the variation of the distributed capacitance is achieved by controlling the strip to group plane distance. When compared to the aforementioned distributed types, this realization reveals to be more complex in terms of design, fabrication complexity, and requires hundreds of volts for the actuation.

5.1.3.3 Performance table

Reference	Type	Bw	$\|S_{21}\|$	$\|S_{11}\|$	$\Delta\angle S_{21}$	MEMS Switch		Comments
						Type	Pull-down voltage	
U.Michigan&Rockwell Tan et al. (2002) [2]	Microstrip on GaAs 2 bit **Switched line type** (12 mm^2)	8□12GHz	< –1Db –0.55Db (av,)	< –17Db	Linear up to 18GHz	Serial Capacitive	□	Very Compact 12mm^2
Rockwell Kim et al. (2001) [1]	Microstrip on GaAs 4 bit **Switched line type** (6 × 5 mm^2)	DC□ 40GHz	–2.5 to –5Db	<–15Db	Linear up to 40GHz	Metal-to-metal serial	~70V	Exc. performance as TTD
Raytheon Pillans et al. (1999) [3]	Microstrip on HR-Si 4 bit Resonant **Switched line type** (50 mm^2)	35GHz (5%)	–3Db to –2Db	<–12Db	<13° error at the smallest state	Shunt Capacitive	~45V	
Raytheon Malczewski et al. (1999) [4]	Microstrip on HR-Si 2 bit **Reflection type** (50 mm^2)	7□11GHz	–1 to –25Db –1.8Db (av.)	<–11Db	□	Shunt Capacitive	35□ 40V	
Seoul National Univ. Kim et al. (2002)	CPW on quartz 2 bit **Reflection type** (1.5 × 2.1 mm^2)	50□70GHz	–2.5 to –5.5Db –4.5Db(av.)	<–12Db	<6.3° error at 60GHz	Metal-to-metal serial	30□40V	
U.California Borgioli et al. (Jan.2000) [5]	CPW on glass 1 bit **Distributed type** (□ mm^2)	0 □35GHz	<–1.5Db	<–11Db	180° at 25GHz 270° at 35GHz	Shunt Capacitive	~75V	11 shunt MEMs. Use of serial MIM to reduce mismatches
U.California Liu et al. (Oct.2000) [13]	CPW on glass 3 bit **Distributed type** (□ mm^2)	10□26GHz	<–2.6Db –1.7Db(av.)	<-8Db <25GHz	<8.5° error ∀ states	Shunt Capacitive	~60V	Tapered line under bridge instead of serial MIM to reduce mismatches

						MEMS Switch		
U.Michigan Barker et al. (1998) [7]	CPW on quartz analog **Distributed type** (□ mm^2)	0□60GHz	<–4Db	<–10B	1.8Db /84° at 40GHz	Shunt Capacitive	10-23V	*38 bridges*
U.Michigan Hayden et al. (Dec.2000) [12]	CPW on quartz 2 bit **Distributed type** (□ mm^2)	1□20GHz	<–25Db but <–5Db for <10GHz	<–11Db	TTD 1-10GHz PS 180°/300° at 10GHz	Shunt Capacitive	30-50V (13V alone)	High influence of MIM in the I.L. and phase shift for >10GHz. *24 bridges*
U.Michigan Hayden et al. (Jan. 2003) [10]	CPW on quartz 2 bit **Distributed type** (8.4 × 2.1 mm^2)	1□40GHz	<–2.1Db –1.5Db (av.)	<–11.5Db	PS 0 to 270° at 37.7GHz	Shunt Capacitive	20V	Improvement of the capacitors using MAM with Q>150. High R. meander biasing *21 bridges*
U.Michigan Hayden et al. (May 2001) [14]	Microstrip on Si 4 bit **Distributed type** (□ mm^2)	DC-18GHz	<–4.0Db –3.0Db (av.)	<–9Db	360° at 18GHz	Shunt Capacitive	40-46V	Radial stub capacitance in series with bridge capacitance.
Seoul National Univ. Kim et al. (2002)	CPW on quartz 2 bit **Distributed type** (6.3 ×1.5 mm^2)	40-70GHz	–3.0Db (av.)	<-10Db	15.2° error at 270°	Shunt Capacitive	15-20V	MAM and RF choke biasing which bypass Cs. *24 bridges*
U. Manitoba Shafai and al. (2004) [15]	Microstrip, GP reconf. Distributed type (5 x 50mm^2)	5-32 GHz	-1.3Db	-8Db	32° at 15 GHz	GP reconf.	'hundreds of V'	Very high actuation voltage

5.1.3.4 MEMS-based V-TTDL technology : key iss

Controllable TTDL have been widely used in the last decades. Until recent years, the control capabilities of such devices had been based on controllable ferrite material, semi-conductors p-i-n diodes or FET transistors. However, the recent development of MEMS technology allowed challenging radically the performances of the aforementioned established delay lines. Instead of offering new topologies for the design, MEMS have mainly allowed increasing dramatically the performances of existing topologies. In order to illustrate those capabilities, here is an overview of demonstrated advantages offered by MEMS-based TTDL:

- Lower insertion loss
- Increased bandwidth
- Low drive power (no DC power consumption outside switching)
- Physical size and weight
- Monolithic integration of the whole feed network

Nevertheless, some of causes of concern for MEMS-based delay lines are:

- Limited allowable transmitted power
- Reliability
- Process cost and compatibility

More details about the limitation of MEMS-based TTDL is given below.

5.1.3.5 Limitations of MEMS-based V-TTDL technology

5.1.3.5.1 Power handling

In radar applications, it is common to transmit several watts of power, although for short duration (pulse excitation). However, this is a major cause of concern for the power handling of delay line. Indeed, any type of MEMS-based delay line is subject to a limited power handling.

In concrete terms, the power handling of a delay line is determined by the limit RF power that can be transmitted without altering the behaviour of the device to a certain extent. Practically, the problem is that for sufficiently high RF power, the RF signal induces a non-negligible effect on the Electromechanical behavior of the device. This results in a non-linear TTDL but even to a complete failure of the device for a certain transmitted power. In detail, the power handling limit depends on:

- The type of delay line (switched or distributed)
- The type of switch or variable capacitor used (analogous, digital) and their geometry
- The mode of operation of the line (delay switching only when the RF power is off or also 'hot' switching)

Consequently, it is hard to compare the power handling of different lines but this must be a key design preoccupation in the case of high power application. An example of power handling analysis in given in [16], so as a switch designed for enhanced power capability.

5.1.3.5.2 Actuation voltage

Like several other MEMS devices, delay lines often need relatively high control voltages, which can be superior to 30 V. This especially holds true for the *distributed type* with digital capacitors and for *switched and reflection types*. This practically limits their use in devices such as mobile handset. Indeed, the trend for such device is to lower the DC operating frequency as much as possible, and is in practice much lower than 10 V.

5.1.3.5.3 Mismatch

The use of digital capacitor in *distributed* delay lines allowed increasing significantly the stability (RF behavior stability with regard to DC noise), but also the delay/losses ratio, which can be considered as a major performance coefficient of a TTDL.

However, this also led to an increased variation of the equivalent charcteristic impedance of the TTDL between 'off' and 'on' states, hence larger a mismatch. In corporate feed (see Figure 5.1-1), the phase shifter in each branch must actually be constituted of a cascade of sub-phase shifters in order that several angles can be scanned (with a single digital V-TTDL in each branch, the array would only be able to scan at $-\alpha$,0 and $+\alpha$). Consequently, the mismatch can be a very limited factor for the use of the *distributed type* if the scan angle resolution is high.

In the *switched* and *reflection types*, the mismatch will also increase with the number of angle scanned, as the signal will 'cross' more switches, whose performance is the major limitation for these types of V-TTDL.

5.1.3.5.4 Reliability

After the main advantages of MEMS technology over existing ones had been demonstrated, a great attention was paid to the reliability of such devices. Indeed, the reliability is still a cause for concern for the insertion of MEMS RF devices in operational systems.

There are very different causes for potential failure in MEMS devices which have to be addressed separately. Here, we will just mention some of these issues and give relevant reference. Some general information is to be found in [17]. Long-term RF power handling has been treated in [18] whereas mechanical constraints (shocks and vibrations) are studied in [19] and [20]. Finally, an interesting paper addressing the implications of MEMS failures on the performance of a reference device (2-Bit phase shifter), with probabilistic methods, is found in [21].

5.1.3.6 Needs for new features and capabilities

5.1.3.6.1 Performances

Summarizing section, two major fields for improvements are to increase the following ratios in V-TTDL:

- Power handling / actuation voltage
- Delay / mismatch

So as the:

- Reliability

5.1.3.6.2 Packaging

Like many other MEMS devices, controllable delay lines must be packaged for practical use. However, almost all published results concern unpackaged lines which are mostly measured directly on-wafer. A reference of a package delay line is given in [22]. Consequently, there is a need to characterize the packaging effect on the line performances. On the other hand, the packaging is an important issue with regard to the cost of MEMS phase shifter since large areas are to be enclosed, hence greater the packaging price when compared with MEMS single switches.

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5.2 POSSIBLE ANTENNA APPLICATIONS

5.2.1 State of the art

In 1999, DARPA (Defense Advanced Research Projects Agency) launched the RECAP program (Reconfigurable antenna aperture). The application is for military ground communications systems, that will need in the future reconfigurable capabilities. RF MEMS has been foreseen as the key element to develop such low cost systems.

The stated goal of the program was to create a phased-array that could reconfigure to tune its operating frequency over a 10:1 bandwidth while maintaining the ability to electrically scan to large off-broadside angles. The program included multiple efforts to develop phased-array antennas that utilize MEMS switches to change the array frequency, polarization, or directivity patterns. RECAP produced several reconfigurable aperture concepts and innovations such as a reconfigurable metamaterial antenna with MEMS **[COREY01]**. More than a dozen contractors developed innovative applications of MEMS, but all of these suffered due to the main technological immaturity of RF MEMS, which are particularly :

- Hermetic packaging issues
- Reliability
- Power handling capabilities (in hot switching applications) : Still limited to 100 Mw

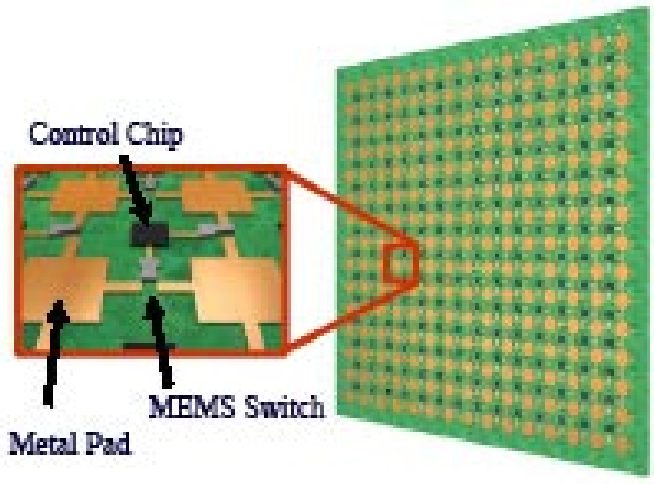


Figure 5.2-1: Example of reconfigurable metamaterial antenna with MEMS []

For low cost phased array radar, previous architecture using RF MEMS is now being challenged by new RF MEMS free architecture using fully integrated, on chip Tx/Rx module for an acceptable cost (Northrup, Raytheon,…). In the same time, a research program (RF MEMS Improvement Program) was launched by DARPA.

Europe also funded a lot of research projects on Antenna with MEMS. These projects confirmed the interest of MEMS for achieving at moderate cost antenna reconfigurability, but the applications required drastic work on the MEMS technology itself.

From our knowledge, it can be said that compared with what's being achieved within Europe, US laboratories (Raytheon, Lincoln labs, Georgia Tech, Air Force research laboratories, Hughes research labs, University of Michigan, NASA,…) are 3 to 4 years ahead performance wise.

The objective of this chapter is to identify the new functionnalities brought by RF MEMS for antennas, and the related limitations of the design.

5.2.2 Reflectarrays

A reflectarray is a planar array illuminated by a primary feed. This array is composed of planar elements reflecting the incident wave with a phase shift controlled through either by diodes or by miniature switches (MEMS). It is consequently possible to steer and form a beam by controlling the phase shift of the elements.

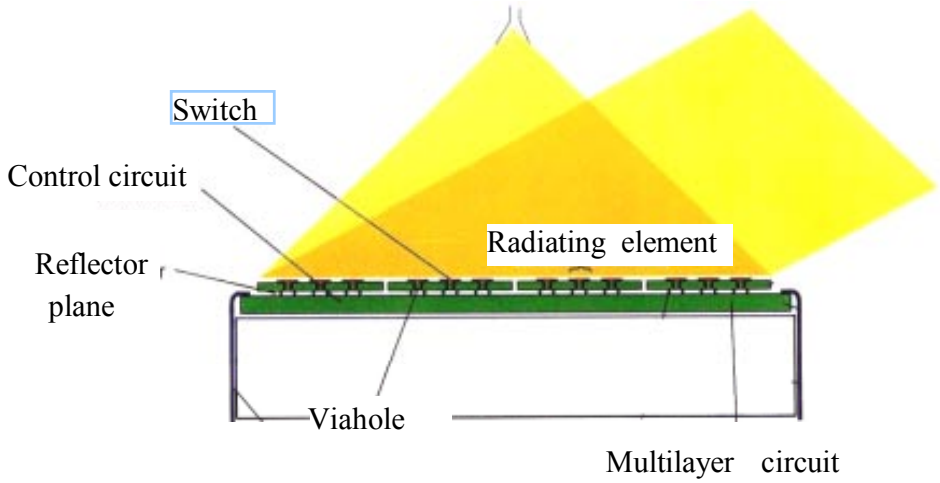


Figure 5.2-2: Principle of the reflectarray

A reflectarray antenna is an attractive solution for reconfigurable antennas, for it has both advantages of arrays – beam shaping with fixed antenna – and reflectors – high efficiency single feed.

The reflectarray is also very attractive for low profile antennas (passive or active). For space application, particularly, it can be easier to stow in the launcher.

ALCATEL Space has a strong heritage on reflectarrays, and conducted different studies in order to build competitive products, which are developed here-under :

5.2.2.1 Reflectarray in Circular polarisation

The French Research project ARRESAT, headed by ALCATEL SPACE and in connection with industrial partners, academic partners and SMEs, was the first study on reconfigurable reflectarrays with MEMS **[LEGAR04a].** The main objectives were to demonstrate the feasibility of low loss active phase shift elements with MEMS control and to demonstrate the high radiating performances of a reflectarray.

The following specifications were selected for the phase shift element :

- Ka band ;
- Circular polarisation ;
- Large bandwidth;
- Low loss and integrates MEMS switches to monitor its phase ;
- Compact ,

The aimed application was for the satellite antennas of a telecommunications system using Low Earth Orbit satelittes.

Innovating phase shift elements, providing phase control thanks to Micro Electro Mechanical Switches (MEMS) were designed and built.

Special attention was given within the design process, to include the MEMS characteristics, expressed as a C_{down}/C_{up} ratio, where C_{down} refers to the capacity with the membrane down, and C_{up} to the capacity with the membrane up ;

These phase shift elements operated in circular polarisation over a very large band (17.8-19.3 GHz), with a 2.5 bits resolution.

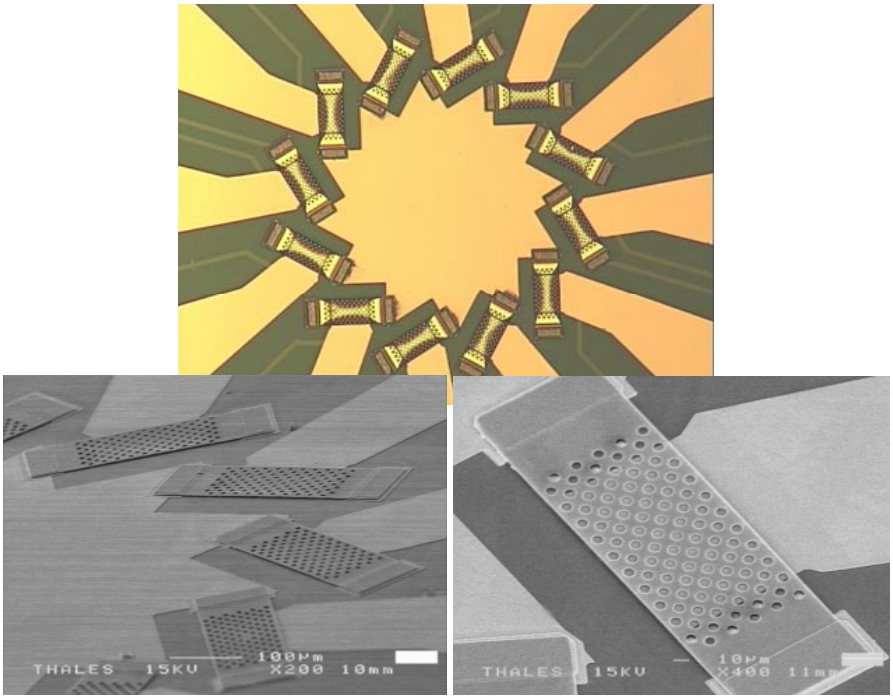
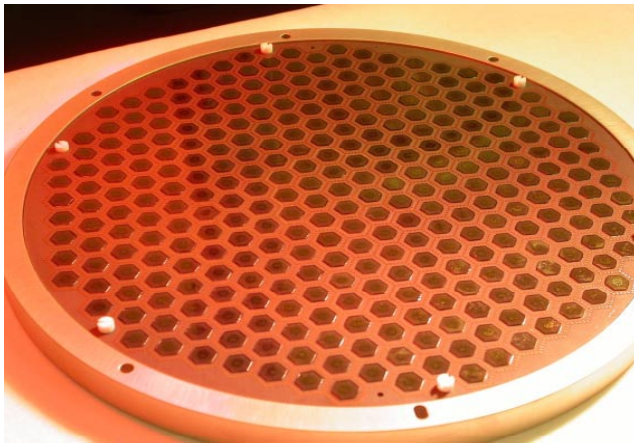


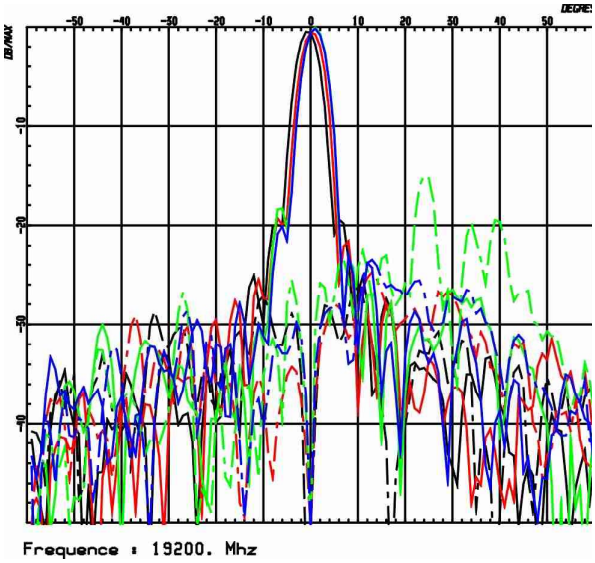
Figure 5.2-3: Macro-component-MEMS switches integrated onto the phase shift element

A reflectarray antenna was designed, fabricated, and measured and demonstrated excellent results over a wide band : Radiation efficiency > 60% over this band, and very low cross polarisation (<-35 Db) ;



b) Array of phase shifting elements

a) Measurement set-up



c) Radiation pattern measured at 19,2 GHz

Figure 5.2-4: Active Reflectarray with MEMS control

5.2.2.2 Reflectarray in linear polarisation

Phase shift elements in linear polarisation were designed in Ku and Ka bands with stringent specifications : losses < 0.5 Db, 3 bits phase quantization, Bandwidth greater than 5%,…

The phase shift element consists of a cavity backed patch element with two slots loaded with MEMS. The MEMS control the electrical length of the slots which monitors the phase shift applied to an impinging plane wave.

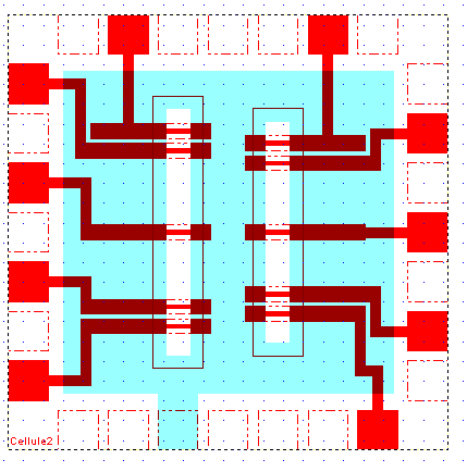


Figure 5.2-5: Phase shift element. Slotted patch.
MEMS control the length of the slot.

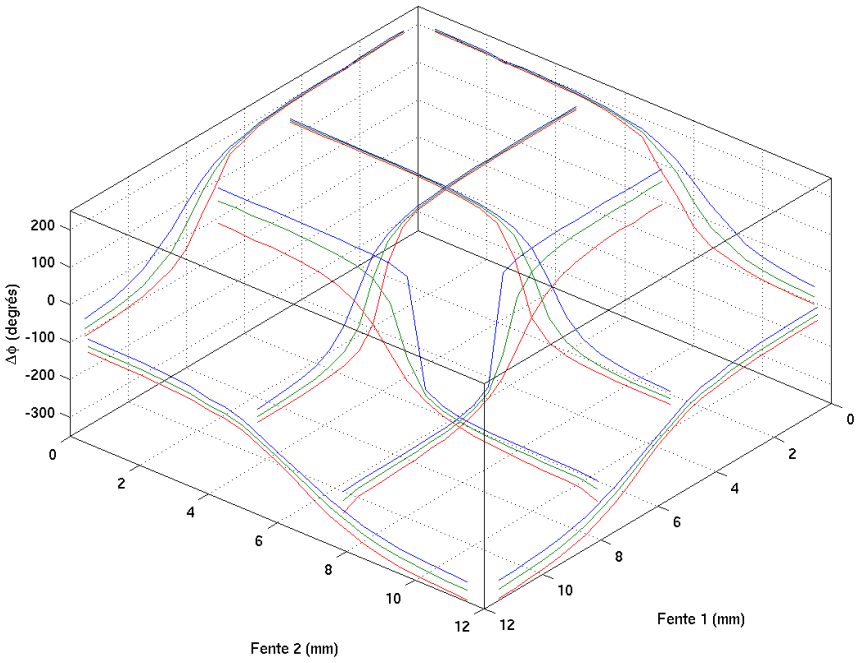


Figure 5.2-6: Phase shift as a function of the slots lengths.
Blue, and red curves correpsonds to the edge frequencies (more than 7% bandwidth), Green curve to the central frequency.

5.2.2.3 Issues

The main issues for the reflectarrays are the following :

- Lowest losses as possible : Resonant structures such as FSS, reflectarray elements, are extremely sensitive to the tg δ of the material. Low losses material shall therefore be selected, such as Alumina, or very thin silicon (micromachined on the rear face). Slot elements are also good candidates for such a requirement.
- Collective mounting solutions or Monolithic approach : For achieving low cost, a global and repetitive process shall be defined, which includes packaging, MEMS substrate, RF layers, DC board.

5.2.3 Radiating element with multifrequency operation

5.2.3.1 General comments on reconfigurable antennas

The comments given below are also valid for polarization and pattern reconfigurable antennas.

The various examples of reconfigurable radiating elements can be classified into three categories:

- Antennas where MEMS devices (switches or actuators) are integrated inside the radiating elements themselves,
- Antennas where MEMS devices (mainly switches) are connected to radiating elements through shorts transmission line sections,
- Antennas where MEMS devices (mainly switches) are integrated in the feeding network of the arrays or sub-arrays.

The first category yields more compact structures but requires the insertion of the component in the vicinity of a current maximum to obtain a strong effect on the antenna resonance. The stronger the effect, the larger the tuning ability but also the larger the coupling between the component and the antenna field. The component influence cannot be easily handled because of the non-ideal behaviour of the components. This influence results in:

- a drop of the antenna efficiency, especially in the ON state of the components because of non-zero resistances in the electrical model,
- a shift of the predicted resonant frequencies because of added inductors/capacitors in the electrical model.

As a result, rigorous designs require global electromagnetic models including some refinements in the component modelling (sophisticated electrical model, 2D or 3D distributions of the component). At this stage, one has to consider that the equivalent circuit for MEMS or solid-state components are generally obtained with microstrip or CPW ports and cannot necessarily be transferred in an antenna environment.

Moreover, biasing circuits should be designed to minimize the influence of DC lines on the electromagnetic characteristics of the antenna. Finally, MEMS packaging techniques have to be taken into account when designing the antenna.

In the second category, the switchable component is located outside the antenna and loads the antenna through transmission line sections. This solution is less compact but yields lower losses in the tuning circuit and reduced parasitic radiation. A simple circuit model of the component is sufficient to evaluate its influence accurately.

In the third category, MEMS switches are directly integrated in the feeding network of the antenna. Radiating elements and switches can be fabricated on opposite faces of the same substrate, or on separate substrates. This could lead to some technological challenges, such as double-face processes or wafer bonding techniques. As for the second category, this approach allows to use conventional electrical models of switches.

Examples corresponding to these three categories are given in the following sub-sections.

Now, it is clear that most concepts developed with pin diodes or FET can be applied with MEMS. The MEMS can be used in its packaged version or included in the fabrication of the antenna. The main advantage of MEMS compared to solid-state components relies on lower RF losses and better linearity (depending on the actuation mode, DC consumption is also usually smaller than for electronic components). Therefore, one can expect improved efficiency performance for MEMS-based reconfigurable antennas.

5.2.3.2 General comments on frequency-reconfigurable antennas

A radiating element with multifrequency operation is a reconfigurable antenna whose impedance features can be modified by tuning the electrical properties of a solid state component (varactors, PIN diodes, transistors,…) integrated inside the antenna volume. This definition can be extended to micromechanical components (MEMs) and to biased silicon substrates **[FUSCO]**. In this section, tunable/diversity properties are more specifically related to the resonant frequency of a planar antenna. The continuous or switched variation of the resonant frequency must be obtained with good return loss and efficiency performance in the tuning range.

The frequency diversity can either be used in multistandard/multiband terminals (for instance Bluetooth+Wi-Fi 802.11a/b/g at 2.4/5.4/5.8 GHz) or for a fine resonance adjustment when de-tuning occurs. In RFID tags or mobile phones, de-tuning results from the hand or body influence. This adjustment could ultimately be associated with some feedback loop to realize self-reacting antennas. Examples of key functions required to obtain self-reacting features are given below:

- Control of antenna band centre and bandwidth for channel switching and filtering,
- Diversity arrangements to allow MIMO (Multiple Input, Multiple Output) operation or diversity gain,
- Integration of a variable phase and amplitude response in the antenna to add some channel equalisation capability.

The development of reconfigurable antennas only makes sense if the module cost and connection complexity are reduced compared to configurations that require a separate antenna. As a strong effort has been devoted to multiband passive antennas during the last decade, one has to justify the advantages of tunable antennas counterbalancing their added complexity (bias circuit, soldering points, ..) and cost:

- Multiband passive antennas often present narrow bandwidths for one or several bands. Therefore, these antennas can be sensitive to fabrication tolerances or electromagnetic disturbances (human body). This sensitivity can be fight if tuning properties are added,
- Multiband antennas necessarily receive unwanted signals and/or added noise from the other bands when a given band/standard is selected. Therefore, filtering circuits are necessary in the front-end whereas intrinsic filtering is performed in tunable antennas,

- Compactness: multiband passive antenna can hardly be small, efficient and have good radiation properties (polarization, pattern) in all bands simultaneously. In tunable antennas, as diversity is basically obtained by electronically scaling an initial antenna, the main features are kept in the tuning range. The antenna size is fixed by the lowest operating frequency.

5.2.3.3 Principle of operation

In a first approach, the electrical component can be seen as an ideal switch or an ideal capacitor. In order to obtain an effective impact on the resonance, this component should be located in a strategic position inside the antenna, i.e., a position where its parasitic influence on the electromagnetic field is strong. Another solution consists in loading the antenna by an external line and to insert a switchable component inside the line. The main idea is to create a continuous (capacitor) or discrete (switch) alteration of the resonant lengths, either by modifying the current paths, the propagation constants or by loading the antenna.

5.2.3.4 State of art

Two interesting solutions proposed by the Helsinki University of Technology (HUT) are presented along with a typical concept developed at the University of Michigan (UoM). The other concepts have been developed by IETR and UMLV.

5.2.3.4.1 Frequency-tunable antenna for mobile phone using FET and pin diode switches

Figure 5.2-7 shows a frequency-tunable internal antenna for mobile phones proposed by HUT **[KIVE02]**. A tuning circuit was added to a dual-band antenna element for the European GSM bands (880-960 MHz, 1710-1880 MHz) to cover also the US cellular system band (824-894 MHz) with the same antenna. The tuning circuit consisted of low-loss transmission line sections and an SPDT FET switch, which has suitable characteristics for use in real mobile phones. The antenna was positioned on a metallized PCB having dimensions 110 mm × 40 mm, thus representing the PCB of a typical mobile phone.

The basic idea is to connect the first tuning line having length *l*1 in turn to the second tuning line having length either *l*2,1 or *l*2,2 and thereby change the reactance loading the antenna. The switch was not directly connected to the antenna but separated from it by a section of transmission line. This allows low power loss in the switch, as the position of the switch is close to a current minimum.

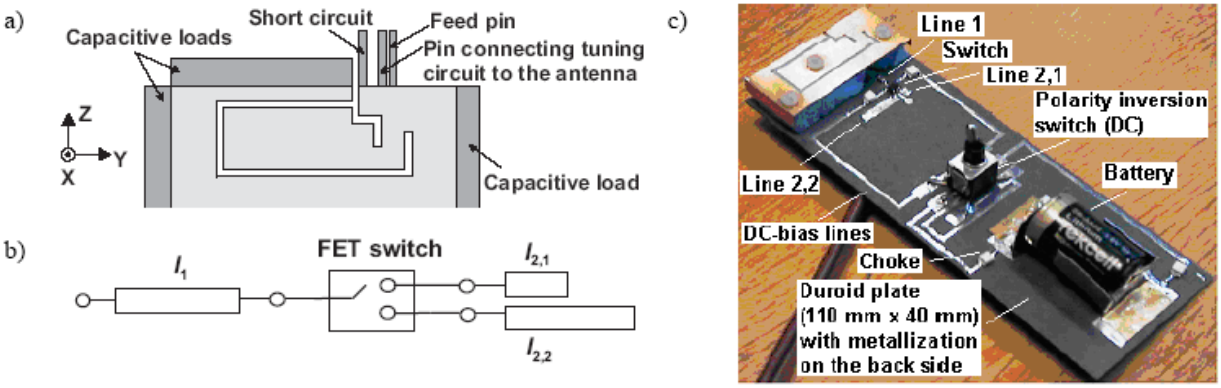


Figure 5.2-7: Frequency-tunable internal antenna for mobile phones, a) Antenna element (to scale), darkened parts are bent down, b) Structure of the tuning circuit, c) Photograph of the prototype. (HUT)

The narrow impedance bandwidth of small antennas for personal mobile communications can be alleviated with electrical frequency tuning, which increases the effective bandwidth and can enable the use of a single antenna element in several radio systems without increasing its size. To date, the main emphasis has been on the achievable tuning range while power loss caused by the tuning circuitry is a major problem of frequency-tunable antennas. The minimization of power loss and caused by the tuning circuit have received special attention from HUT **[OLLli02]** in a **frequency-tunable shorted patch antenna** (Figure 5.2-8). The antenna is based on a shorted patch with Q_0 = 20. A PIN-diode was used as the switch.

The prototype is capable of switching between the transmitting (TX, 880…915 MHz) and receiving (RX, 925…960 MHz) band of an E-GSM900 mobile station. The goal was to minimise the power loss in the tuning circuit and to obtain approximately equal and high radiation efficiencies at both bands. With the help of a circuit model (Figure 5.2-9), an optimal configuration for the tuning circuit can be determined. Both in simulations and in measurements, the necessary frequency tuning was obtained at the expense of roughly 3 % reduction in efficiency compared to the antenna without the tuning circuit.

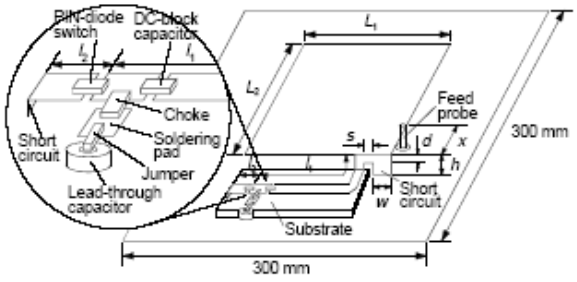


Figure 5.2-8: Geometry of frequency-tunable shorted patch antenna

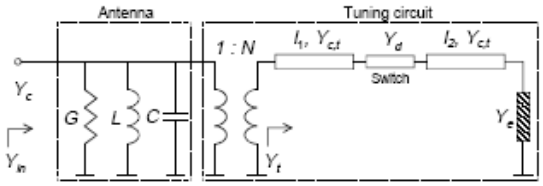


Figure 5.2-9 : Circuit model for frequency-tunable resonant antenna with series switch. Load admittance Ye represents the open (Ye = 0) or shorted (Ye = ∞) end of line 2

5.2.3.4.2 MEMS-based reconfigurable patch antennas on silicon

To illustrate the interest for MEMS-based reconfigurable antennas, a patch antenna with two independent MEMS actuators is shown in Figure 5.2-10 **[SIMO01]**. The antenna is fabricated on high resistivity silicon wafer (ε_r = 11.7, h = 400µm) with spin-on-glass (SOG) (ε_{r1}= 3.1, h1 =1.5µm) as the dielectric support layer. Each actuator consists of a moveable metal overpass suspended over a metal stub and supported at either ends by metalized vias which are electrically connected to the patch antenna. The metal strip of length L and width W attached to the metal stub behaves as a parallel plate capacitor. The patch antenna operates at its nominal frequency as determined by the dimension b when the actuator is in the OFF state. The actuator is in the ON state when the overpass is pulled down by the electrostatic force due to the bias, and the capacitance of the metal strip appears in shunt with the input impedance of the patch antenna. This capacitance tunes the patch to a lower operating frequency.

The measured return loss for the two states of the actuators is shown in Figure 5.2-11. When both the actuators are in the OFF state, the patch resonates at its nominal operating frequency (f0) of about 25.0 GHz. When both actuators are in the ON state, the Fon is 24.6 GHz. The 400 MHz shift is about 1.6 percent of f0.

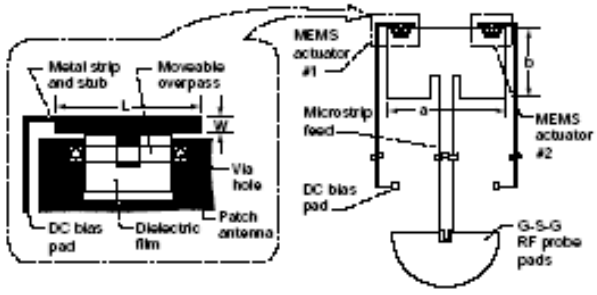


Figure 5.2-10: Frequency reconfigurable patch antenna element with two independent MEMS actuators, L = 580 µm, W = 50 µm, a = 2600 µm, b = 1500 µm

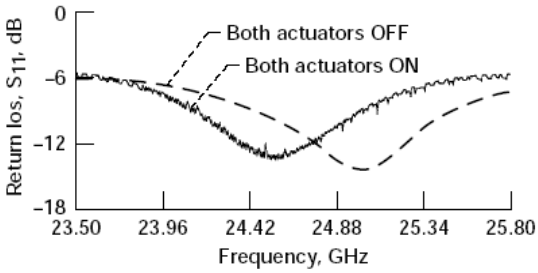


Figure 5.2-11: Measured return loss demonstrating frequency reconfigurability with integrated MEMS actuators while maintaining good impedance match.

5.2.3.4.3 Agile CPW-patch antenna on silicon *IETR*

A wideband frequency agile patch antenna has been proposed in **[LEGAR03]**. Compared to previous designs, this solution enables to obtain a quasi-constant gain over the whole frequency band, with the same feeding network (Figure 5.2-12).

For validation purposes, a patch antenna was fabricated on a 400 µm high-resistivity Silicon (ε_r=11.8 ; tanδ=2.10^{-3}) substrate with two BCB layers. The appropriate combination of (i) parasitic elements, (ii) slits etched in the patch and (iii) MEMS switches allows a discrete frequency shift over a 2:1 frequency band.

An alternative and simpler solution consists is using only MEMS switches bridged onto the patch and above the parasitic element. A schematic diagram of the antenna configuration is given in Figure 5.2-13 and Figure 5.2-14. In that case, the resonance frequency of the antenna is tuned between 37 GHz and 43 GHz.

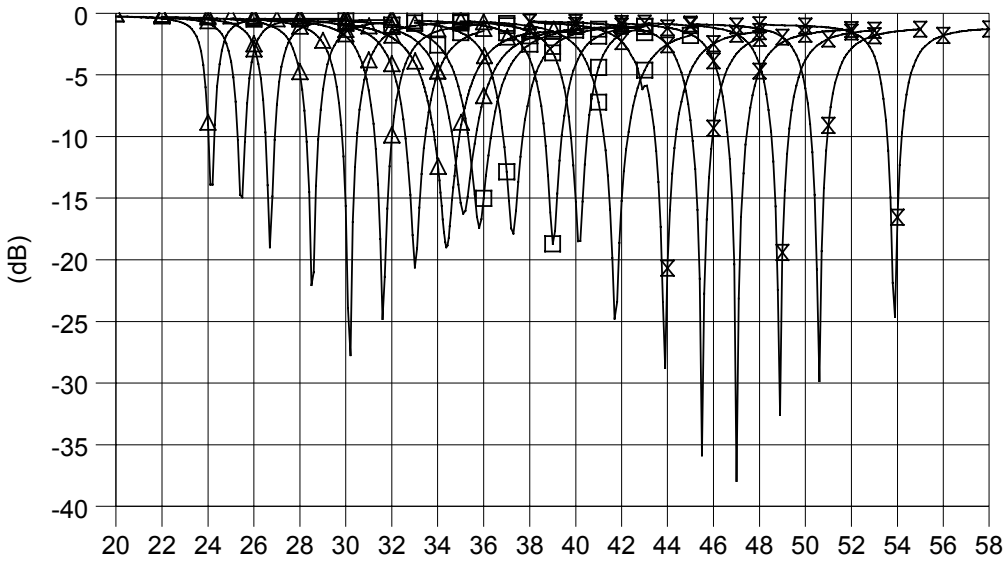


Figure 5.2-12: Measured return loss of the frequency-agile antenna

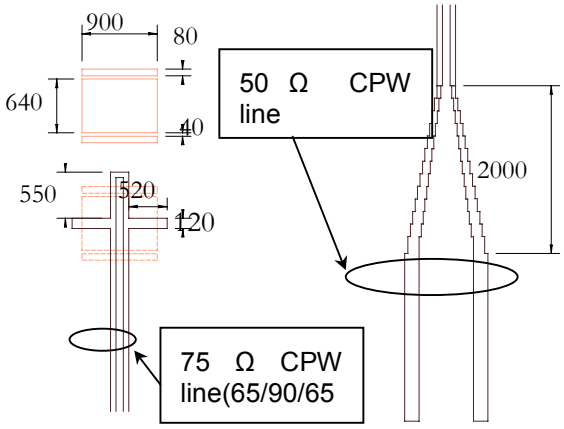


Figure 5.2-13: Frequency agile antenna. (dimensions are in µm)

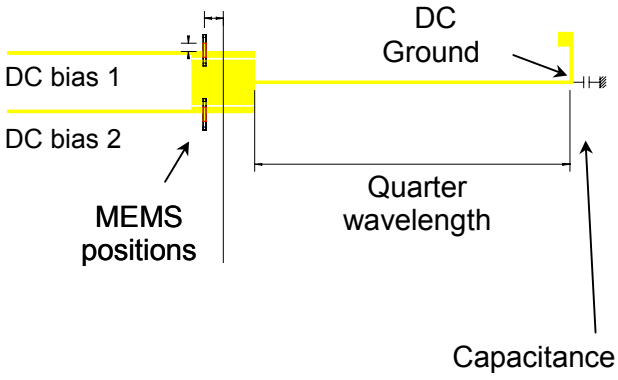
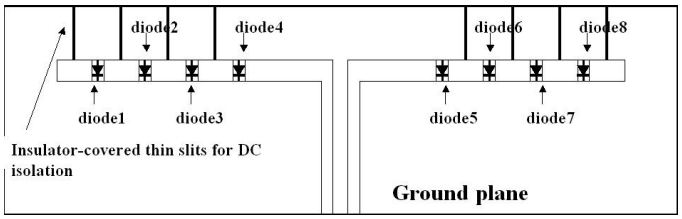


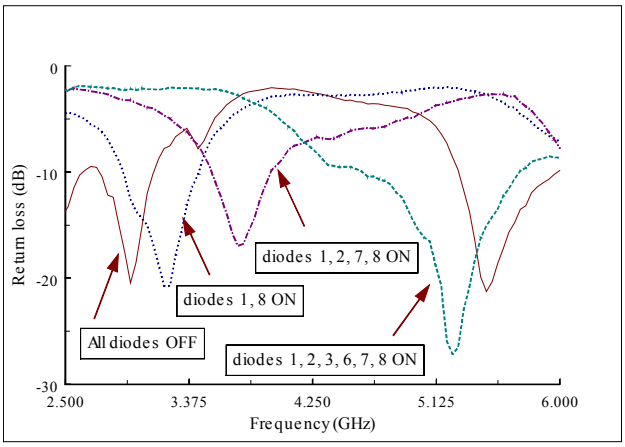
Figure 5.2-14: Top view of a dual-frequencies tunable antenna.

5.2.3.4.4 Reconfigurable antennas based on slot-antennas and aperture-coupled antennas

As mentioned previously, one basic principle of reconfigurable antennas consists in the electronic control of the resonant length of the antenna. This length can be effectively added or subtracted to the physical length by inserting a switchable short/open inside the antenna. A simple example of a switchable CPW-fed slot antenna including eight *pin* diodes **[LAHE01]** is given in Figure 5.2-15. Another example is the dual-frequency operation of a CPW-fed patch antenna **[LUXE00, LAHE02]** where the pin diodes are inserted in the coupling slot (Figure 5.2-16).



(a)



(b)

Figure 5.2-15: Switchable CPW-fed slot-antenna based on eight pin diodes. (a) Switchable CPW-fed slot antenna including eight *pin* diodes and a biasing circuit , (b) Return loss measurements for different states of the diodes

The slot-antenna is built on a Duroid substrate (εr=2.2, tgδ=10-3, h=1.524mm). The slot is periodically loaded by eight thin metal strips allowing the insertion of beam lead *pin* diodes (MACOM4P461). The biasing circuitry of the diodes is obtained by etching thin slits (100 μm) on the ground plane to divide the antenna into DC isolated areas. The slits are covered by a layer of adhesive tape which insures DC isolation. The adhesive layer is topped with a layer of copper tape allowing RF continuity.

In the **CPW-fed patch antenna** (Figure 5.2-16), the width of the excitation slot (500 μm) has been selected so that a beam-lead diode (MACOM4P461), which total length is 800 μm, can easily be soldered. This constraint on the maximum slot width does not prevent from a proper impedance matching because the slot width influence on the coupling quality is small for capacitively coupled antennas.

The multi frequency operation is obtained in the previous structures because the return loss is low for all working frequencies. For most microstrip antennas, this feature is not so easy to obtain. In Figure 5.2-15, the property results from the weak dependency of the return loss toward the slot width for a given resonant length. In Figure 5.2-16, it has been shown that the arms of the coupling slot have a weak influence on the matching for capacitively coupled patch antennas.

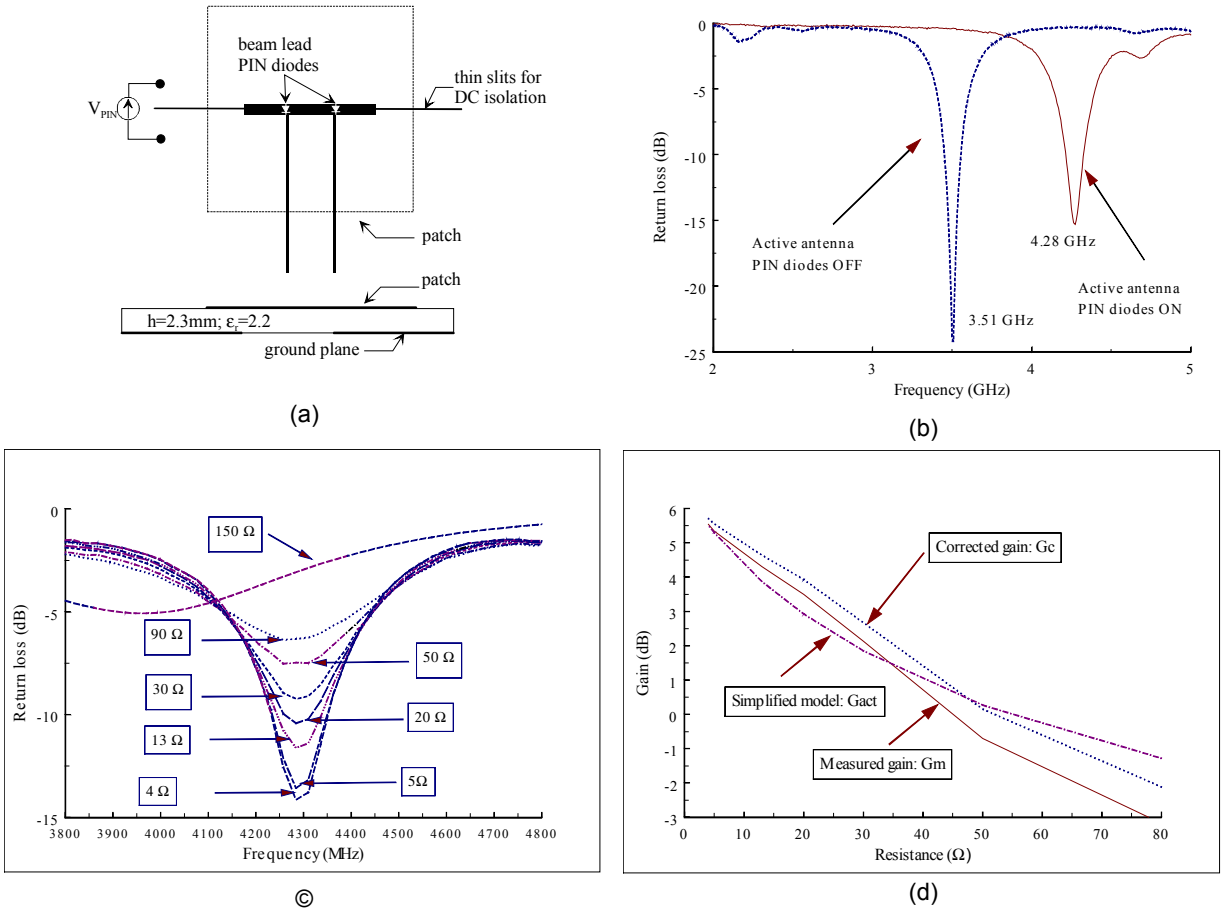
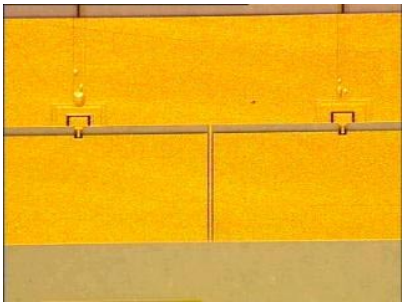


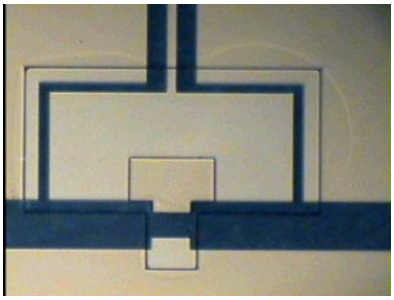
Figure 5.2-16: CPW-fed patch antenna with two symmetrical diodes inserted in the coupling slot. (a) CPW-fed patch antenna with two symmetrical diodes inserted in the coupling slot. (b) Measured return loss for both diode states. (c) Influence of the diode resistance on the resonant frequency. (d) Antenna gain as a function of the equivalent resistance of the *pin* diodes (ON state)

The resonant length can also be altered by introducing a capacitive effect inside the slot. In the **tunable MEMS-based CPW-fed slot antenna** (Figure 5.2-17), this effect is obtained by adjusting the height of two series MEMS above a slot-antenna. The basics for the resonance alteration are given in Figure 5.2-18. The antenna is fabricated with micromachining techniques by IRCOM Limoges **[PIOC02]**. MEMS capacitive shunt switches are realised with a thin dielectric layer (alumina) placed between the metal surfaces to avoid any short circuit in the low state of the MEMS (D3-b). The MEMS are packaged in a metal cavity to avoid any contact with the external environment. This cavity eliminates the radiation of the slot in the lower half space.

The cavity depth is 400 μm. The slot antenna is excited by CPW line which passes through the cavity by a small aperture. The slot is covered by a thin layer of quartz. The cavity sides have been placed after a parametric study to push up the first resonance of the cavity above 30 GHz. For the first resonance, the working frequency can theoretically be modified from 20.16 GHz to any lower frequency but the lowest frequency depends of the smallest achievable height of the membrane. As the MEMS height can hardly be controlled through the applied DC field for d<0.6 μm, we conclude that the minimum achievable resonant frequency occurs between 15 and 16 GHz which corresponds to a 22% tuning range. By controlling the membrane height above the slot, one can expect a frequency tuning/switching from 30 to 27GHz approximately for the second resonance (15% tuning range).



(a)



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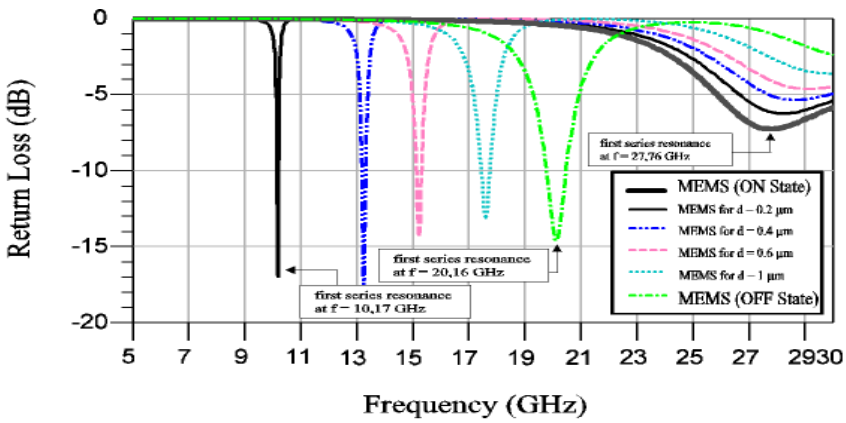

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Figure 5.2-17: Tunable MEMS-based CPW-fed slot antenna. (a) MEMS-based cavity-baked CPW-fed slot-antenna on quartz. (b) Details of the MEMs area and bias circuitry. (c) Influence of the MEMs height on the return loss

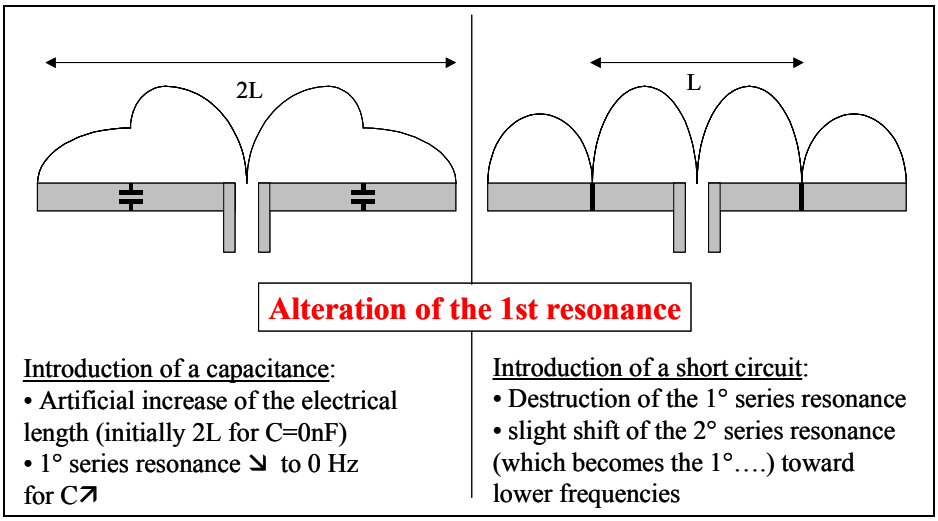

Figure 5.2-18: Basic principle for the alteration of the first resonant frequency in a slot-antenna

5.2.4 Radiating element with polarisation adjustment

5.2.4.1 General comments on polarization adjustment

The objective here is to dynamically reconfigure the antenna polarisation in order to receive (or transmit) a linearly polarized signal or a circularly polarized signal.

The polarisation adjustment may be requested by different needs:

- For a satellite antenna, the objective is to reconfigure an antenna in order to account for changes of specification while the antenna is in-orbit ;
- For other links, ability to switch polarization also helps mitigate propagation effects due to adverse weather or improve the link in a multiple path environment ;

At radiating element level, it is possible to reconfigure the polarization from circular to linear by using nearly square patch elements with MEMS actuator housed within the patch. With such an embodiment, no additional spacing is required in an array.

5.2.4.2 Nearly square patch antenna with a MEMS actuat

A first design is presented in Figure 5.2-19. It is made of a nearly square patch antenna with an integrated MEMS actuator **[SIMO02]**.

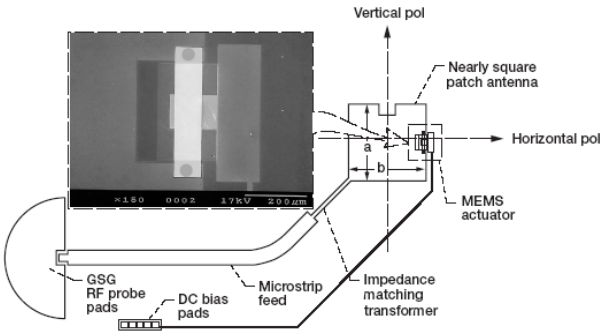

Figure 5.2-19: Polarization reconfigurable patch antenna element with integrated MEMS actuator, a = 1500 μm and b = 1492 μm. Inset shows photomicrograph of the MEMS actuator.

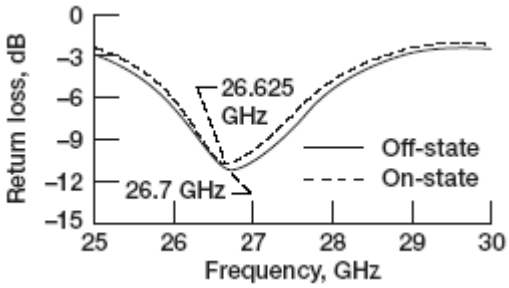

Figure 5.2-20: Measured return loss

Briefly the actuator consists of a moveable metal overpass suspended over a metal stub. The overpass is supported at both ends by metalized vias which are electrically connected to the nearly square patch antenna. The metal overpass is actuated by an electrostatic force of attraction set up by a voltage applied between the overpass and the metal stub. A dielectric film deposited over the metal stub prevents stiction when the surfaces come in contact. The nearly square patch antenna with notches is designed to support two degenerate orthogonal modes when excited at a corner. When the MEMS actuator is in the OFF-state the perturbation of the modes is negligible and hence the patch radiates a circularly polarized (CP) wave. When an electrostatic force resulting from the application of a bias pulls down the overpass, the MEMS actuator is in the ON-state. This action perturbs the phase relation between the two modes causing the patch to radiate dual linearly polarized (LP) waves.

The measured return loss for the OFF and ON states of the actuator is shown in Figure 5.2-20. The patch is well matched to the 50Ω feed line and resonates at a frequency of 26.7 GHz (OFF state) and at a frequency of 26.625 GHz (ON state). The change in the resonance frequency for the two states is considered to be negligeable. In the OFF-state the patch radiates a circularly polarized wave. The measured radiation patterns along the two orthogonal planes are shown in Figure 5.2-21. The measured axial ratio at boresight is about 2.0 Db.. In the ON-state, the patch radiates dual linearly polarized waves. The measured E- and H-plane radiation patterns for the vertical polarization are shown in Figure 5.2-22. Similar radiation patterns are observed for the horizontal polarization.

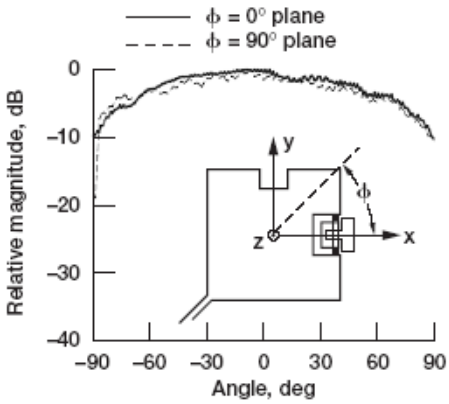

Figure 5.2-21: Measured circularly polarized radiation patterns

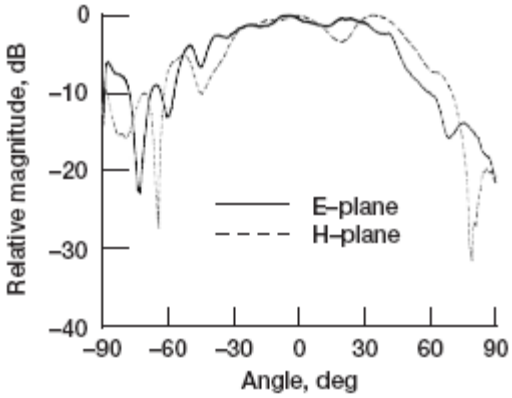

Figure 5.2-22: Measured linearly polarized radiation patterns for vertical polarization.

5.2.4.3 Nearly square patch antenna with a Scratch Drive Actuators (SDA)

Another concept of polarization-agile antenna based on Scratch Drive Actuators (SDA) **[AKIYA]** is proposed in **[LEGAR04b].** Micro-actuators are associated to metallic parasitic plates and pushed them towards the truncated corners of a circularly-polarized microstrip patch antenna (Figure 5.2-23). SDAs are constructed from a standard process including the fabrication of the metallic plates and the antenna. This antenna operates in the 47 GHz band and is processed on a 200 µm Silicon substrate (ε_r=11,8 ; σ=3,38.10^5 S/m). A 150µm-depth cavity is etched under the patch to reduce surface wave losses. The antenna is initially circularly polarized. The use of 2 SDAs arrays moving the metallic plates close to each truncated corner of the patch enables to generate a linear polarization (Figure 5.2-24).

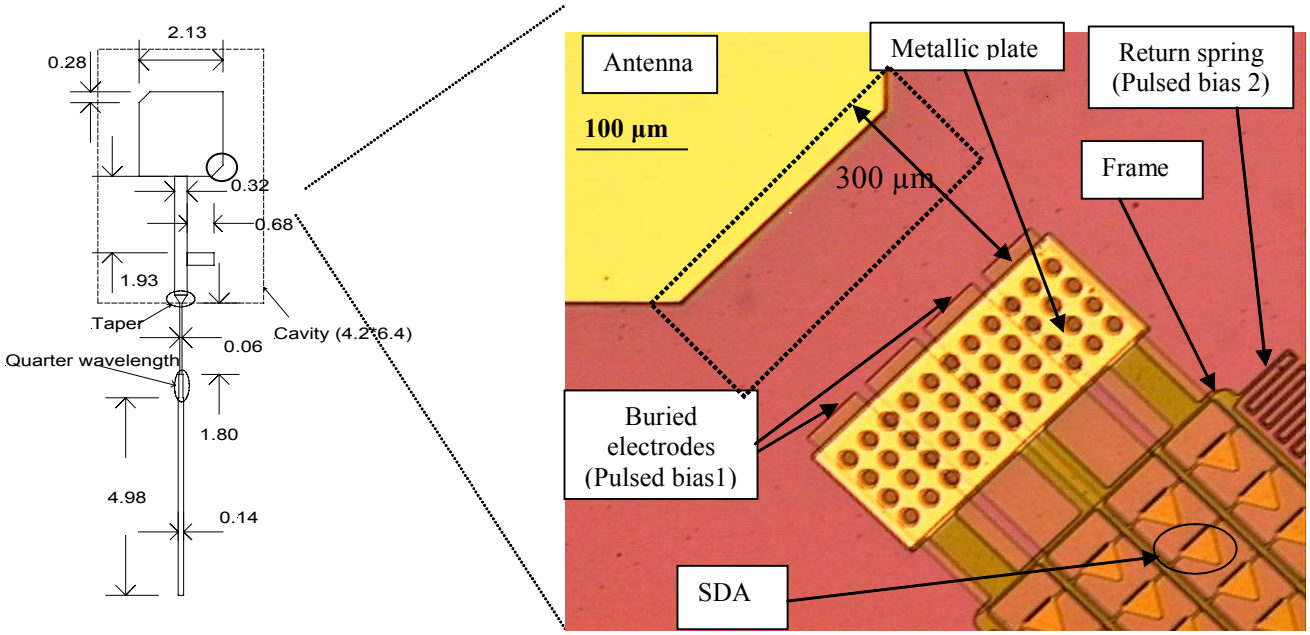

Figure 5.2-23: Schematic view of the microstrip antenna. (All dimensions are in mm) and optical microscope photograph of the system before releasing.

Figure 5.2-25 shows the variation of the theoretical axial ratio as a function of frequency: an accurate adjustment of the distance separating the parasitic plates and the truncated corners allows a continuous control of the polarization state of the radiated field. These results have been confirmed experimentally.

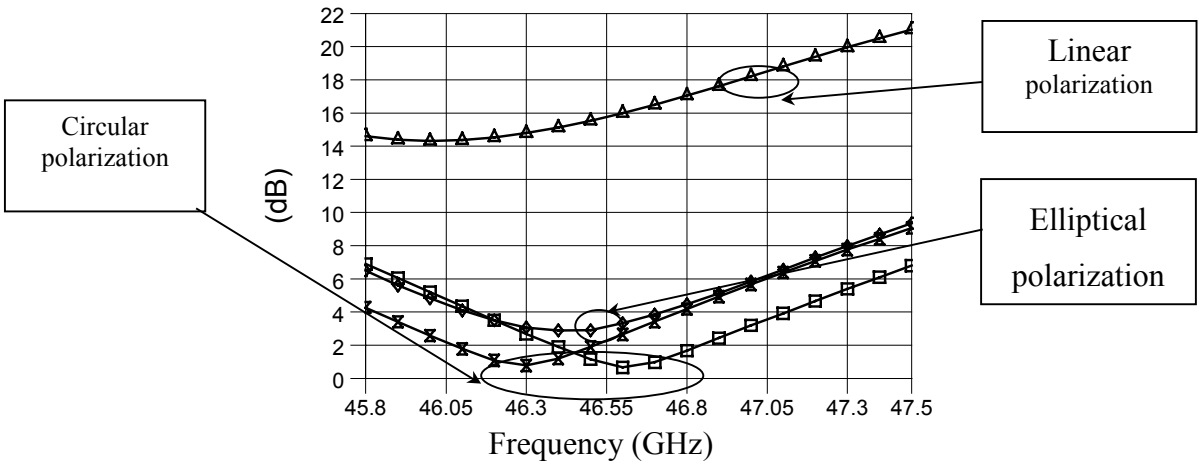

Figure 5.2-24: Simulated axial ratio

5.2.4.4 Polarization reconfigurable patch antenna via use of beam-lead pin diodes (RHCP/LHCP)

In recent papers, circular polarisation (CP) modulation was presented as a powerful modulation scheme for active read/ write microwave tagging systems (logical 1 for RHCP, logical 0 for LHCP). The polarization reconfigurable patch antenna described here has been for such an application **[BOTI00]**.

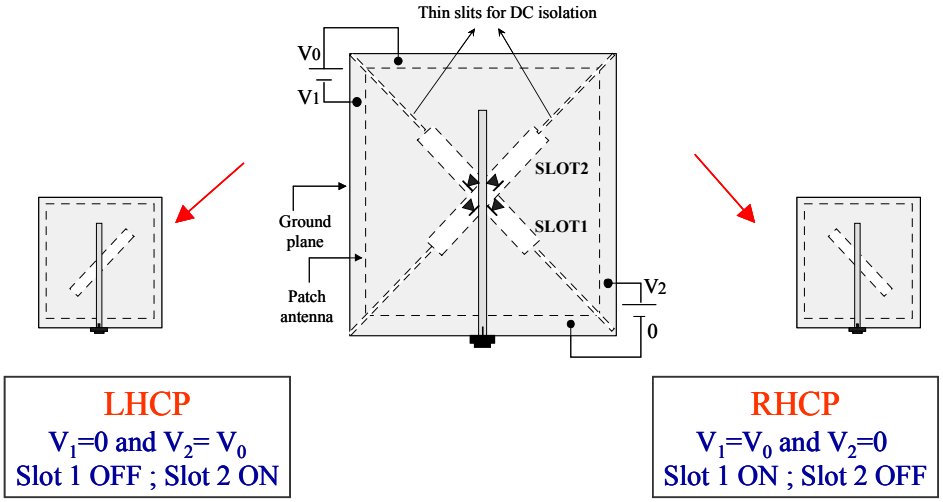

Figure 5.2-25: CP antennas with switchable polarisation sense. Design of the antennand working principles

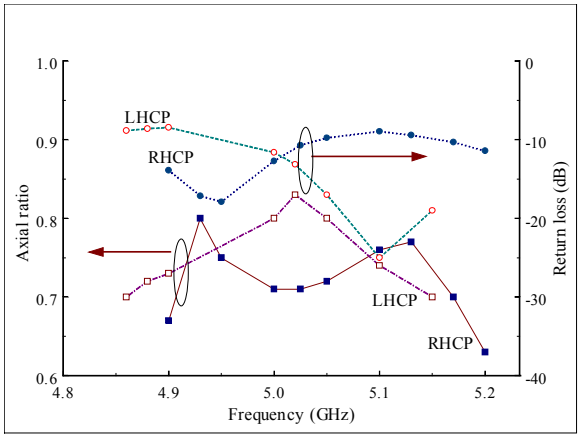

Figure 5.2-26: Experimental return loss and axial ratio at broadside for both CP configurations

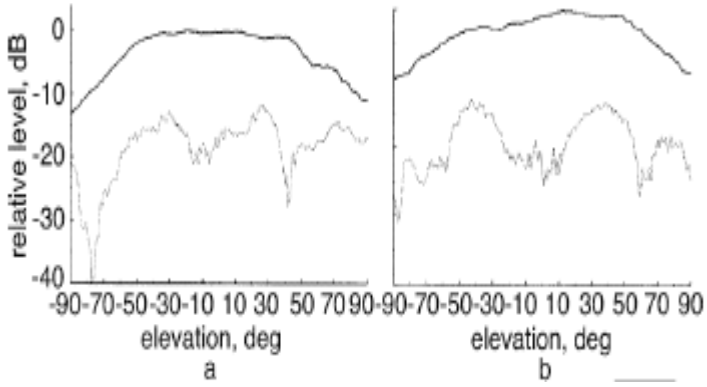

Figure 5.2-27: Radiation patterns in the RHCP configuration at 5.0 GHz in the two main planes

The basic antenna is a rectangular patch antenna excited by a single diagonal slot fed by a microstrip line. The generated modes TM10 and TM01 are linear orthogonal modes resonant at separate frequencies. To obtain a circular polarisation, they are excited in equal amplitude and 90° out of phase at 5.65GHz by adjusting the aspect ratio *Lp*/*Wp*.

The switchable antenna is depicted in Figure 5.2-25. An identical slot was added along the other diagonal. The pairs of beam-led *pin* diodes (MACOM4P461) are inserted in each coupling slot at 3mm from the intersection. By switching ON a pair of diodes while the other is OFF, one can expect to select either sense of CP. Each region is DC biased as represented symbolically. In Fig. 5, the RHCP is selected by (*V*1=*V*0= 10V,*V*2=0V) while the LHCP is obtained for (*V*1= 0V,*V*2=*V*0= 10V). The return loss and CP performances are presented in Figure 5.2-26. Owing to the fabrication tolerances, the CP bandwidths are not exactly centred at the same frequency and the CP purity is quite low (AR < 0.8). Nevertheless, a common 4% CP bandwidth is obtained with good matching performance (*S*11 < –10Db) on the overall band. Radiation patterns are given in Figure 5.2-27 for RHCP at the central frequency (5GHz) of the CP bandwidth. The measured gain is 5.5Db.

5.2.5 Integrated antenna with adjustable radiation pattern

5.2.5.1 General comments

Integrated antennas with adjustable radiation pattern have many applications, such as:

- wireless indoor network applications, in particular to improve system performance in a multi-path propagation environment,
- radar systems.

Apart from spatial and polarization diversities, radiation pattern diversity is one technique to minimize possible outage and thus allows better quality and reliability of the communication.

In this sub-section, three levels of pattern reconfiguration are considered:

- radiating element level,
- subarray level,
- phased array level with variable delay lines.

5.2.5.2 Pattern reconfiguration at radiating element level

Pattern diversity consists of an antenna output with two or more radiation patterns, resulting for example from different switch settings.

The antenna under consideration is a parasitic slot antenna **[PETI04]**. Parasitic antenna arrays are a family of arrays where strong inter-element couplings are involved and determine the radiation pattern. A three-element array is represented in Figure 5.2-28. The prototype operates in the 5GHz-6GHz band and allows for pattern diversity either at 5.25 GHz (first Hiperlan band) or 5.6GHz (second Hiperlan band). These frequencies are also close to the WLAN band around 5.8GHz. Two combinations of switchable diagrams have been studied: Broadside or Endfire with max at θ=+/-80° (Figure 5.2-29) and Left or Right radiation at ±60° (Figure 5.2-30).

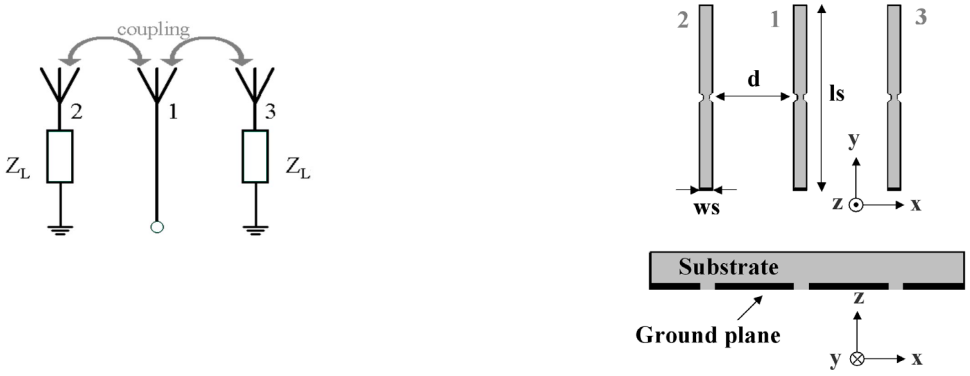

Figure 5.2-28: Principle of a three-element parasitic antenna array and implementation with three radiating slots (l_s = 29.8 mm, w_s = 2.3 mm, d = 14.5 mm ($0.28\lambda_0$)).

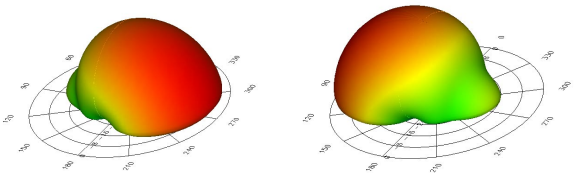

Figure 5.2-29: Right/Left patterns obtained by loading the external slots by an asymmetrical combination of loads X1-X2 or X2-X1 (with ADS Momentum)

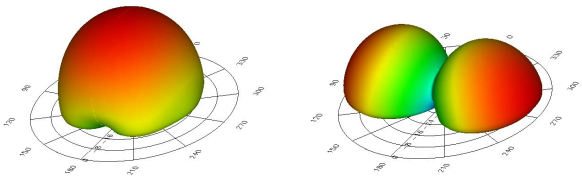

Figure 5.2-30: Broadside/Endfire obtained by loading the external slots by a symmetrical combination of loads X1-X1 or X2-X2 (with ADS Momentum)

This strong mutual coupling yields the computation of the active element pattern of the array and constitutes a key mechanism in parasitic antenna arrays. A specific CAD model of the antenna array has been developed (Figure 5.2-31) to calculate the active radiation pattern directly within the circuit simulator environment (ADS). This technique avoids unnecessary EM simulations when only the feed circuit is modified, and improves the accuracy of the design by setting optimization goals directly on the radiation pattern.

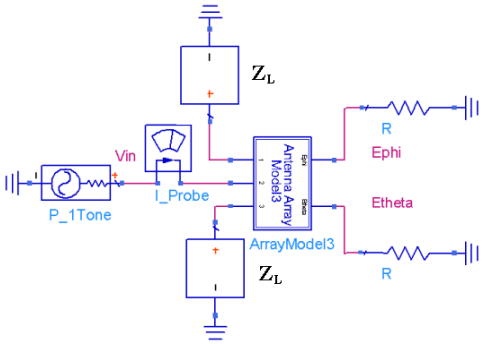

Figure 5.2-31: Simulation schematic of the parasitic antenna array in Agilent ADS.

Here, the SPA (Switched Parasitic Antenna) is realized with three radiating slots etched on a Diclad 527 substrate (ε_R=2.55 ; tanδ=0.0022 ; t=17.5µm ; h=0.762µm). The centre slot is electromagnetically coupled to a microstrip line, while the external slots are loaded by CPW stubs (Figure 5.2-32). A MEMS (packaged and thermally stimulated MIRA MEMS developed by LETI) is symmetrically inserted in each stub. Depending on the MEMS state, the loads at the input of the external slots can either be X1 or X2. A parametric study is required to optimize these loads. The model allows a fast optimization of the loading impedances X1, X2 of the parasitic radiators in order to reach specific types of radiation pattern (broadside, omnidirectional, endfire). 3D charts such as the one shown in Figure 5.2-33 are used to find the optimal load for a maximum gain in a given direction. A good matching of the antenna can eventually be obtained by adjusting the dimensions of the centre slot.

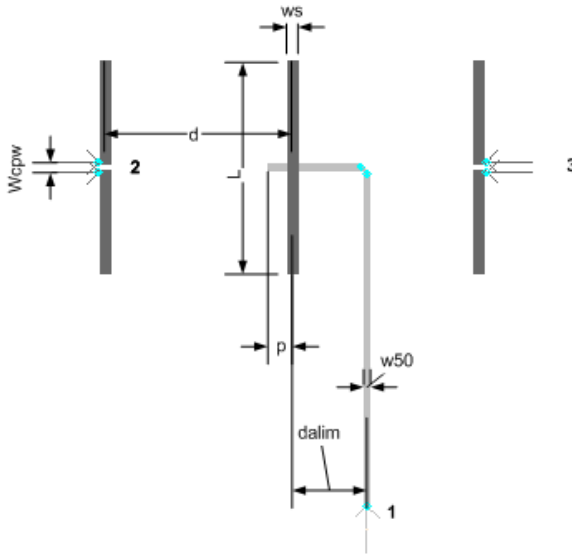

Figure 5.2-32: SPA optimized for 5.25 GHz

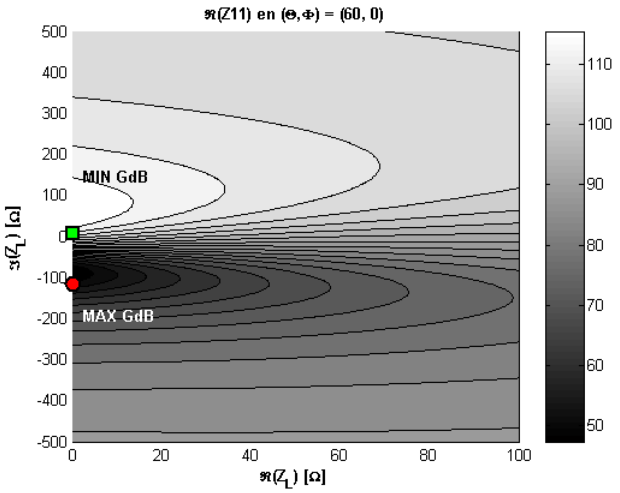

Figure 5.2-33: Gain of the array at θ = 60° as a function of the loading impedance $Z_L = R_L + jX_L$.

5.2.5.3 Pattern reconfiguration at subarray level

An intuitive concept of pattern reconfiguration at the subarray level consists in allowing to feed (or not) each radiating element of an antenna array or a subarray. For that purpose, MEMS switches can be integrated in the feeding network.

As an example, a reconfigurable CPW-fed slot microstrip 4-elements (i=1,…,4) linear array is represented in Figure 5.2-34 [LEGAR1]. The radiating elements of the array and the CPW feeding network are fabricated on opposite faces of a 400µm-thick high-resistivity Silicon (ε_r=11.8 ; tanδ=2.10^{-3}) wafer. Two 20µm-thick BCB layers (ε_r=2.65, tanδ=2.10^{-3}) are used to reduce surface wave losses (Figure 5.2-35).

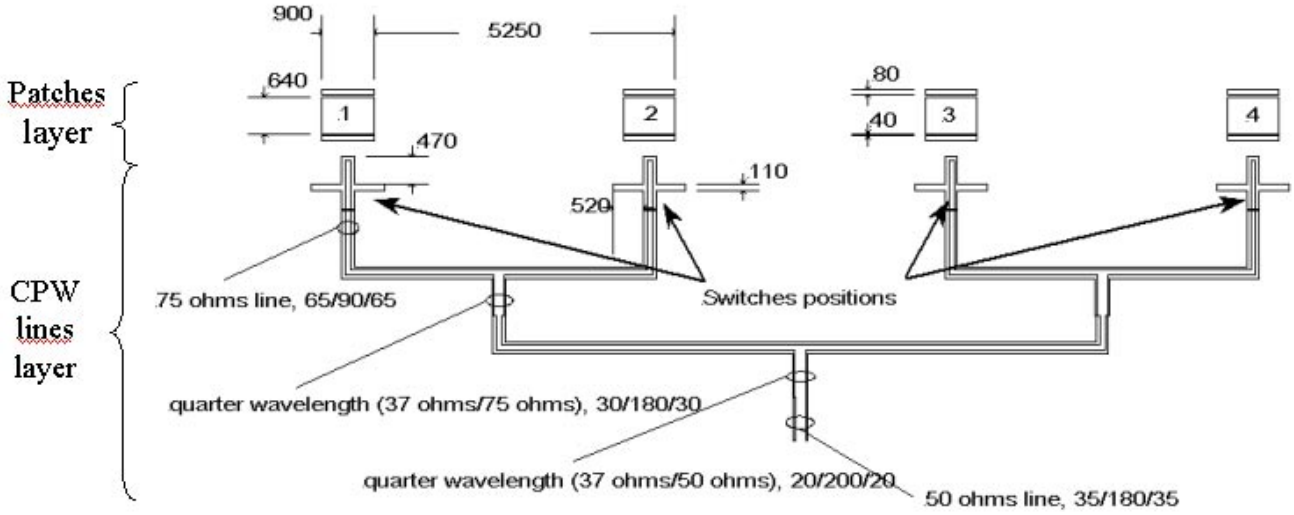

Figure 5.2-34: CPW-fed patch antenna array. Dimensions are in micrometers.

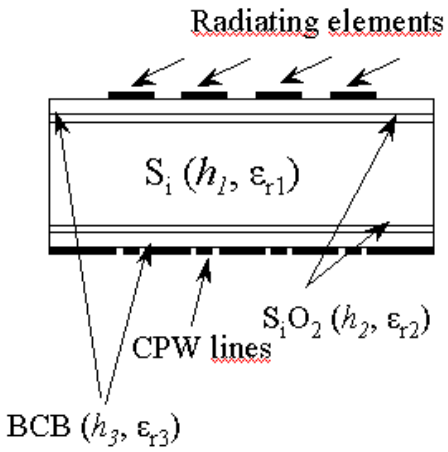

Figure 5.2-35: BCB/SiO_2/Si multilayer substrate

Four MEMS switches are integrated in the CPW transmission lines near to the coupling slots. This antenna design has two important features:

- each switch (i=1,…,4) is actuated independently: this enables to obtain a wide variety of radiation patterns. The corresponding biasing network of each switch is depicted in Figure 5.2-36,
- the length of each CPW section are designed to minimize the return loss, whatever the states of the switches. Full-wave simulations confirm that return losses remain lower than -10 dB (Figure 5.2-37), whatever the state of the switches. Six cases are considered:

  Case 1: Switch #1: Off, Switch #2: Off, Switch #3: Off, Switch #4: Off,

  Case 2: Switch #1: On, Switch #2: Off, Switch #3: Off, Switch #4: Off,

  Case 3: Switch #1: On, Switch #2: Off, Switch #3: Off, Switch #4: On,

  Case 4: Switch #1: Off, Switch #2: On, Switch #3: On, Switch #4: Off,

  Case 5: Switch #1: On, Switch #2: On, Switch #3: Off, Switch #4: Off,

  Case 6: Switch #1: On, Switch #2: On, Switch #3: On, Switch #4: Off,

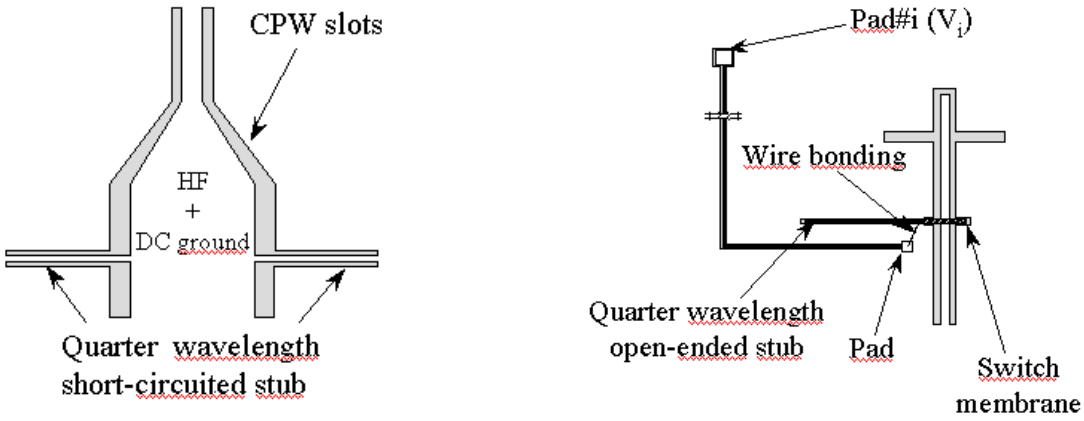

Figure 5.2-36: Biasing of the four capacitive switches. (a) The central conductor of the CPW line is used as DC ground. (b) Independent actuation of switch #i

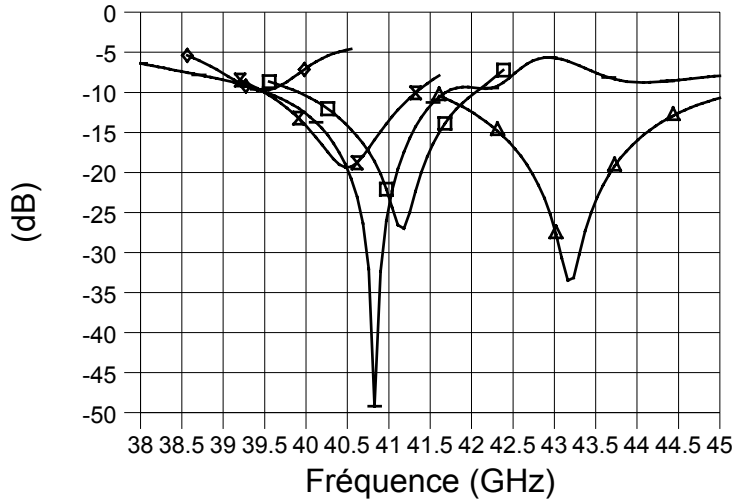

Figure 5.2-37: Computed return loss of the CPW array: Case 1, Case 2, Cases 3 and 4 Case 5, Case 6.

The radiation patterns of cases 1 and 6 are given in Figure 5.2-38 and Figure 5.2-39, respectively. These results confirm the possibility of controlling the shape of the patterns by activating or not MEMS switches integrated in an feeding network.

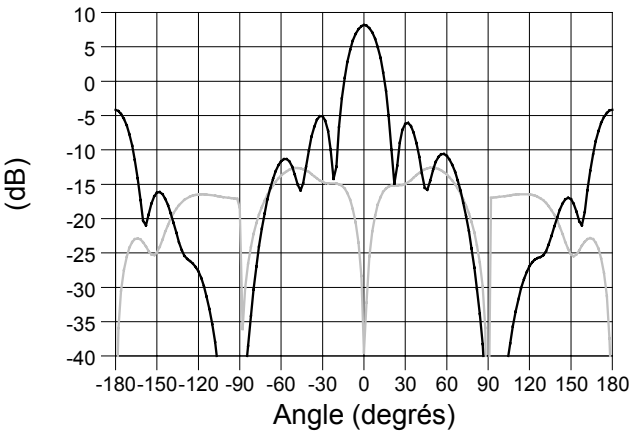

Figure 5.2-38: Theoretical radiation pattern at resonance (43 GHz) for Case 1.

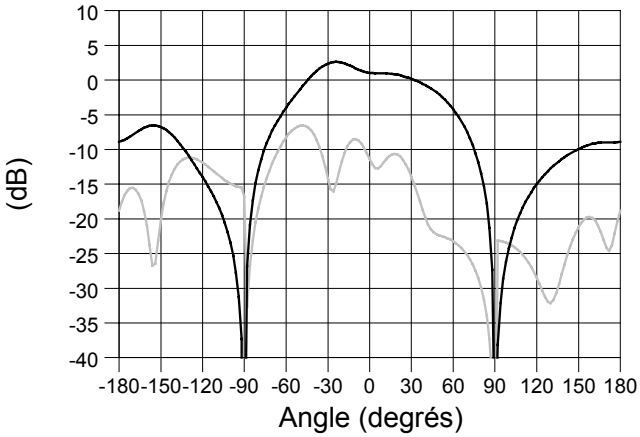

Figure 5.2-39: Theoretical radiation pattern at resonance (39.5 GHz) for Case 61.

The main drawback of this design is that the resonant frequency of the array depends on the state of the four switches. The integration of MEMS switches directly on the patch layer would enable to reconfigure the radiation patterns of the array at a *fixed* frequency **[LEGAR04a]**.

5.2.5.4 Pattern reconfiguration at phased array level with variable delay lines

5.2.5.4.1 Bandwidth of phased arrays

The bandwidth of scan phased arrays depends on the radiating elements, but also on the feed network. In general, the radiating elements are matched over a broad band and the array bandwidth is mostly determined by the feed network and phase shifters.

It is important to observe that the bandwidth of the array can be limited by different and quasi-independent factors: whereas the matching of the radiating element limit the bandwidth of the array from a *reflected energy* point of view ('matching bandwidth'), the feed network structure can also induce another form of limitation to the bandwidth, which is a *dependence of the scan angle to the frequency* (named here 'scan angle distortion bandwidth'). As will be seen below, this distortion is linked with the phase properties of the feed network.

There are naturally also other limitations to the bandwidth of arrays when getting into more details in the analysis of the performance of phased arrays, which are beyond the scope of this document. Nevertheless, it is noticeable that they are not only 'phase' issues in the role of the feed network in the array bandwidth ('scan angle distortion bandwidth') since the performance of the power splitter and the matching of the different lines in the feed network will also influence the 'matching bandwidth' of the array.

5.2.5.4.2 Corporate feed

Figure 5.2-40 depicts a one-dimensional parallel-fed phased array, also referred as *corporate* feed.

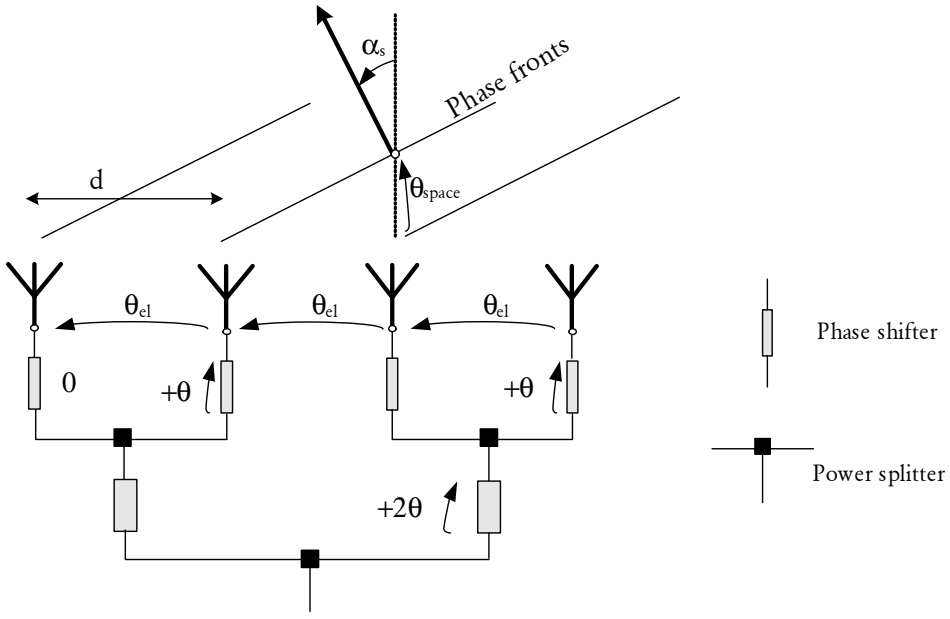

Figure 5.2-40: corporated fed phased array

By definition, all scan phased arrays used in radars need controllable phase shifter. In the case of corporate feed, we can deduce the following relation between scan angle and frequency:

$$\Delta\theta = -\frac{2\pi d}{c} \cdot \sin\alpha_s \cdot f$$

with:
- α_s: Scan angle (α_s=0 at azimuth)
- $\Delta\theta$: Phase difference between two *states* of the phase shifter
- *d*: Inter-elements distance
- *c*: Light velocity in the propagating media
- *f*: Frequency

For a narrowband array, a simple device producing the required phase shift between different states $\Delta\theta$ at the operation frequency *f* allows to scan the desired angle. However, in the case of a wide band phased array, we want the scan angle to be constant with the frequency. An observation of the above expression readily shows that this means that the phase shift $\Delta\theta$ must be proportional to the frequency. The device needed to produce the phase shift is therefore a phase shifter whose phase shift is proportional to the frequency, hence a V-TTDL.

Consequently, the 'scan angle distortion bandwidth' of a corporate-fed array with V-TTDL controllable elements corresponds to the band where the V-TTDL dispersion is below a certain level, determined by the maximum error allowed for the scan angle. If a good performance is achieved from this point of view, the actual bandwidth of the array will be determined by the 'matching bandwidth'.

The next table summarizes the requirements for the phase properties of the phase shifter in a corporate feed:

CORPORATE FEED		*Scanning*	
		No (fixed beam)	Yes
BW	Narrow band	Any line	Any V-phase shifter
	Wide band	TTDL	V-TTDL

5.2.5.4.3 Other feed types

In the case of series feed network, it can be shown that the use of V-TTDL and/or of constant-phase shifters does not allow obtaining a scan angle which is frequency-independent.

5.2.6 References

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